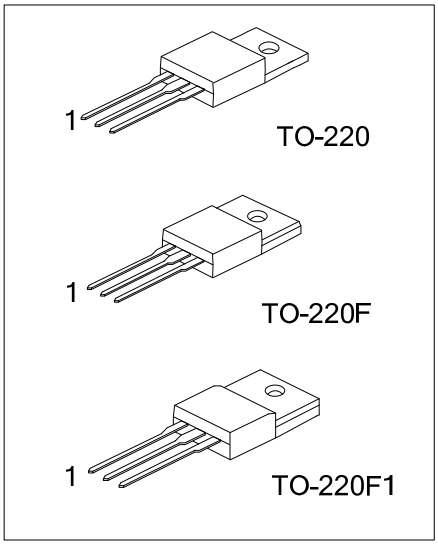
12N70

Power MOSFET

12 Amps, 700 Volts
N-CHANNEL MOSFET



■ DESCRIPTION

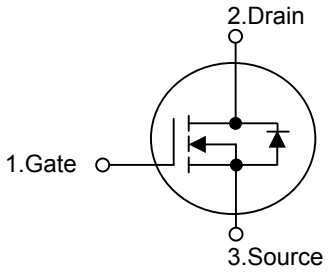
The UTC **12N70** are N-Channel enhancement mode power field effect transistors (MOSFET) which are produced using UTC's proprietary, planar stripe, DMOS technology.

These devices are suited for high efficiency switch mode power supply. To minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode the advanced technology has been especially tailored.

■ FEATURES

* $R_{DS(ON)}$ = 0.87Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 42 nC)
* Low reverse transfer capacitance (C_{RSS} = typical 25 pF)
* Fast switching capability
* Avalanche energy specified
* Improved dv/dt capability, high ruggedness

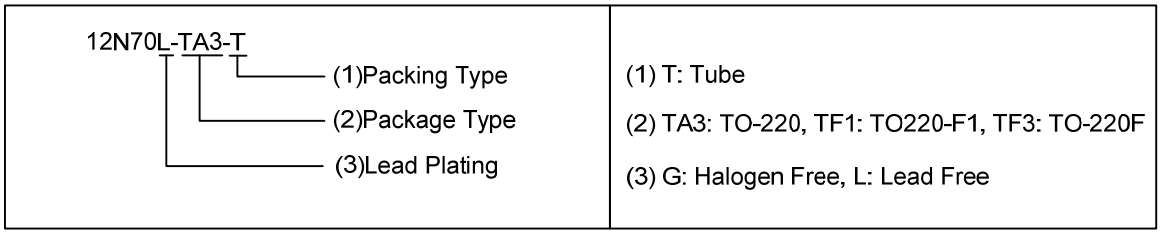
■ SYMBOL



■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free Plating	Halogen Free		1	2	3	
12N70L-TA3-T	12N70G-TA3-T	TO-220	G	D	S	Tube
12N70L-TF1-T	12N70G-TF1-T	TO-220F1	G	D	S	Tube
12N70L-TF3-T	12N70G-TF3-T	TO-220F	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source



■ ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V_{DSS}	700	V
Gate-Source Voltage		V_{GSS}	±30	V
Avalanche Current (Note 2)		I_{AR}	12	A
Drain Current	Continuous	I_D	12	A
	Pulsed (Note 2)	I_{DM}	48	A
Avalanche Energy	Single Pulsed (Note 3)	E_{AS}	790	mJ
	Repetitive (Note 2)	E_{AR}	24	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	4.5	V/ns
Power Dissipation	TO-220	P_D	225	°C/W
	TO-220F/TO-220F1		51	°C/W
Junction Temperature		T_J	+150	°C
Operating Temperature		T_{OPR}	-55 ~ +150	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Repetitive Rating : Pulse width limited by maximum junction temperature
3. L = 10mH, I_{AS} = 12A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
4. I_{SD} ≤ 12A, di/dt ≤200A/s, V_{DD} ≤BV_{DSS} Starting T_J = 25°C

■ THERMAL DATA

PARAMETER		SYMBOL	RATING	UNIT
Junction to Ambient		θ_{JA}	62.5	°C/W
Junction to Case	TO-220	θ_{JC}	0.56	°C/W
	TO-220F/TO-220F1		2.43	°C/W

■ ELECTRICAL CHARACTERISTICS (T_C =25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	700			V
Drain-Source Leakage Current	I_{DSS}	V_{DS} = 700 V, V_{GS} = 0 V			10	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
Breakdown Voltage Temperature Coefficient	$\triangle BV_{DSS}/\triangle T_J$	I_D = 250 μA, Referenced to 25°C		0.7		V/°C
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0		4.0	V
Static Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 6.0A		0.87	1.0	Ω
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{ISS}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1MHz		1480	1900	pF
Output Capacitance	C_{OSS}			200	270	pF
Reverse Transfer Capacitance	C_{RSS}			25	35	pF
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 300V, I_D = 12A, R_G = 25Ω (Note 1, 2)		30	70	ns
Turn-On Rise Time	t_R			115	240	ns
Turn-Off Delay Time	$t_{D(OFF)}$			95	200	ns
Turn-Off Fall Time	t_F			85	180	ns
Total Gate Charge	Q_G	V_{DS}= 480V,I_D= 12A, V_{GS}= 10 V (Note 1, 2)		42	54	nC
Gate-Source Charge	Q_{GS}			8.6		nC
Gate-Drain Charge	Q_{GD}			21		nC

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_S = 12A			1.4	V
Maximum Continuous Drain-Source Diode Forward Current	I_S				12	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				48	A
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 12A, dI_F/dt = 100 A/μs (Note 1)		380		ns
Reverse Recovery Charge	Q_{RR}			3.5		μC

Notes: 1. Pulse Test : Pulse width ≤300μs, Duty cycle ≤ 2%
2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

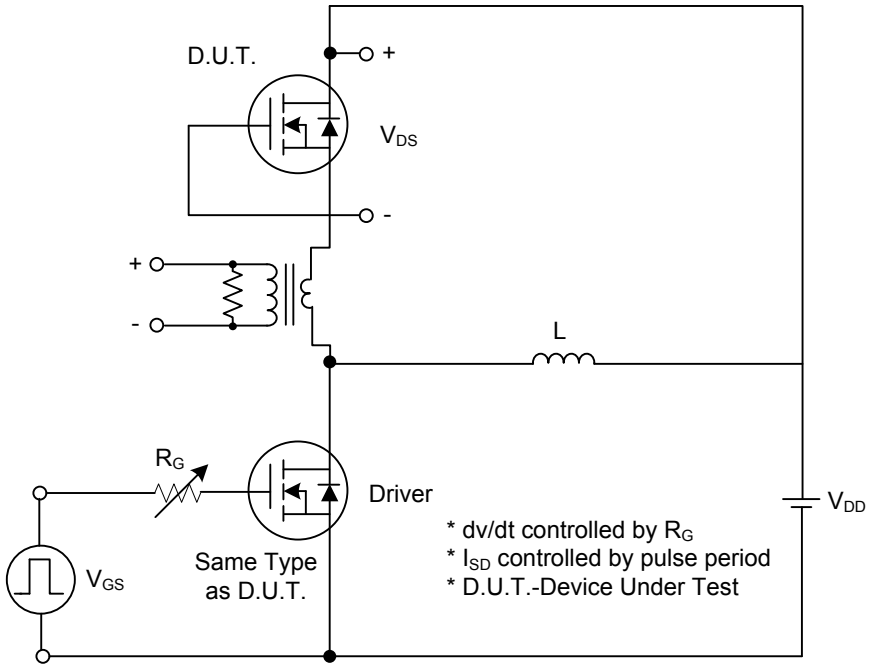


Fig. 1A Peak Diode Recovery dv/dt Test Circuit

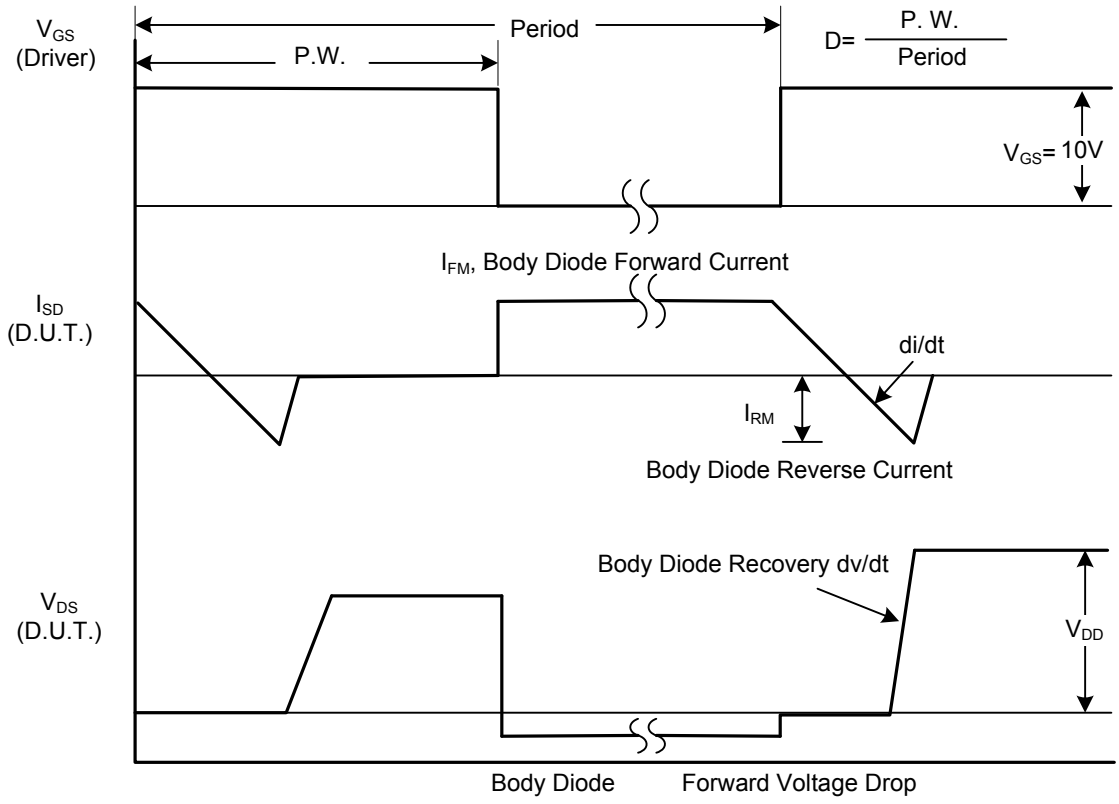


Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ TEST CIRCUITS AND WAVEFORMS (Cont.)

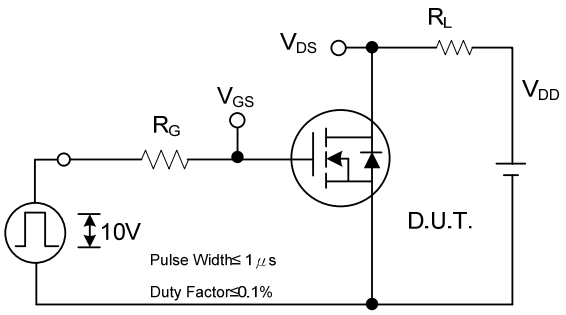


Fig. 2A Switching Test Circuit

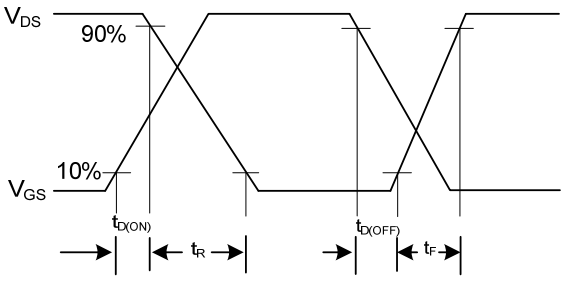


Fig. 2B Switching Waveforms

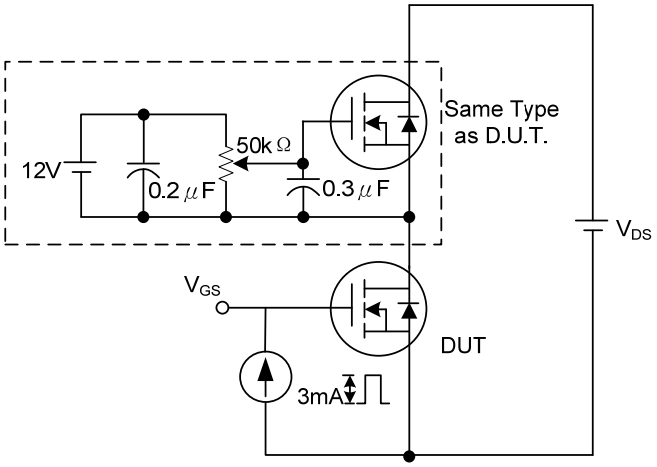


Fig. 3A Gate Charge Test Circuit

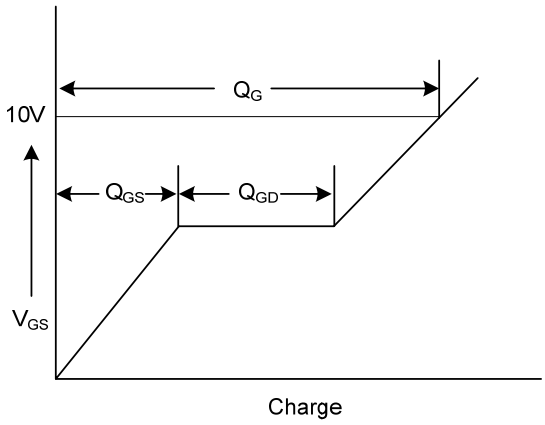


Fig. 3B Gate Charge Waveform

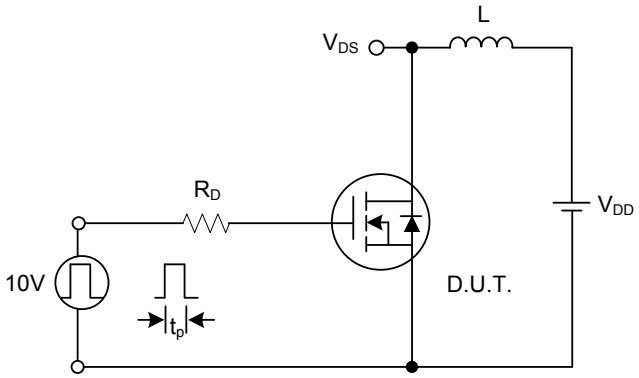


Fig. 4A Unclamped Inductive Switching Test Circuit

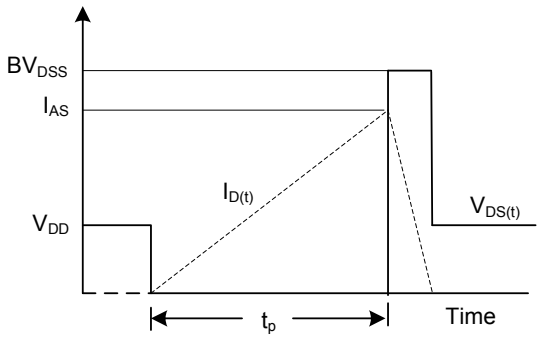


Fig. 4B Unclamped Inductive Switching Waveforms

■ TYPICAL CHARACTERISTICS