

Description

NEC's 3-volt CMOS-8L family are ultra-high performance, sub-micron gate arrays, targeted for applications requiring extensive integration and high speeds. The device processing includes an optimized 3 volt 0.5-micron (drawn) silicon-gate CMOS technology and two or three-layer metallization. This technology features channelless (sea-of-gates) architecture with an internal gate delay of 200 ps ($F/O=1$; $L=0$ mm).

The μ PD65800 series of 3 volt devices consists of 17 masters, offered in densities of 11K gates to 627K gates. Usable gates range from 6500 to 440,000 gates. These gate arrays are ideal for use in engineering workstations, high-end PCs, mainframes and LAN products, where extensive integration and high speed are primary design goals. CMOS-8L gate arrays are also well-suited for all battery-operated applications where high performance and low power consumption are critical; and feasible only with a truly optimized 3 volt CMOS process.

The μ PD65800 series are fully supported by NEC's advanced ASIC design technology. NEC's OpenCAD[®] integration system lets the designer choose the most powerful design tools and services available. The CMOS-8 macro cell (block) library is upwardly compatible with CMOS-7 and CMOS-6 block libraries. The CMOS-8L library is also functionally compatible with the CMOS-8 and CMOS-8LCX families.

Features

- Internal gate delays of 200 ps ($F/O = 1$; $L = 0$ mm)
- Channelless, 0.50 μ m CMOS architecture
- Process technology optimized for 3V operation
- Variable output drive: 6, 9, 12, 18, 24 or 48 mA
- Slew-rate controlled output buffers
- I/Os interface directly to 5V logic
- Powerful block library with more than 500 macros
- Libraries characterized at $3V \pm 10\%$ and $3.3V \pm 0.3V$
- Single/Dual-Port RAM and ROM memory blocks
- 48mA reduced voltage swing I/O buffers are in development
- Phase-lock-loop for chip-to-chip clock synchronization in development
- Advanced package options include PQFP and PGA
- Supports scan test methodology
- High pad to gate ratio optimizes silicon usage

Figure 1. Various CMOS-8L Packages

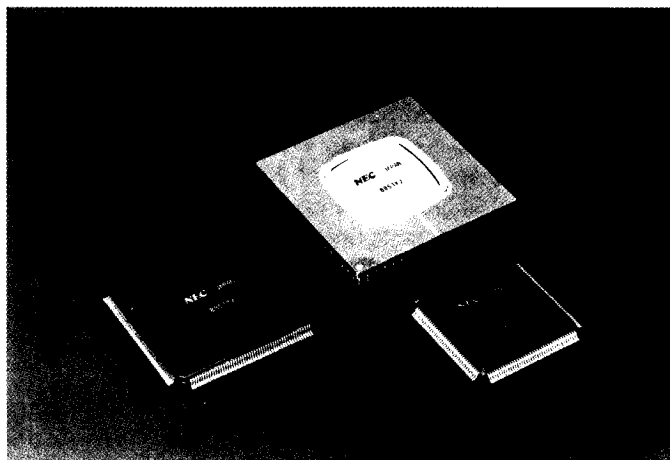


Table 1 Gate Array Sizes

Device	Available Gates	Usable Gates	Total Pads	Metal Layers
μ PD65840	10,912	6,547	164	2
μ PD65841	20,832	12,499	204	2
μ PD65842	30,192	18,115	212	2
μ PD65843	40,592	24,355	244	2
μ PD65845	52,528	31,516	276	2
μ PD65846	61,904	37,142	300	2
μ PD65865	52,528	36,769	276	3
μ PD65866	61,904	43,332	300	3
μ PD65868	81,984	57,388	340	3
μ PD65869	102,272	71,590	380	3
μ PD65870	120,768	84,537	412	3
μ PD65871	148,256	103,779	452	3
μ PD65872	202,752	141,926	524	3
μ PD65873	255,744	179,020	588	3
μ PD65875	342,000	239,400	676	3
μ PD65878	488,720	342,104	804	3
μ PD65879	627,328	439,129	908	3

Actual gate utilization may vary depending on circuit implementation. Utilization is 70% for three-layer metal; 60% for two-layer metal. Depending on package and circuit specification, some pads are used for V_{DD} and GND and are not available as signal pads.

Circuit Architecture

CMOS-8L products are built with NEC's 0.50-micron (drawn) channelless gate array architecture. As shown in figure 2, CMOS gate array chips are divided into I/O and internal cell areas. The I/O cell area contains input and output buffers that isolate the internal cells from high-energy external signals. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design. A cell configured as a two-input NAND gate is shown in figure 3. These p-channel and n-channel transistors are sized to offer a superb ratio of speed to silicon area.

Output Slew-Rate Selection

Fast rise and fall times of CMOS output buffers can cause system noise and signal overshoot. When an unterminated line is being driven by a buffer, the maximum line length is determined by the rise and fall time of the output buffers and the round-trip signal delay of the line.

Figure 2. Chip Layout and Internal Cell Configuration

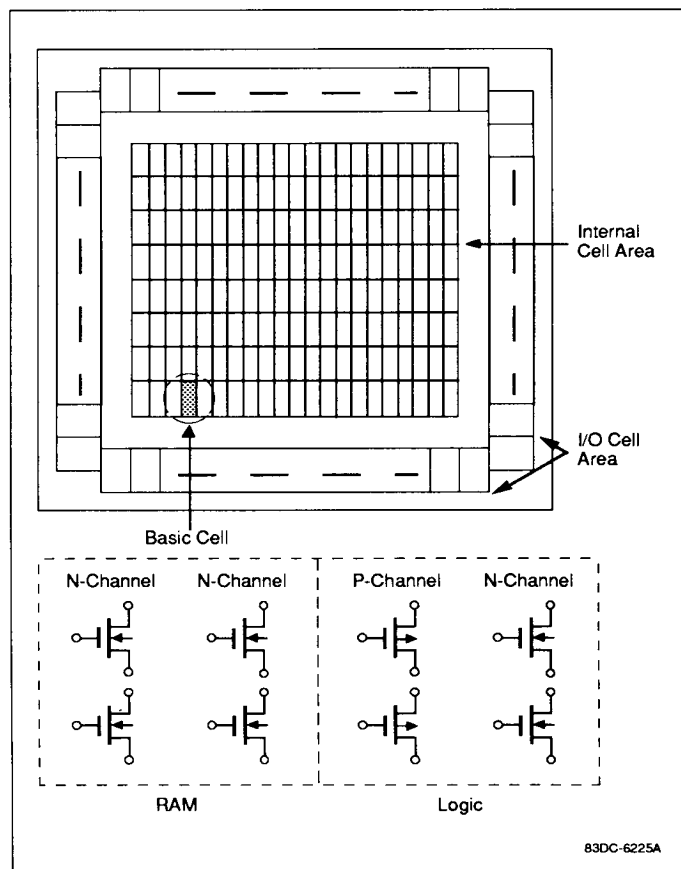
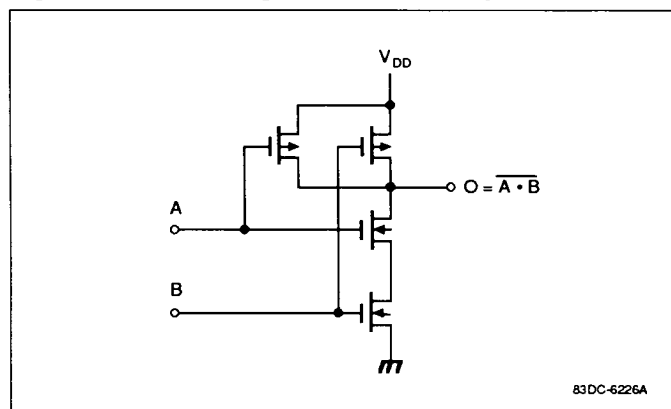


Figure 3. Cell Configured as a Two-Input NAND



As a general rule, the round-trip delay of the line should not exceed the rise or fall time of the driving signal. Transmission lines that are longer than those determined by this rule can degrade system performance due to reflections and ringing. One benefit of slew-rate output buffers is that longer interconnections on a PC board and routing flexibility are possible.

ASIC designers, therefore, can slow down the output edge-rate by using a slew-rate output buffer and thus accommodate longer transmission lines on PC boards.

Slew-rate buffers also inject less noise into the internal power and ground busses of the device, than their non-slew-rate counterparts. As a consequence, slew-rate buffers require fewer power/ground pairs for simultaneous switching outputs.

Packaging and Test

CMOS-8L gate arrays support automatic test generation through a scan-test methodology, which allows higher fault coverage, easier testing and quicker development time. NEC also offers advanced packaging solutions including (butt-lead) PGAs and flat packages. These packages give CMOS-8L devices a distinct performance edge in high-integration applications.

Publications

This data sheet contains preliminary specifications, package information, and operational data for the CMOS-8L gate array families. Additional design information will be available in NEC's CMOS-8L Block Library and CMOS-8L Design Manual. Contact your local NEC Design Center or the NEC Literature Center for further ASIC design information; see the back of this data sheet for locations and phone numbers.

Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to +4.6 V
3V interface I/O voltage	-0.5 V to $V_{DD} + 0.5$ V
5V interface I/O voltage	-0.5 V to $V_{DD} + 3.0$ V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; $f = 1$ MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note: (1) Values include package pin capacitance.

Power Consumption at $V_{DD} = 3.3$ V $\pm$ 0.3V

Description	Limits (max)	Unit	Test Conditions
Internal cell	3.27	μ W/MHz	$V_{DD} = 3.3$ V
Input block (FI01)	10.0	μ W/MHz	$V_{DD} = 3.3$ V
Output block	0.181	mW/MHz	$C_L = 15$ pF

Recommended Operating Conditions at $V_{DD} = 3.3$ V $\pm$ 0.3V

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	2.7	3.6	V
Ambient temperature	T_A	-40	+85	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	ns
Input rise or fall time, Schmitt	t_R, t_F	0	10	ms
Positive Schmitt-trigger voltage	V_P	TBD	TBD	V
Negative Schmitt-trigger voltage	V_N	TBD	TBD	V
Hysteresis voltage	V_H	TBD	TBD	V

AC Characteristics at $V_{DD} = 3.3$ V $\pm$ 0.3V; $T_A = -40$ to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	175			MHz	D-F/F; F/O = 2
Delay time, 2-input NAND gate	t_{PD}		189		ps	F/O = 1; L = 0 mm @ $V_{DD} = 3.3$ V
	t_{PD}		367		ps	F/O = 2; L = 2 mm @ $V_{DD} = 3.3$ V
Delay time, buffer						
	Input (FI01)		1.1		ns	F/O = 1; L = 0 mm @ $V_{DD} = 3.3$ V
	Output (FO06)		2.0		ns	$C_L = 15$ pF @ $V_{DD} = 3.3$ V
Output rise time (FO06)	t_R		1.1		ns	$C_L = 15$ pF @ $V_{DD} = 3.3$ V
Output fall time (FO06)	t_F		1.1		ns	$C_L = 15$ pF @ $V_{DD} = 3.3$ V

Absolute Maximum Ratings

Power supply voltage, V_{DD}	-0.5 to +4.6 V
3V interface I/O voltage	-0.5 V to $V_{DD} + 0.5$ V
5V interface I/O voltage	-0.5 V to $V_{DD} + 3.0$ V
Latch-up current, I_{LATCH}	>1 A (typ)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +150°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should not be operated outside the recommended operating conditions.

Input/Output Capacitance

$V_{DD} = V_I = 0$ V; $f = 1$ MHz

Terminal	Symbol	Typ	Max	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Power Consumption at $V_{DD} = 3.0$ V $\pm$ 10%

Description	Limits (max)	Unit	Test Conditions
Internal cell	2.70	μ W/MHz	$V_{DD} = 3.0$ V
Input block (FI01)	8.0	μ W/MHz	$V_{DD} = 3.0$ V
Output block	0.164	mW/MHz	$C_L = 15$ pF

Recommended Operating Conditions at $V_{DD} = 3.0$ V $\pm$ 10%

Parameter	Symbol	Min	Max	Unit
Power supply voltage	V_{DD}	2.7	3.6	V
Ambient temperature	T_A	-40	+85	°C
Low-level input voltage	V_{IL}	0	0.3 V_{DD}	V
High-level input voltage	V_{IH}	0.7 V_{DD}	V_{DD}	V
Input rise or fall time	t_R, t_F	0	200	ns
Input rise or fall time, Schmitt	t_{R*}, t_{F*}	0	10	ms
Positive Schmitt-trigger voltage	V_P	TBD	TBD	V
Negative Schmitt-trigger voltage	V_N	TBD	TBD	V
Hysteresis voltage	V_H	TBD	TBD	V

AC Characteristics at $V_{DD} = 3.0$ V $\pm$ 10%; $T_A = -40$ to +85°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Toggle frequency	f_{TOG}	175			MHz	D-F/F; F/O = 2
Delay time, 2-input NAND gate	t_{PD}		206		ps	F/O = 1; L = 0 mm @ $V_{DD} = 3.0$ V
	t_{PD}		400		ps	F/O = 2; L = 2 mm @ $V_{DD} = 3.0$ V
Delay time, buffer						
	Input (FI01)		TBD		ns	F/O = 1; L = 0 mm @ $V_{DD} = 3.0$ V
	Output (FO06)		TBD		ns	$C_L = 15$ pF @ $V_{DD} = 3.0$ V
Output rise time (FO06)	t_R		TBD		ns	$C_L = 15$ pF @ $V_{DD} = 3.0$ V
Output fall time (FO06)	t_F		TBD		ns	$C_L = 15$ pF @ $V_{DD} = 3.0$ V

DC Characteristics

$V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ or $3 \text{ V} \pm 10\%$; $T_A = -40$ to $+85$ °C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Quiescent current (Note 1)	I_L		TBD	TBD	μA	$V_I = V_{DD}$ or GND
Input leakage current						
Regular	I_I		TBD	TBD	μA	$V_I = V_{DD}$ or GND
50 k Ω pull-up	I_I	TBD	TBD	TBD	μA	$V_I = \text{GND}$
5 k Ω pull-up	I_I	TBD	TBD	TBD	mA	$V_I = \text{GND}$
50 k Ω pull-down	I_I	TBD	TBD	TBD	μA	$V_I = V_{DD}$
Off-state output leakage current	I_{OZ}			TBD	μA	$V_O = V_{DD}$ or GND
Input clamp voltage	V_{IC}	TBD			V	$I_I = 18 \text{ mA}$
Output short circuit current (Note 2)	I_{OS}	TBD			mA	$V_O = 0 \text{ V}$
Low-level output current						
6 mA	I_{OL}	-6			mA	$V_{OL} = 0.4 \text{ V}$
9 mA	I_{OL}	-9			mA	$V_{OL} = 0.4 \text{ V}$
12 mA	I_{OL}	-12			mA	$V_{OL} = 0.4 \text{ V}$
18 mA	I_{OL}	-18			mA	$V_{OL} = 0.4 \text{ V}$
24 mA	I_{OL}	-24			mA	$V_{OL} = 0.4 \text{ V}$
48 mA	I_{OL}	-48			mA	$V_{OL} = 0.4 \text{ V}$
High-level output current						
6 mA	I_{OH}	6			mA	$V_{OH} = 2.4 \text{ V}$
9 mA	I_{OH}	9			mA	$V_{OH} = 2.4 \text{ V}$
12 mA	I_{OH}	12			mA	$V_{OH} = 2.4 \text{ V}$
18 mA	I_{OH}	18			mA	$V_{OH} = 2.4 \text{ V}$
24 mA	I_{OH}	24			mA	$V_{OH} = 2.4 \text{ V}$
48 mA	I_{OH}	48			mA	$V_{OH} = 2.4 \text{ V}$
Low-level output voltage	V_{OL}			0.1	V	$I_{OL} = 0 \text{ mA}$
High-level output voltage	V_{OH}	$V_{DD} - 0.1$			V	$I_{OH} = 0 \text{ mA}$

Notes:

- (1) The maximum value reflects the use of pull-up/pull-down resistors and oscillator blocks. Contact an NEC ASIC Design Center for assistance in calculation.
- (2) Rating is for only one output operating in this mode for less than 1 second.

Table 2 CMOS-8L Package Options

Master Slice	μ PD65xxx	-840	-841	-842	-843	-845	-865	-846	-866	-868
Maximum I/O Pins		164	204	212	244	276	276	300	300	340
Plastic Quad Flatpack (PQFP)										
120-pin	(0.8 mm)	P	P	A	A	A	A	A	A	A
136-pin	(0.65 mm)	P	P	P	P	A	A	A	A	A
160-pin	(0.65 mm)	D	D	D	D	D	D	A	A	A
Plastic Quad Flatpack (PQFP-FP)										
100-pin	(0.5 mm)	P	A	A	A	A	A	A	A	A
120-pin	(0.5 mm)	P	P	P	A	A	A	A	A	A
144-pin	(0.5 mm)	P	P	P	P	A	A	A	A	A
160-pin	(0.5 mm)	D	D	D	D	D	D	A	A	A
176-pin	(0.5 mm)	—	D	D	D	D	D	D	D	D
208-pin	(0.5 mm)	—	—	D	D	D	D	D	D	D
240-pin	(0.5 mm)	—	—	—	D	D	D	D	D	D
272-pin	(0.5 mm)	—	—	—	—	D	D	D	D	D
304-pin	(0.5 mm)	—	—	—	—	—	—	—	—	D
Plastic Quad Flatpack (PQFP-VFP)										
256-pin	(0.4 mm)	—	—	—	—	D	D	D	D	D
Ceramic Pin Grid Array (CPGA)										
72-pin		A	A	A	A	A	A	A	A	A
132-pin		P	P	P	P	A	A	A	A	A
176-pin		—	P	P	P	P	P	P	P	P
208-pin		—	—	P	P	P	P	P	P	P
280-pin		—	—	—	—	—	—	P	P	P
364-pin		—	—	—	—	—	—	—	—	—
Ceramic Pin Grid Array (CPGA) Butt-Lead										
288-pin		—	—	—	—	—	—	P	P	P
528-pin		—	—	—	—	—	—	—	—	—

A = Available with first release
 P = Planned
 D = In Development
 — = Unavailable or not planned

NOTE:

NEC reserves the right to alter the package plan based on the results of qualification. For current package availability, please contact your local NEC Design Center.

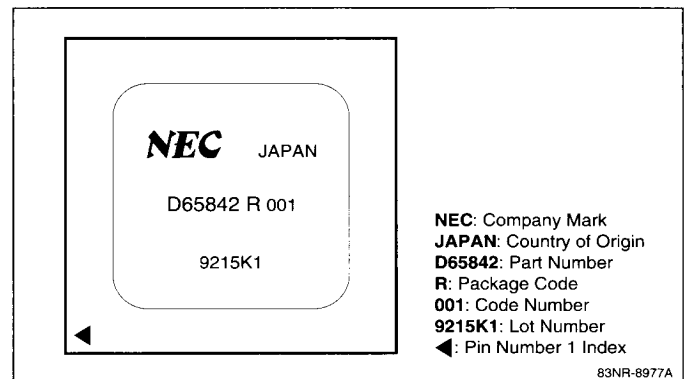
Typical CMOS-8L Package Marking


Table 2 CMOS-8L Package Options (cont)

Master Slice	μPD65xxx	-869	-870	-871	-872	-873	-875	-878	-879
Maximum I/O Pins		380	412	452	524	588	676	804	908
Plastic Quad Flatpack (PQFP)									
120-pin	(0.8 mm)	A	A	A	A	A	A	A	A
136-pin	(0.65 mm)	A	A	A	A	A	A	A	A
160-pin	(0.65 mm)	A	A	A	A	A	A	A	A
Plastic Quad Flatpack (PQFP-FP)									
100-pin	(0.5 mm)	A	A	A	—	—	—	—	—
120-pin	(0.5 mm)	A	A	A	A	A	A	—	—
144-pin	(0.5 mm)	A	A	A	A	A	A	—	—
160-pin	(0.5 mm)	A	A	A	A	A	A	A	—
176-pin	(0.5 mm)	A	A	A	A	A	A	A	A
208-pin	(0.5 mm)	D	D	A	A	A	A	A	A
240-pin	(0.5 mm)	D	D	D	A	A	A	A	A
272-pin	(0.5 mm)	D	D	D	A	A	A	A	A
304-pin	(0.5 mm)	D	D	D	D	A	A	A	A
Plastic Quad Flatpack (PQFP-VFP)									
256-pin	(0.4 mm)	D	D	D	A	A	A	A	A
Ceramic Pin Grid Array (CPGA)									
72-pin		A	A	A	A	A	A	A	A
132-pin		A	A	A	A	A	A	A	A
176-pin		P	A	A	A	A	A	A	A
208-pin		P	P	A	A	A	A	A	A
280-pin		P	P	P	P	A	A	A	A
364-pin		P	P	P	P	P	P	A	A
Ceramic Pin Grid Array (CPGA) Butt-Lead									
288-pin		P	P	P	P	A	A	A	A
528-pin		—	—	P	—	P	P	P	P

A = Available with first release

P = Planned

D = In Development

— = Unavailable or not planned

NOTE:

NEC reserves the right to alter the package plan based on the results of qualification. For current package availability, please contact your local NEC Design Center.

NEC's ASIC Design System

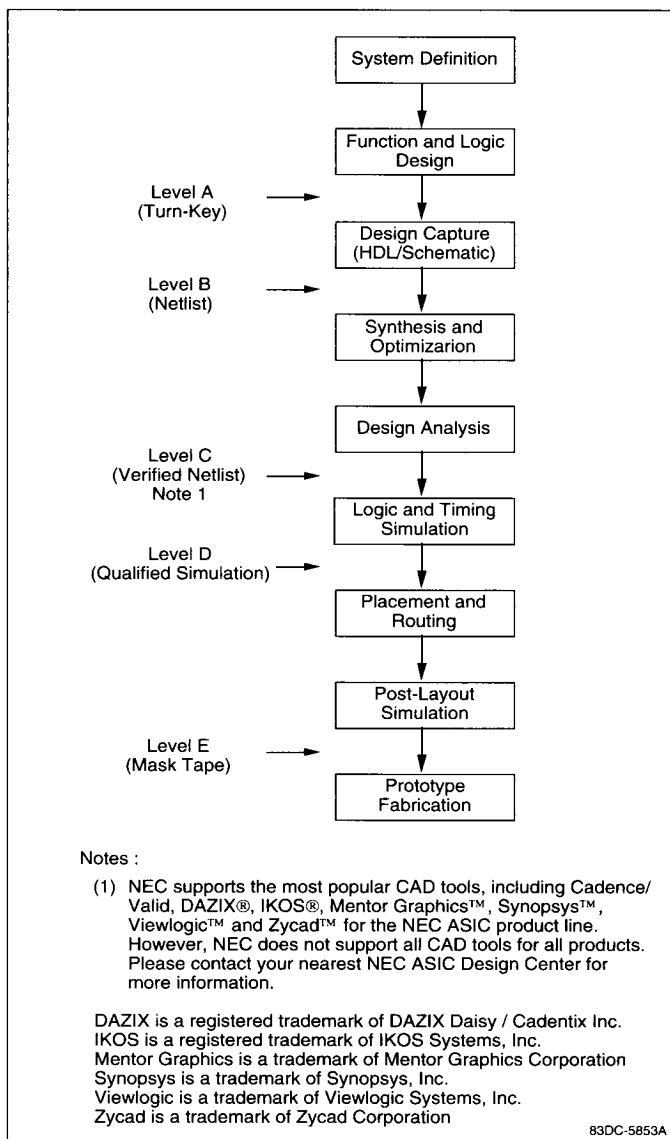
CMOS-8L gate arrays are fully supported by NEC's network of ASIC Design Centers, listed on the back of this data sheet.

Design flow for CMOS-8L gate arrays is shown in figure 4. Users can enlist Design Center support at any step in the design flow before actual manufacturing. Figure 4 shows the various levels at which Design Center support may begin — anywhere from level A through level E. Level C, "Verified Netlist," is the most popular interface.

NEC supports its ASIC products with a comprehensive CAD system that significantly reduces the time and expense usually associated with the development of semi-custom devices. NEC's OpenCAD® integration system supports tools for floorplanning, logic synthesis, automatic test generation, accelerated fault-grading, full timing simulation and advanced place-and-route algorithms. These advanced CAD tools help ensure accurate designs.

Sample design kits are available at no charge to qualified users: contact an NEC ASIC Design Center for more information. (Software licensing required—NEC reserves the right to prioritize support based on user requirements.)

Figure 4. Gate Array Design Flow



Block Library List

The CMOS-8L family offers a variety of blocks, including gates, flip-flop circuits, and shift registers. The functions of these blocks are designed to be compatible with those of the CMOS-8, CMOS-7 and CMOS-6 families. In addition, memory blocks such as RAM and ROM will be provided, and low-power gates are available. The low-power blocks are designed for gate count reduction; the number of cells are fewer than that of the standard block, contributing to lower power consumption and higher efficiency. Another feature is the I/Os can directly interface to 5V logic.

Block List

Block Name	Description	I _{OL} (mA)	Cells
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Interface Blocks

3V CMOS Input Buffers

FI01	3V CMOS input	-	1 (3)
FID1	3V CMOS input, 50 kΩ pull-down	-	1 (3)
FIU1	3V CMOS in, 50 kΩ pull-up	-	1 (3)
FIW1	3V CMOS in, 5 kΩ pull-up	-	1 (3)
FIS1	3V CMOS Schmitt input	-	1 (8)
FDS1	3V CMOS Schmitt input, 50 kΩ pull-down	-	1 (8)
FUS1	3V CMOS Schmitt input, 50 kΩ pull-up	-	1 (8)
FWS1	3V CMOS Schmitt input, 5 kΩ pull-up	-	1 (8)
FIB1	3V CMOS input, high fanout for clock driver	-	1 (24)
FDB1	3V CMOS input, high fanout for clock driver, 50 kΩ pull-down	-	1 (24)
FUB1	3V CMOS input, high fanout for clock driver, 50 kΩ pull-up	-	1 (24)
FWB1	3V CMOS input, high fanout for clock driver, 5 kΩ pull-up	-	1 (24)

3V CMOS Input Buffers without Protection Diode up to V_{DD}

FIA1	3V CMOS input	-	1 (3)
FDA1	3V CMOS input, 50 kΩ pull-down	-	1 (3)
FUA1	3V CMOS input, 50 kΩ pull-up	-	1 (3)
FWA1	3V CMOS input, 5 kΩ pull-up	-	1 (3)
FIE1	3V CMOS Schmitt input	-	1 (8)
FDE1	3V CMOS Schmitt input, 50 kΩ pull-down	-	1 (8)
FUE1	3V CMOS Schmitt input, 50 kΩ pull-up	-	1 (8)
FWE1	3V CMOS Schmitt input, 5 kΩ pull-up	-	1 (8)
FIH1	3V CMOS input, high fanout for clock driver	-	1 (24)
FDH1	3V CMOS input, high fanout for clock driver, 50 kΩ pull-down	-	1 (24)
FUH1	3V CMOS input, high fanout for clock driver, 50 kΩ pull-up	-	1 (24)
FWH1	3V CMOS input, high fanout for clock driver, 5 kΩ pull-up	-	1 (24)

5V CMOS Input Buffers

FIV1	5V CMOS input	-	1 (3)
FDV1	5V CMOS input, 50 kΩ pull-down	-	1 (3)
FIF1	5V CMOS Schmitt input	-	1 (8)
FDF1	5V CMOS Schmitt input, 50 kΩ pull-down	-	1 (8)
FIG1	5V CMOS input, high fanout for clock driver	-	1 (24)
FDG1	5V CMOS input, high fanout for clock driver, 50 kΩ pull-down	-	1 (24)

Block Name	Description	I _{OL} (mA)	Cells
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Interface Blocks (Cont.)

3V CMOS Output Buffers

FO0A	3V CMOS output	1.0	1 (4)
FO0B	3V CMOS output	2.0	1 (4)
FO09	3V CMOS output	3.0	1 (4)
FO04	3V CMOS output	6.0	1 (4)
FO01	3V CMOS output	9.0	1 (4)
FO02	3V CMOS output	12.0	1 (4)
FO03	3V CMOS output	18.0	1 (8)
FO06	3V CMOS output	24.0	1 (8)
FO0C	3V CMOS output	48.0	2 (8)

3V CMOS Slew-Rate Output Buffers

FE02	3V CMOS output, low noise	12.0	1 (3)
FE03	3V CMOS output, low noise	18.0	1 (3)
FE06	3V CMOS output, low noise	24.0	1 (3)
FE0C	3V CMOS output, low noise	48.0	2 (3)

5V CMOS Output Buffers

FV0A	5V CMOS output	1.0	1 (4)
FV0B	5V CMOS output	2.0	1 (4)
FV09	5V CMOS output	3.0	1 (4)
FV04	5V CMOS output	6.0	1 (4)
FV01	5V CMOS output	9.0	1 (8)
FV02	5V CMOS output	12.0	2 (8)
FV03	5V CMOS output	18.0	2 (8)
FV06	5V CMOS output	24.0	3 (8)

5V CMOS Slew-Rate Output Buffers

FW02	5V CMOS output, low noise	12.0	2 (3)
FW02	5V CMOS output, low noise	18.0	2 (3)
FW06	5V CMOS output, low noise	24.0	3 (3)

3V CMOS Three-State Output Buffers

B00T	3V CMOS output	3.0	1 (6)
B0DT	3V CMOS output, 50 kΩ pull-down	3.0	1 (6)
B0UT	3V CMOS output, 50 kΩ pull-up	3.0	1 (6)
B0WT	3V CMOS output, 5 kΩ pull-up	3.0	1 (6)
B00E	3V CMOS output	6.0	1 (6)
B0DE	3V CMOS output, 50 kΩ pull-down	6.0	1 (6)
B0UE	3V CMOS output, 50 kΩ pull-up	6.0	1 (6)
B0WE	3V CMOS output, 5 kΩ pull-up	6.0	1 (6)
B008	3V CMOS output	9.0	1 (6)
B0D8	3V CMOS output, 50 kΩ pull-down	9.0	1 (6)
B0U8	3V CMOS output, 50 kΩ pull-up	9.0	1 (6)
B0W8	3V CMOS output, 5 kΩ pull-up	9.0	1 (6)
B007	3V CMOS output	12.0	1 (6)
B0D7	3V CMOS output, 50 kΩ pull-down	12.0	1 (6)
B0U7	3V CMOS output, 50 kΩ pull-up	12.0	1 (6)
B0W7	3V CMOS output, 5 kΩ pull-up	12.0	1 (6)
B009	3V CMOS output	18.0	1 (9)
B0D9	3V CMOS output, 50 kΩ pull-down	18.0	1 (9)
B0U9	3V CMOS output, 50 kΩ pull-up	18.0	1 (9)
B0W9	3V CMOS output, 5 kΩ pull-up	18.0	1 (9)
B00H	3V CMOS output	24.0	1 (9)
B0DH	3V CMOS output, 50 kΩ pull-down	24.0	1 (9)
B0UH	3V CMOS output, 50 kΩ pull-up	24.0	1 (9)
B0WH	3V CMOS output, 5 kΩ pull-up	24.0	1 (9)

Note: Number of internal cells required is shown in parentheses.

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
3V CMOS Three-State Output Buffers (Cont.)			
B00J	3V CMOS output	48.0	2 (9)
B0DJ	3V CMOS output, 50 kΩ pull-down	48.0	2 (9)
B0UJ	3V CMOS output, 50 kΩ pull-up	48.0	2 (9)
B0WJ	3V CMOS output, 5 kΩ pull-up	48	2 (9)
3V CMOS Slew-Rate Three-State Output Buffers			
BE07	3V CMOS output	12.0	1 (5)
BED7	3V CMOS output, 50 kΩ pull-down	12.0	1 (5)
BEU7	3V CMOS output, 50 kΩ pull-up	12.0	1 (5)
BEW7	3V CMOS output, 5 kΩ pull-up	12.0	1 (5)
BE09	3V CMOS output	18.0	1 (5)
BED9	3V CMOS output, 50 kΩ pull-down	18.0	1 (5)
BEU9	3V CMOS output, 50 kΩ pull-up	18.0	1 (5)
BEW9	3V CMOS output, 5 kΩ pull-up	18.0	1 (5)
BE0H	3V CMOS output	24.0	1 (5)
BEDH	3V CMOS output, 50 kΩ pull-down	24.0	1 (5)
BEUH	3V CMOS output, 50 kΩ pull-up	24.0	1 (5)
BEWH	3V CMOS output, 5 kΩ pull-up	24.0	1 (5)
BE0J	3V CMOS output	48.0	2 (5)
BEDJ	3V CMOS output, 50 kΩ pull-down	48.0	2 (5)
BEUJ	3V CMOS output, 50 kΩ pull-up	48.0	2 (5)
BEWJ	3V CMOS output, 5 kΩ pull-down	48.0	2 (5)
5V CMOS Three-State Output Buffers			
BV0Q	5V CMOS output	1.0	1 (16)
BVDQ	5V CMOS output, 50 kΩ pull-down	1.0	1 (16)
BV0M	5V CMOS output	2.0	1 (16)
BVDM	5V CMOS output, 50 kΩ pull-down	2.0	1 (16)
BV0T	5V CMOS output	3.0	1 (16)
BVDT	5V CMOS output, 50 kΩ pull-down	3.0	1 (16)
BVOE	5V CMOS output	6.0	1 (16)
BVDE	5V CMOS output, 50 kΩ pull-down	6.0	1 (16)
BV08	5V CMOS output	9.0	1 (19)
BVD8	5V CMOS output, 50 kΩ pull-down	9.0	1 (19)
BV07	5V CMOS output	12.0	2 (19)
BVD7	5V CMOS output, 50 kΩ pull-down	12.0	2 (19)
BV09	5V CMOS output	18.0	2 (19)
BVD9	5V CMOS output, 50 kΩ pull-down	18.0	2 (19)
BV0H	5V CMOS output	24.0	3 (19)
BVDH	5V CMOS output, 50 kΩ pull-down	24.0	3 (19)
5V CMOS Slew-Rate Three-State Output Buffers			
BY07	5V CMOS output	12.0	2 (15)
BYD7	5V CMOS output, 50 kΩ pull-down	12.0	2 (15)
BY09	5V CMOS output	18.0	2 (15)
BYD9	5V CMOS output, 50 kΩ pull-down	18.0	2 (15)
BY0H	5V CMOS output	24.0	3 (15)
BYDH	5V CMOS output, 50 kΩ pull-down	24.0	3 (15)
3V CMOS Open Drain Output Buffers			
EXTH	3V N-ch open drain	3.0	1 (4)
EXUH	3V N-ch open drain, 50 kΩ pull-up	3.0	1 (4)
EXWH	3V N-ch open drain, 5 kΩ pull-up	3.0	1 (4)
EXTJ	3V N-ch open drain	6.0	1 (4)
EXUJ	3V N-ch open drain, 50 kΩ pull-up	6.0	1 (4)
EXWJ	3V N-ch open drain, 5 kΩ pull-up	6.0	1 (4)

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
3V CMOS Open Drain Output Buffers (Cont.)			
EXT1	3V N-ch open drain	9.0	1 (4)
EXT3	3V N-ch open drain, 50 kΩ pull-up	9.0	1 (4)
EXW3	3V N-ch open drain, 5 kΩ pull-up	9.0	1 (4)
EXT9	3V N-ch open drain	12.0	1 (4)
EXTB	3V N-ch open drain, 50 kΩ pull-up	12.0	1 (4)
EXWB	3V N-ch open drain, 5 kΩ pull-up	12.0	1 (4)
EXT5	3V N-ch open drain	18.0	1 (8)
EXT7	3V N-ch open drain, 50 kΩ pull-up	18.0	1 (8)
EXW7	3V N-ch open drain, 5 kΩ pull-up	18.0	1 (8)
EXTD	3V N-ch open drain	24.0	1 (8)
EXTF	3V N-ch open drain, 50 kΩ pull-up	24.0	1 (8)
EXWF	3V N-ch open drain, 5 kΩ pull-up	24.0	1 (8)
EXTL	3V N-ch open drain	48.0	2 (2)
EXUL	3V N-ch open drain, 50 kΩ pull-up	48.0	2 (8)
EXWL	3V N-ch open drain, 5 kΩ pull-up	48.0	2 (8)
EXTQ	3V P-ch open drain	*3.0	1 (4)
EXDQ	3V P-ch open drain, 50 kΩ pull-down	*3.0	1 (4)
EXTR	3V P-ch open drain	*6.0	1 (4)
EXDR	3V P-ch open drain, 50 kΩ pull-down	*6.0	1 (4)
EXT2	3V P-ch open drain	*9.0	1 (4)
EXT4	3V P-ch open drain, 50 kΩ pull-down	*9.0	1 (4)
EXTA	3V P-ch open drain	*12.0	1 (4)
EXTC	3V P-ch open drain, 50 kΩ pull-down	*12.0	1 (4)
EXT6	3V P-ch open drain	*18.0	1 (4)
EXT8	3V P-ch open drain, 50 kΩ pull-down	*18.0	1 (4)
EXTE	3V P-ch open drain	*24.0	1 (8)
EXTG	3V P-ch open drain, 50 kΩ pull-down	*24.0	1 (8)
EXTS	3V P-ch open drain	*48.0	2 (8)
EXDS	3V P-ch open drain, 50 kΩ pull-down	*48.0	2 (8)
3V CMOS Slew-Rate Open Drain Output Buffers			
EET9	3V N-ch open drain	12.0	1 (2)
EETB	3V N-ch open drain, 50 kΩ pull-up	12.0	1 (2)
EEWB	3V N-ch open drain, 50 kΩ pull-up	12.0	1 (2)
EET5	3V N-ch open drain	18.0	1 (2)
EET7	3V N-ch open drain, 50 kΩ pull-up	18.0	1 (2)
EEW7	3V N-ch open drain, 5 kΩ pull-up	18.0	1 (2)
EETD	3V N-ch open drain	24.0	1 (2)
EETF	3V N-ch open drain, 50 kΩ pull-up	24.0	1 (2)
EEWF	3V N-ch open drain, 5 kΩ pull-up	24.0	1 (2)
EETL	3V N-ch open drain	48.0	2 (2)
EEUL	3V N-ch open drain, 50 kΩ pull-up	48.0	2 (2)
EEWL	3V N-ch open drain, 5 kΩ pull-up	48.0	2 (2)
EETA	3V P-ch open drain	*12.0	1 (2)
EETC	3V P-ch open drain, 50 kΩ pull-down	*12.0	1 (2)
EET6	3V P-ch open drain	*18.0	1 (2)
EET8	3V P-ch open drain, 50 kΩ pull-down	*18.0	1 (2)
EETE	3V P-ch open drain	*24.0	1 (2)
EETG	3V P-ch open drain, 50 kΩ pull-down	*24.0	1 (2)
EETS	3V P-ch open drain	*48.0	2 (2)
EEDS	3V P-ch open drain, 50 kΩ pull-down	*48.0	2 (2)

Note: Number of internal cells required is shown in parentheses.
 * Indicates I_{OH}

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
5V CMOS Open Drain Output Buffers			
EVTH	5V N-ch open drain	3.0	1 (4)
EVTJ	5V N-ch open drain	6.0	1 (4)
EVT1	5V N-ch open drain	9.0	1 (8)
EVT9	5V N-ch open drain	12.0	1 (8)
EVT5	5V N-ch open drain	18.0	2 (8)
EVTD	5V N-ch open drain	24.0	2 (8)
5V CMOS Slew-Rate Output Buffers			
EYT9	5V N-ch open drain	12.0	1 (2)
EYT5	5V N-ch open drain	18.0	2 (2)
EYTD	5V N-ch open drain	24.0	2 (2)
3V CMOS Bi-Directional Output Buffers			
B00U	CMOS input, CMOS 3-state output	3.0	1 (9)
B0DU	CMOS input, CMOS 3-state out, 50 kΩ pull-down	3.0	1 (9)
B0UU	CMOS input, CMOS 3-state out, 50 kΩ pull-up	3.0	1 (9)
B0WU	CMOS input, CMOS 3-state out, 5 kΩ pull-up	3.0	1 (9)
B00C	CMOS input, CMOS 3-state output	6.0	1 (9)
B0DC	CMOS input, CMOS 3-state out, 50 kΩ pull-down	6.0	1 (9)
B0UC	CMOS input, CMOS 3-state out, 50 kΩ pull-up	6.0	1 (9)
B0WC	CMOS input, CMOS 3-state out, 5 kΩ pull-up	6.0	1 (9)
B003	CMOS inut, CMOS 3-state output	9.0	1 (8)
B0D3	CMOS input, CMOS 3-state out, 50 kΩ pull-down	9.0	1 (8)
B0U3	CMOS input, CMOS 3-state out, 50 kΩ pull-up	9.0	1 (8)
B0W3	CMOS in, CMOS 3-state out, 5 kΩ pull-up	9.0	1 (8)
B001	CMOS input, CMOS 3-state out	12.0	1 (9)
B0D1	CMOS input, CMOS 3-state out, 50 kΩ pull-down	12.0	1 (9)
B0U1	CMOS input, CMOS 3-state out, 50 kΩ pull-up	12.0	1 (9)
B0W1	CMOS input, CMOS 3-state out, 5 kΩ pull-up	12.0	1 (9)
B005	CMOS input, CMOS 3-state out	18.0	1 (12)
B0D5	CMOS input, CMOS 3-state out, 50 kΩ pull-down	18.0	1 (12)
B0U5	CMOS input, CMOS 3-state out, 50 kΩ pull-up	18.0	1 (12)
B0W5	CMOS input, CMOS 3-state out, 5 kΩ pull-up	18.0	1 (12)
B00F	CMOS input, CMOS 3-state out	24.0	1 (12)
B0DF	CMOS input, CMOS 3-state out, 50 kΩ pull-down	24.0	1 (12)
B0UF	CMOS input, CMOS 3-state out, 50 kΩ pull-up	24.0	1 (12)
B0WF	CMOS input, CMOS 3-state out, 5 kΩ pull-up	24.0	1 (12)
B00W	CMOS input, CMOS 3-state output	48.0	2 (12)
B0DW	CMOS input, CMOS 3-state output, 50 kΩ pull-down	48.0	2 (12)
B0UW	CMOS input, CMOS 3-state out, 50 kΩ pull-up resistor	48.0	2 (12)
B0WW	CMOS input, CMOS 3-state output, 5 kΩ pull-up resistor	48.0	2 (12)
BSIU	CMOS Schmitt input, CMOS 3-state ouput	3.0	1 (14)
BSDU	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	3.0	1 (14)
BSUU	CMOS Schmitt input, CMOS 3-state out, 50 kΩ pull-up	3.0	1 (14)
BSWU	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	3.0	1 (14)
BSIC	CMOS Schmitt input, CMOS 3-state output	6.0	1 (14)
BSDC	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	6.0	1 (14)
BSUC	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	6.0	1 (14)
BSWC	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	6.0	1 (14)

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
3V CMOS Bi-Directional Output Buffers			
BSI3	CMOS Schmitt input, CMOS 3-state output	9.0	1 (14)
BSD3	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	9.0	1 (14)
BSU3	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	9.0	1 (14)
BSW3	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	9.0	1 (14)
3V CMOS Three-State I/O Buffers			
BSI1	CMOS Schmitt input, CMOS 3-state output	12.0	1 (14)
BSD1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	12.0	1 (14)
BSU1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	12.0	1 (14)
BSW1	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	12.0	1 (14)
BSI5	CMOS Schmitt input, CMOS 3-state output	18.0	1 (17)
BSD5	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	18.0	1 (17)
BSU5	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	18.0	1 (17)
BSW5	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	18.0	1 (17)
BSIF	CMOS Schmitt input, CMOS 3-state output	24.0	1 (17)
BSDF	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	24.0	1 (17)
BSUF	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	24.0	1 (17)
BSWF	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	24.0	1 (17)
BSIW	CMOS Schmitt input, CMOS 3-state output	48.0	2 (17)
BSDW	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	48.0	2 (17)
BSUW	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	48.0	2 (17)
BSWW	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	48.0	2 (17)
3V CMOS Slew-Rate Three-State Output Buffers			
BE01	CMOS input, CMOS 3-state output	12.0	1 (8)
BED1	CMOS input, CMOS 3-state output, 50 kΩ pull-dn	12.0	1 (8)
BEU1	CMOS input, CMOS 3-state output, 50 kΩ pull-up	12.0	1 (8)
BEW1	CMOS input, CMOS 3-state output, 5 kΩ pull-up	12.0	1 (8)
BE05	CMOS input, CMOS 3-state output	18.0	1 (8)
BED5	CMOS input, CMOS 3-state output, 50 kΩ pull-dn	18.0	1 (8)
BEU5	CMOS input, CMOS 3-state output, 50 kΩ pull-up	18.0	1 (8)
BEW5	CMOS input, CMOS 3-state output, 5 kΩ pull-up	18.0	1 (8)
BE0F	CMOS input, CMOS 3-state output	24.0	1 (8)
BEDF	CMOS input, CMOS 3-state output, 50 kΩ pull-dn	24.0	1 (8)
BEUF	CMOS input, CMOS 3-state output, 50 kΩ pull-up	24.0	1 (8)
BEWF	CMOS input, CMOS 3-state output, 5 kΩ pull-up	24.0	1 (8)
BE0W	CMOS input, CMOS 3-state output	48.0	2 (8)
BEDW	CMOS input, CMOS 3-state output, 50 kΩ pull-dn	48.0	2 (8)
BEUW	CMOS input, CMOS 3-state output, 50 kΩ pull-up	48.0	2 (8)
BEWW	CMOS input, CMOS 3-state output, 5 kΩ pull-up	48.0	2 (8)

Note: Number of internal cells required is shown in parentheses.

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
3V CMOS Slew-Rate Three-State Output Buffers (Cont.)			
BFI1	CMOS Schmitt input, CMOS 3-state output,	12.0	1 (13)
BFD1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	12.0	1 (13)
BFU1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	12.0	1 (13)
BFW1	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	12.0	1 (13)
BFI5	CMOS Schmitt input, CMOS 3-state output	18.0	1 (13)
BFD5	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	18.0	1 (13)
BFU5	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	18.0	1 (13)
BFW5	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	18.0	1 (13)
BFI1	CMOS Schmitt input, CMOS 3-state output,	24.0	1 (13)
BFD1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	24.0	1 (13)
BFU1	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	24.0	1 (13)
BFW1	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	24.0	1 (13)
BFIW	CMOS Schmitt input, CMOS 3-state output,	48.0	2 (13)
BFDW	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	48.0	2 (13)
BFUW	CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-up	48.0	2 (13)
BFWW	CMOS Schmitt input, CMOS 3-state output, 5 kΩ pull-up	48.0	2 (13)
5V CMOS Bi-Directional Output Buffers			
BW0X	5V CMOS input / CMOS 3-state output	1.0	1 (19)
BWDX	5V CMOS input / CMOS 3-state output, with 50K pull-down	1.0	1 (19)
BW0K	5V CMOS input / CMOS 3-state output	2.0	1 (19)
BWDK	5V CMOS input / CMOS 3-state output, with 50K pull-down	2.0	1 (19)
BW0U	5V CMOS input / CMOS 3-state output	3.0	1 (19)
BWDU	5V CMOS input / CMOS 3-state output, with 50K pull-down	3.0	1 (19)
BW0C	5V CMOS input / CMOS 3-state output	6.0	1 (19)
BWDC	5V CMOS input / CMOS 3-state output, with 50K pull-down	6.0	1 (19)
BW03	5V CMOS input / CMOS 3-state output	9.0	1 (22)
BWD3	5V CMOS input / CMOS 3-state output, with 50K pull-down	9.0	1 (22)
BW01	5V CMOS input / CMOS 3-state output	12.0	2 (22)
BWD1	5V CMOS input / CMOS 3-state output, with 50K pull-down	12.0	2 (22)
BW05	5V CMOS input / CMOS 3-state output	18.0	2 (22)
BWD5	5V CMOS input / CMOS 3-state output, with 50K pull-down	18.0	2 (22)
BW0F	5V CMOS input / CMOS 3-state output,	24.0	3 (22)
BWDF	5V CMOS input / CMOS 3-state output, with 50K pull-down	24.0	3 (22)

Block Name	Description	I _{OL} (mA)	Cells
Interface Blocks (Cont.)			
5V CMOS Bi-Directional Output Buffers (Cont.)			
BKIX	5V CMOS Schmitt input, CMOS 3-state output	1.0	1 (24)
BKDX	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	1.0	1 (24)
BKIK	5V CMOS Schmitt input, CMOS 3-state output	2.0	1 (24)
BKDK	5V CMOS Schmitt input, CMOS 3-state output, 50kΩ pull-down	2.0	1 (24)
BKIU	5V CMOS Schmitt input, CMOS 3-state output	3.0	1 (24)
BKDU	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	3.0	1 (24)
BKIC	5V CMOS Schmitt in, CMOS 3-state output	6.0	1 (24)
BKDC	5V CMOS Schmitt input, CMOS 3-state out, 50 kΩ pull-down resistor	6.0	1 (24)
BKI3	5V CMOS Schmitt input, CMOS 3-state output	9.0	1 (27)
BKD3	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	9.0	1 (24)
BKI1	5V CMOS Schmitt input, CMOS 3-state output	12.0	2 (27)
BKD1	5V CMOS Schmitt input, CMOS 3-state output, 50kΩ pull-down	12.0	2 (27)
BKI5	5V CMOS Schmitt input, CMOS 3-state output	18.0	2 (27)
BKD5	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down resistor	18.0	2 (27)
BKIF	5V CMOS Schmitt input, CMOS 3-state output	24.0	3 (27)
BKDF	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	24.0	3 (27)
5V CMOS Slew-Rate Bi-Directional Output Buffers			
BX01	5V CMOS input / CMOS 3-state output	12.0	2 (18)
BXD1	5V CMOS input / CMOS 3-state output, with 50K pull-down	12.0	2 (18)
BX05	5V CMOS input / CMOS 3-state output	18.0	2 (18)
BXD5	5V CMOS input / CMOS 3-state output, with 50K pull-down	18.0	2 (18)
BX0F	5V CMOS input / CMOS 3-state output	24.0	3 (18)
BXDF	5V CMOS input / CMOS 3-state output, with 50K pull-down	24.0	3 (18)
BZI1	5V CMOS Schmitt input, CMOS 3-state output	12.0	2 (23)
BZD1	5V CMOS Schmitt in, CMOS 3-state output, 50kΩ pull-down	12.0	2 (23)
BZI5	5V CMOS Schmitt input, CMOS 3-state output	18.0	2 (23)
BZD5	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	18.0	2 (23)
BZI1	5V CMOS Schmitt input, CMOS 3-state output	24.0	3 (23)
BZDF	5V CMOS Schmitt input, CMOS 3-state output, 50 kΩ pull-down	24.0	3 (23)

Note: Number of internal cells required is shown in parentheses.

Block Name	Description	Cells
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Interface Blocks

Inverters

F101	Inverter (F/O = 17)	1
F102	Inverter (F/O = 37)	2
F103	Inverter (F/O = 60)	3
F104	Inverter (F/O = 92)	4
F108	Inverter (F/O = 160)	12

Buffers

F111	Non-inverting buffer (F/O = 17)	2
F112	Non-inverting buffer (F/O = 35)	3
F113	Non-inverting buffer (F/O = 54)	4
F114	Non-inverting buffer (F/O = 74)	5
F118	Non-inverting buffer (F/O = 180)	11

NOR Gates

F202	2-input NOR	2
F203	3-input NOR	3
F204	4-input NOR	4
F205	5-input NOR	5
F206	6-input NOR	5
F208	8-input NOR	7
F222	2-input NOR, power	4
F223	3-input NOR, power	6
F224	4-input NOR, power	8

OR Gates

F212	2-input OR	2
F213	3-input OR	3
F214	4-input OR	3
F215	5-input OR	5
F216	6-input OR	5
F232	2-input OR, power	3
F233	3-input OR, power	4
F234	4-input OR, power	4

NAND Gates

F302	2-input NAND	2
F303	3-input NAND	3
F304	4-input NAND	4
F305	5-input NAND	5
F306	6-input NAND	5
F308	8-input NAND	6
F322	2-input NAND, power	4
F323	3-input NAND, power	6
F324	4-input NAND, power	8

AND Gates

F312	2-input AND	2
F313	3-input AND	3
F314	4-input AND	3
F315	5-input AND	5
F316	6-input AND	5
F332	2-input AND, power	3
F333	3-input AND, power	4
F334	4-input AND, power	4

Note: Number of internal cells required is shown in parentheses.

Block Name	Description	Cells
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Function Blocks – Normal Power

AND-NOR Gates

F421	2-wide 1-2-input AND-OR inverter	3
F422	3-wide 1-1-2-input AND-OR inverter	4
F423	2-wide 1-3-input AND-OR inverter	4
F424	2-wide 2-2-input AND-OR inverter	4
F425	3-wide 2-2-2-input AND-OR inverter	6
F426	2-wide 3-3-input AND-OR inverter	6
F429	4-wide 2-2-2-2-input AND-OR inverter	8
F442	2-wide 4-4-input AND-OR inverter	8
F462	3-wide 1-2-3-input AND-OR inverter	6

OR-NAND Gates

F431	2-wide 1-2-input OR-AND inverter	3
F432	3-wide 1-1-2-input OR-AND inverter	4
F433	2-wide 1-3-input OR-AND inverter	4
F434	2-wide 2-2-input OR-AND inverter	4
F435	2-wide 2-3-input OR-AND inverter	5
F436	2-wide 3-3-input OR-AND inverter	6
F454	4-wide 2-2-2-2-input OR-AND inverter	8

Clock Drivers

FKK1	Clock driver (F/O = 360)	40
FKK2	Clock driver (F/O = 720)	80
FKK3	Clock driver (F/O = 1080)	120
FKK4	Clock driver (F/O = 1440)	160
FKK5	Clock driver (F/O = 1800)	200

Exclusive OR Functions

F511	2-input Exclusive-OR	4
F512	2-input Exclusive-NOR	4

Parity Generators

F581	8-bit odd parity generator	19
F582	8-bit even parity generator	19

Adders

F521	1-bit full-adder	9
F523	4-bit binary full-adder	32
F526	Carry look-ahead generator	34
F527	4-bit full-adder	66

Miscellaneous

F091	H, L level generator	1
F093	Interface block for oscillator buffer	1

Three-state Buffers

F531	3-state buffer with enable	5
F532	3-state buffer with active low enable	5

Decoders

F561	2-to-4 decoder	10
F981	2-to-4 decoder with active low enable	13
F982	3-to-8 decoder with active low enable	26

Multiplexers

F569	8-to-1 multiplexer	18
F570	4-to-1 multiplexer	10
F571	2-to-1 multiplexer	6
F572	Quad 2-to-1 multiplexer	14

Block Name	Description	Cells	Block Name	Description	Cells
Function Blocks – Normal Power (Cont.)			Function Blocks – Normal Power (Cont.)		
Latches			Comparator		
F595	R-S latch	5	F985	4-bit magnitude comparator	32
F601	D-latch	6	Scan		
F602	D-latch with reset	6	S000	Scan path D-F/F with set-reset	11
F603	D-latch with reset low	7	S002	Scan path D-F/F	9
F604	D-latch with active low gate (G)	6	S050	Scan path D-F/F with set-reset, hold	14
F605	D-latch with active low gate (G), reset low	7	S052	Scan path D-F/F with hold	12
F901	4-bit D-latch, buffered output	20	S100	Scan path J-K F/F with set-reset	14
F902	8-bit D-latch, buffered output	38	S102	Scan path J-K F/F	12
Flip-Flops			S150	Scan path J-K F/F with set-reset, hold	17
F596	Synchronous R-S F/F with set-reset	11	S152	Scan path J-K F/F with hold	15
F611	D-F/F	8	S201	Scan path D-latch with reset	12
F614	D-F/F with set-reset	10	S202	Scan path D-latch	11
F615	D-F/F with reset low	9	S301	Scan path D-latch with reset	8
F616	D-F/F with set low	9	S302	Scan path D-latch	7
F617	D-F/F with set-reset low	10	S999	Scan path 2-to-1 data selector	4
F631	D-F/F active low clock	8	Delays		
F637	D-F/F active low clock with set-reset low	10	F130	Delay block (for monostable multivibrator)	8
F641	D-F/F, buffered output	8	F131	Delay gate	6
F644	D-F/F with set-reset, buffered output	10	F132	Delay gate	1
F647	D-F/F with set-reset low, buffered output	10	Function Blocks – Low Power		
F661	D-F/F active low clock, buffered output	8	Inverter		
F667	D-F/F active low clock with set-reset low, buffered output	10	L101	Inverter	1
F714	Toggle F/F with set-reset	9	Buffer		
F717	Toggle F/F with set-reset low	9	L111	Non-inverting buffer	1
F737	Toggle low F/F with set-reset low	9	NOR Gates		
F744	Toggle F/F with set-reset, buffered output	9	L202	2-input NOR	1
F747	Toggle F/F with set-reset low, buffered output	9	L203	3-input NOR	2
F767	Toggle active low F/F with set-reset low, buffered output	9	L204	4-input NOR	2
F771	J-K F/F, buffered output	10	OR Gates		
F774	J-K F/F with set-reset, buffered output	12	L212	2-input OR	2
F777	J-K F/F with set-reset low, buffered output	12	L213	3-input OR	2
F781	J-K F/F active low clock, buffered output	10	L214	4-input OR	3
F787	J-K F/F active low clock with set-reset low, buffered output	12	NAND Gates		
F791	Toggle F/F with set-reset and toggle enable	12	L302	2-input NAND	1
F792	Toggle active low F/F with set-reset low and toggle enable low	12	L303	3-input NAND	2
F922	4-bit D-F/F with reset	33	L304	4-input NAND	2
F924	4-bit D-F/F	28	L305	5-input NAND	3
Shift Registers			L306	6-input NAND	3
F911	4-bit shift register with reset	33	AND Gates		
F912	4-bit serial/parallel shift register	35	L312	2-input AND	2
F913	4-bit serial/parallel shift register with reset low	39	L313	3-input AND	2
F914	4-bit shift register	28	L314	4-input AND	3
F915	4-bit shift register w/direct load low, buffered output	44	AND-NOR Gates		
Counters			L421	2-wide 1-2-input AND-OR inverter	2
F961	4-bit synchronous binary up counter with reset low, load low, buffered output	52	L422	3-wide 1-1-2-input AND-OR inverter	2
F962	4-bit synchronous binary up counter with reset low	38	L423	2-wide 1-3-input AND-OR inverter	2
F963	4-bit presettable synchronous up/down binary counter (dual clock with clear)	72	L424	2-wide 2-2-input AND-OR inverter	2
F964	4-bit presettable synchronous up/down binary counter	86			

Block Name	Description	Cells
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Function Blocks – Low Power (Cont.)

AND-NOR Gates

L425	3-wide 2-2-2-input AND-OR inverter	3
L426	2-wide 3-3-input AND-OR inverter	3
L429	4-wide 2-2-2-input AND-OR inverter	4
L442	2-wide 4-4-input AND-OR inverter	4
L462	3-wide 1-2-3-input AND-OR inverter	3

OR-NAND Gates

L431	2-wide 1-2-input OR-AND inverter	2
L432	3-wide 1-1-2-input OR-AND inverter	2
L433	2-wide 1-3-input OR-AND inverter	2
L434	2-wide 2-2-input OR-AND inverter	2
L435	2-wide 2-3-input OR-AND inverter	3
L436	2-wide 3-3-input OR-AND inverter	3
L454	4-wide 2-2-2-input OR-AND inverter	4

Exclusive OR Functions

L511	2-input EX-OR	3
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EX-NOR Gate

L512	2-input EX-NOR	3
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Decoders

L561	2-to-4 decoder	6
L981	2-to-4 decoder with active low enable	8
L982	3-to-8 decoder with active low enable	17

Latches

L601	D-latch	3
L602	D-latch with reset	4
L603	D-latch with reset low	4
L604	D-latch with active low gates (G)	3
L605	D-latch with active low gates (G), reset low	4
L901	4-bit latch	10
L902	8-bit latch	18

Flip-Flops

L611	D-F/F	5
L614	D-F/F with set-reset	7
L617	D-F/F with set-reset low	7
L631	D-F/F with active low clock	5
L637	D-F/F with active low clock, set-reset low	7
L714	Toggle-F/F with set-reset	7
L717	Toggle-F/F with set-reset low	7
L737	Toggle active low F/F with set-reset low	7
L922	4-bit D-F/F with reset	23
L924	4-bit D-F/F	18

Multiplexer

L571	2-to-1 multiplexer	6
L572	Quad 2-to-1 multiplexer	10

Shift Registers

L911	4-bit shift register with reset	23
L912	4-bit serial/parallel shift register	23
L913	4-bit serial/parallel in shift register with reset low	27
L914	4-bit shift register	18

Block	Description	Basic RAM	BIST	Cells
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RAM Memory Blocks

High-Speed Basic RAM Blocks - Hard Macros

KD49	Single-port RAM (32 word x 4 bit)	—	—	574
KD8B	Single-port RAM (64 word x 8 bit)	—	—	1672
KD8F	Single-port RAM (256 word x 8 bit)	—	—	5400
KDAB	Single-port RAM (64 word x 10 bit)	—	—	1976
KDAF	Single-port RAM (256 word x 10 bit)	—	—	6600
KE49	Dual-port RAM (32 word x 4 bit)	—	—	820
KE87	Dual-port RAM (16 word x 8 bit)	—	—	520
KE8B	Dual-port RAM (64 word x 8 bit)	—	—	2128
KE8F	Dual-port RAM (256 word x 8 bit)	—	—	6000
KEAB	Dual-port RAM (64 word x 10 bit)	—	—	2432
KEAF	Dual-port RAM (256 word x 10 bit)	—	—	7200

High-Speed Single Port RAM Blocks - Soft Macros

RJ49	Single-port RAM (32 word x 4 bit)	KD49	RU49	778
RJ4B	Single-port RAM (64 word x 4 bit)	KD49	RU4B	1381
RJ4D	Single-port RAM (128 word x 4 bit)	KD49	RU4D	2556
RJ4F	Single-port RAM (256 word x 4 bit)	KD49	RU4F	4908
RJ89	Single-port RAM (32 word x 8 bit)	KD49	RU89	1384
RJ8B	Single-port RAM (64 word x 8 bit)	KD8B	RU8B	1924
RJ8D	Single-port RAM (128 word x 8 bit)	KD8B	RU8D	3632
RJ8F	Single-port RAM (256 word x 8 bit)	KD8B	RU8F	7009
RJ8H	Single-port RAM (512 word x 8 bit)	KD8B	RU8H	13781
RJAB	Single-port RAM (64 word x 10 bit)	KDAB	RUAB	2246
RJAD	Single-port RAM (128 word x 10 bit)	KDAB	RUAD	4262
RJAF	Single-port RAM (256 word x 10 bit)	KDAB	RUAF	8247
RJAH	Single-port RAM (512 word x 10 bit)	KDAB	RUAH	16249
RJCB	Single-port RAM (32 word x 16 bit)	KD49	RUC9	2602
RJCB	Single-port RAM (64 word x 16 bit)	KD8B	RUCB	3666
RJCD	Single-port RAM (128 word x 16 bit)	KD8B	RUCD	7062
RJCF	Single-port RAM (256 word x 16 bit)	KD8B	RUCF	13789
RJEB	Single-port RAM (64 word x 20 bit)	KDAB	RUEB	4306
RJED	Single-port RAM (128 word x 20 bit)	KDAB	RUED	8318
RJEF	Single-port RAM (256 word x 20 bit)	KDAB	RUEF	16265
RJH9	Single-port RAM (32 word x 32 bit)	KD49	RUH9	5030
RJHB	Single-port RAM (64 word x 32 bit)	KD8B	RUHB	7143
RJHD	Single-port RAM (128 word x 32 bit)	KD8B	RUHD	13915
RJKB	Single-port RAM (64 word x 40 bit)	KDAB	RUKB	8423
RJKD	Single-port RAM (128 word x 40 bit)	KDAB	RUKD	16427

High-Speed Dual Port RAM Blocks - Soft Macros

RK49	Dual-port RAM (32 word x 4 bit)	KE49	RU49	1051
RK4B	Dual-port RAM (64 word x 4 bit)	KE49	RU4B	1910
RK4D	Dual-port RAM (128 word x 4 bit)	KE49	RU4D	3690
RK4F	Dual-port RAM (256 word x 4 bit)	KE49	RU4F	6944
RK87	Dual-port RAM (16 word x 8 bit)	KE87	RU87	
RK89	Dual-port RAM (32 word x 8 bit)	KE49	RU89	1904
RK8B	Dual-port RAM (64 word x 8 bit)	KE8B	RU8B	2413
RK8D	Dual-port RAM (128 word x 8 bit)	KE8B	RU8D	4587
RK8F	Dual-port RAM (256 word x 8 bit)	KE8F	RU8F	8887
RK8H	Dual-port RAM (512 word x 8 bit)	KE8F	RU8H	17501
RKAB	Dual-port RAM (64 word x 10 bit)	KEAB	RUAB	2733
RKAD	Dual-port RAM (128 word x 10 bit)	KEAB	RUAD	5215
RKAF	Dual-port RAM (256 word x 10 bit)	KEAF	RUAF	10125
RKAH	Dual-port RAM (512 word x 10 bit)	KEAF	RUAH	19969

Block	Description	Basic RAM	BIST	Cells	Block	Description	Cells
Memory Blocks (Cont.)					ROM Memory Blocks		
High-Speed RAM Blocks - Soft Macros (Cont.)					ROM Blocks		
RKC9	Dual-port RAM (32 word x 16 bit)	KE49	RUC9	3612	J14D	128 word x 4 bit ROM	720
RKCB	Dual-port RAM (64 word x 16 bit)	KE8B	RUCB	4609	J14F	256 word x 4 bit ROM	1040
RKCD	Dual-port RAM (128 word x 16 bit)	KE8B	RUCD	8927	J14H	512 word x 4 bit ROM	1512
RKCF	Dual-port RAM (256 word x 16 bit)	KE8F	RUCF	17491	J14M	1K word x 4 bit ROM	2408
RKEB	Dual-port RAM (64 word x 20 bit)	KEAB	RUEB	5249	J14S	2K word x 4 bit ROM	3960
RKED	Dual-port RAM (128 word x 20 bit)	KEAB	RUED	10183	J14U	4K word x 4 bit ROM	6776
RKEF	Dual-port RAM (256 word x 20 bit)	KE49	RUH9	19968	J18D	128 word x 8 bit ROM	1040
RKH9	Dual-port RAM (32 word x 32 bit)	KE8B	RUHB	7025	J18F	256 word x 8 bit ROM	1456
RKHB	Dual-port RAM (64 word x 32 bit)	KE8B	RUHD	8998	J18H	512 word x 8 bit ROM	2352
RKHD	Dual-port RAM (128 word x 32 bit)	KE8B	RUHD	17604	J18M	1K word x 8 bit ROM	3784
RKKB	Dual-port RAM (64 word x 40 bit)	KEAB	RUKB	10278	J18S	2K word x 8 bit ROM	6600
RKKD	Dual-port RAM (128 word x 40 bit)	KEAB	RUKD	20116	J18U	4K word x 8 bit ROM	11704
High-Density Single-Port RAM Blocks - Soft Macros					J18W	8K word x 8 bit ROM	21584
RB4D	Single-port RAM (128 word x 4 bit)	K14D	RU4D	1316	J1CD	128 word x 16 bit ROM	1456
RB4F	Single-port RAM (256 word x 4 bit)	K14D	RU4F	2623	J1CF	256 word x 16 bit ROM	2352
RB4H	Single-port RAM (512 word x 4 bit)	K14D	RU4H	5210	J1CH	512 word x 16 bit ROM	3696
RB4M	Single-port RAM (1K word x 4 bit)	K14D	RU4M	8926	J1CM	1K word x 16 bit ROM	6512
RB4S	Single-port RAM (2K word x 4 bit)	K14D	RU4S	17754	J1CS	2K word x 16 bit ROM	11400
RB4U	Single-port RAM (4K word x 4 bit)	K14D	RU4U	35172	J1CU	4K word x 16 bit ROM	21280
RB8D	Single-port RAM (128 word x 8 bit)	K14D	RU8D	2472	J1HF	256 word x 32 bit ROM	3696
RB8F	Single-port RAM (256 word x 8 bit)	K18F	RU8F	3978	J1HH	512 word x 32 bit ROM	6512
RB8H	Single-port RAM (512 word x 8 bit)	K18F	RU8H	7711	J1HM	1K word x 32 bit ROM	11248
RB8M	Single-port RAM (1K word x 8 bit)	K18M	RU8M	12522	J1HS	2K word x 32 bit ROM	21128
RB8S	Single-port RAM (2K word x 8 bit)	K18M	RU8S	24776	RAM Blocks (BIST)		
RBAF	Single-port RAM (256 word x 10 bit)	K1AF	RUAF	4897	RU49	32 word x 4 bit	
RBAH	Single-port RAM (512 word x 10 bit)	K1AF	RUAH	9495	RU4B	64 word x 4 bit	
RBAM	Single-port RAM (1K word x 10 bit)	K1AM	RUAM	15499	RU4D	128 word x 4 bit	
RBAS	Single-port RAM (2K word x 10 bit)	K1AM	RUAS	30710	RU4F	256 word x 4 bit	
RBCD	Single-port RAM (128 word x 16 bit)	K14D	RUCD	4657	RU87	16 word x 8 bit	
RBCF	Single-port RAM (256 word x 16 bit)	K18F	RUCF	7744	RU89	32 word x 8 bit	
RBCH	Single-port RAM (512 word x 16 bit)	K18F	RUCH	15188	RU8B	64 word x 8 bit	
RBCM	Single-port RAM (1K word x 16 bit)	K18M	RUCM	24801	RU8D	128 word x 8 bit	
RBEF	Single-port RAM (256 word x 20 bit)	K1AF	RUEF	9539	RU8F	256 word x 8 bit	
RBEH	Single-port RAM (512 word x 20 bit)	K1AF	RUEH	18756	RU8H	512 word x 8 bit	
RBEM	Single-port RAM (1K word x 20 bit)	K1AM	RUHM	30754	RUAB	64 word x 10 bit	
RBHD	Single-port RAM (128 word x 32 bit)	K14D	RUHD	9109	RUAD	128 word x 10 bit	
RBHF	Single-port RAM (256 word x 32 bit)	K18F	RUHF	15268	RUAF	256 word x 10 bit	
RBHH	Single-port RAM (512 word x 32 bit)	K18F	RUHH	30137	RUAH	512 word x 10 bit	
RBKF	Single-port RAM (256 word x 40 bit)	K1AF	RUKF	18861	RUC9	32 word x 16 bit	
RBKH	Single-port RAM (512 word x 40 bit)	K1AF	RUKH	37273	RUCB	64 word x 16 bit	
					RUCD	128 word x 16 bit	
					RUCF	256 word x 16 bit	
					RUEB	64 word x 20 bit	
					RUED	128 word x 20 bit	
					RUEF	256 word x 20 bit	
					RUH9	32 word x 32 bit	
					RUHB	64 word x 32 bit	
					RUHD	128 word x 32 bit	
					RUKB	64 word x 40 bit	
					RUKD	128 word x 40 bit	

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