

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

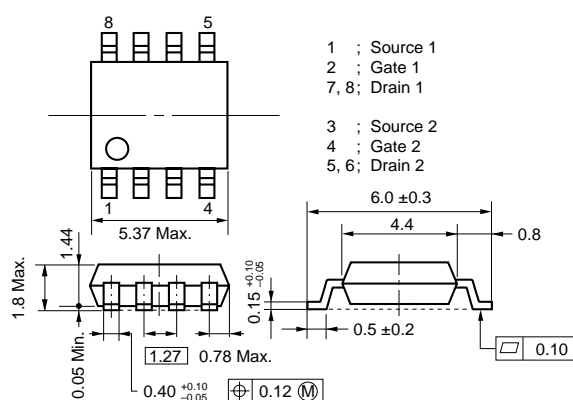
DESCRIPTION

This product is Dual N-Channel MOS Field Effect Transistor designed for power management application of notebook computers, and Li-ion battery application.

FEATURES

- Dual MOS FET chips in small package
- 2.5 V gate drive type low on-state resistance
 $R_{DS(on)1} = 30 \text{ m}\Omega$ (MAX.) ($V_{GS} = 4.5 \text{ V}$, $I_D = 3.0 \text{ A}$)
 $R_{DS(on)2} = 40 \text{ m}\Omega$ (MAX.) ($V_{GS} = 2.5 \text{ V}$, $I_D = 3.0 \text{ A}$)
- Low C_{iss} : $C_{iss} = 1100 \text{ pF}$ (TYP.)
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



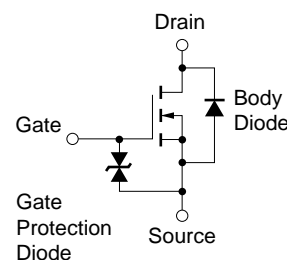
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1758G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0$)	V_{GSS}	±12.0	V
Drain Current (DC)	$I_{D(DC)}$	±6.0	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	±24	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to + 150	$^\circ\text{C}$

EQUIVALENT CIRCUIT



- Notes**
1. $PW \leq 10 \text{ }\mu\text{s}$, Duty cycle $\leq 1 \%$
 2. Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 1.1 \text{ mm}$

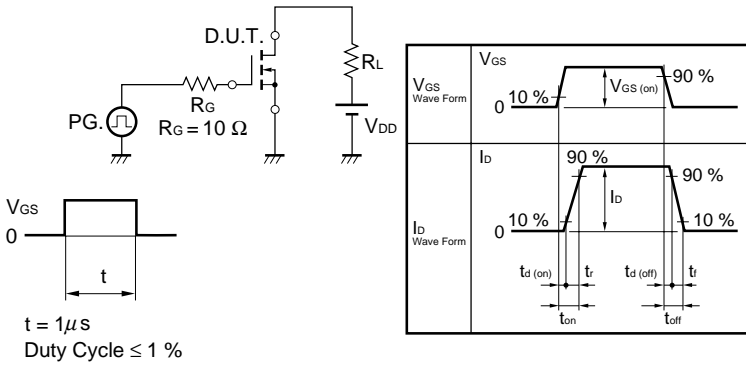
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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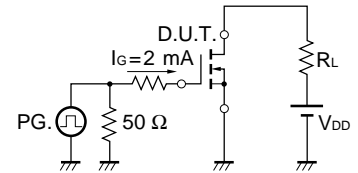
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 4.5 V, I _D = 3.5 A		20	30	mΩ
	R _{DS(on)2}	V _{GS} = 2.5 V, I _D = 3.5 A		25	40	mΩ
Gate to Source Cutoff Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1.0 mA	0.5	0.8	1.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	5.0	13		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±12.0 V, V _{DS} = 0			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz		1100		pF
Output Capacitance	C _{oss}			370		pF
Reverse Transfer Capacitance	C _{rss}			170		pF
Turn-on Delay Time	t _{d(on)}	I _D = 3.0 A, V _{GS(on)} = 4.0 V, V _{DD} = 15 V R _G = 10 Ω		50		ns
Rise Time	t _r			190		ns
Turn-off Delay Time	t _{d(off)}			550		ns
Fall Time	t _f			490		ns
Total Gate Charge	Q _G	I _D = 6.0 A, V _{DD} = 24 V, V _{GS} = 4.0 V		15.0		nC
Gate to Source Charge	Q _{GS}			2.0		nC
Gate to Drain Charge	Q _{GD}			6.5		nC
Body Diode forward Voltage	V _{F(S-D)}	I _F = 6.0 A, V _{GS} = 0		0.8		V

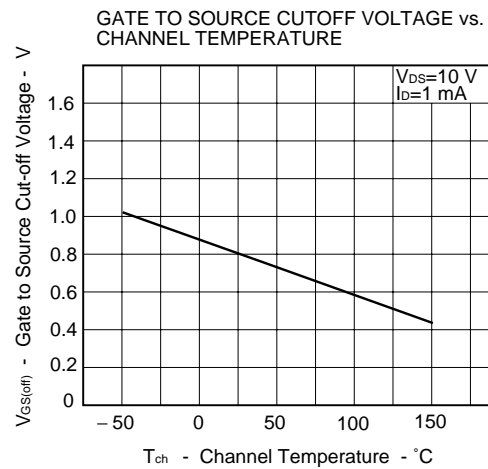
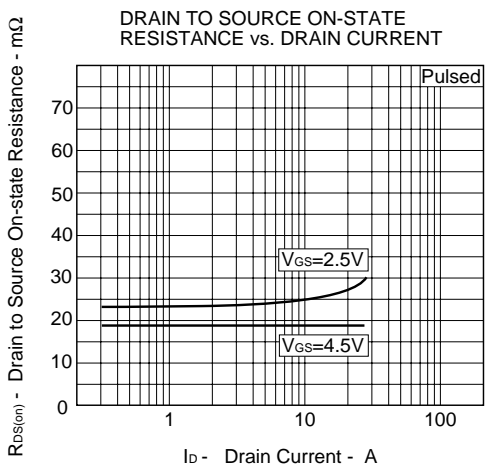
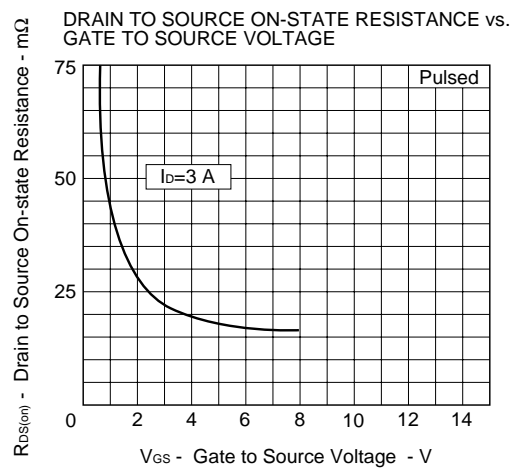
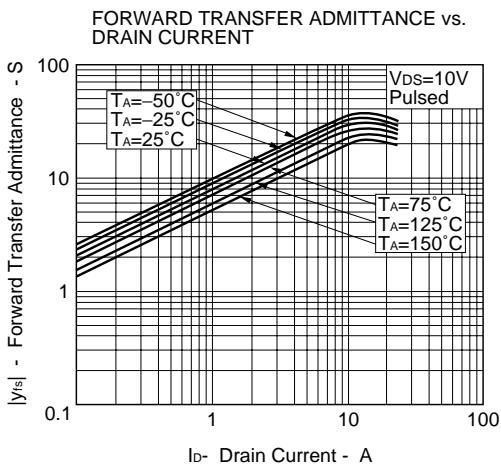
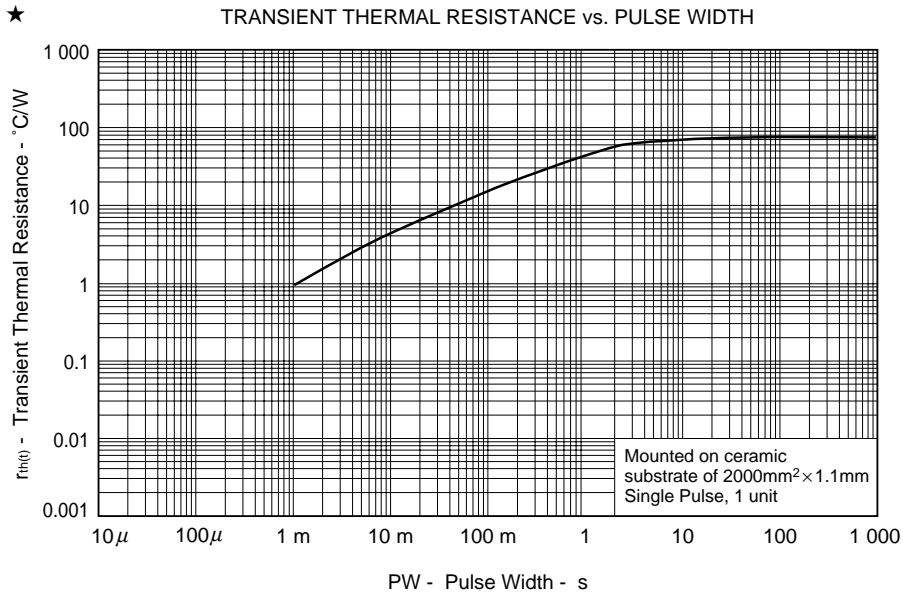
TEST CIRCUIT 1 SWITCHING TIME

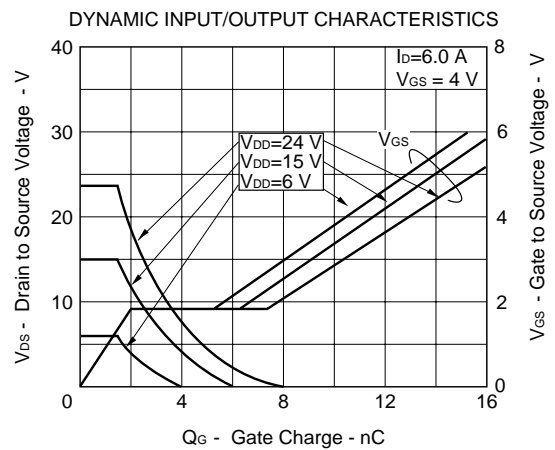
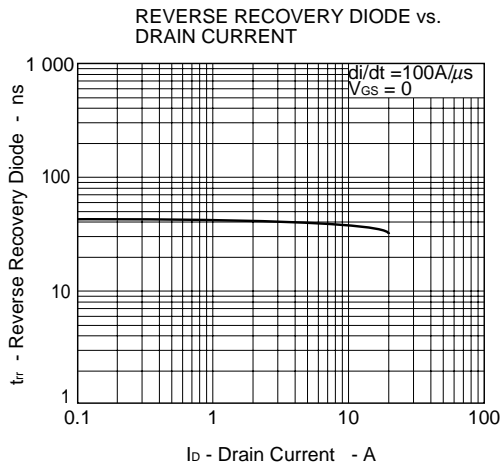
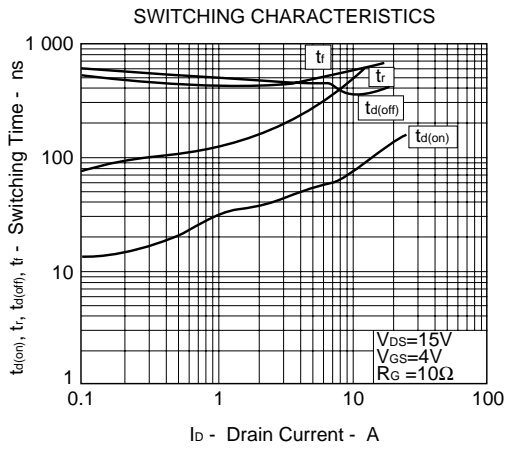
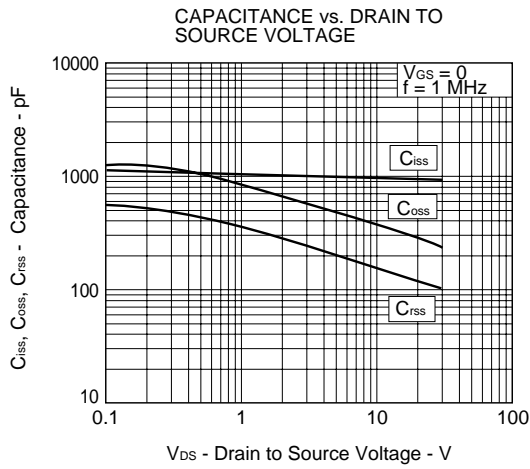
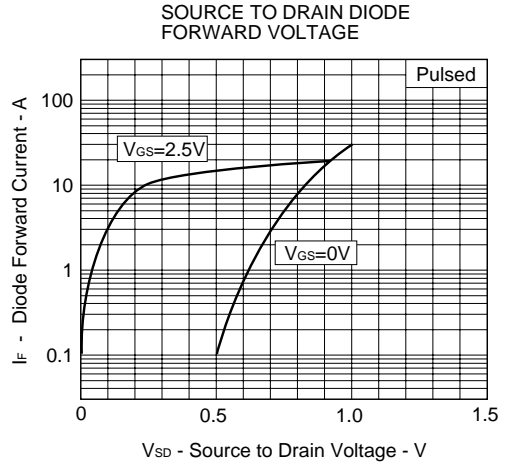
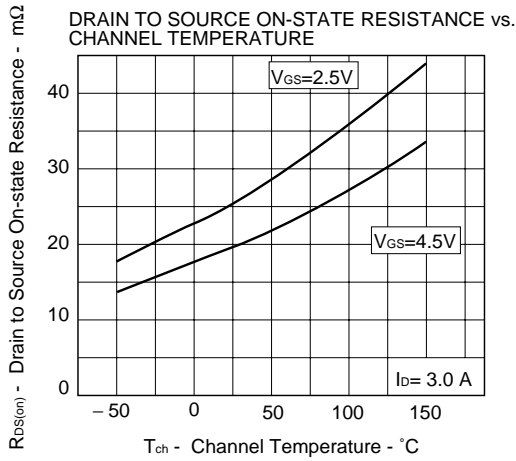


TEST CIRCUIT 2 GATE CHARGE

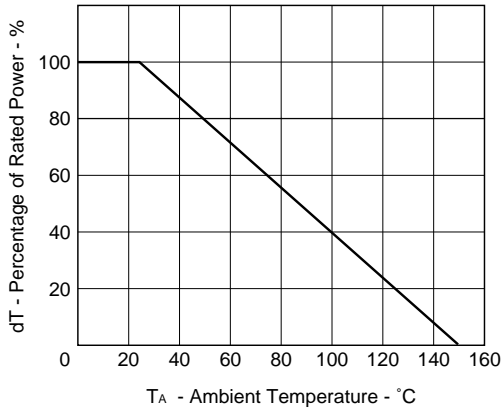


TYPICAL CHARACTERISTICS (T_A = 25 °C)

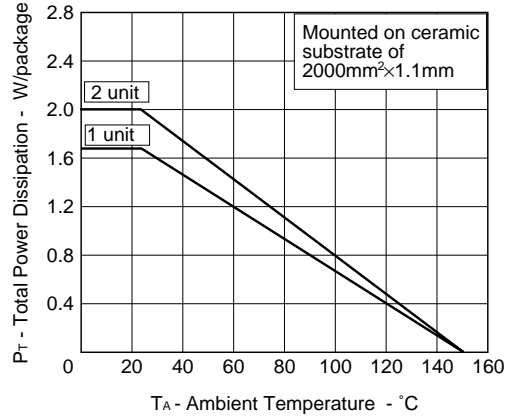




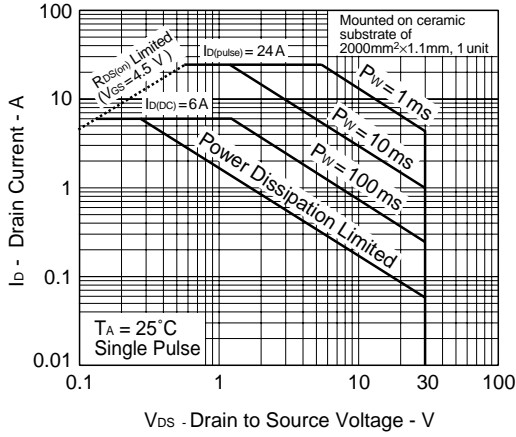
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



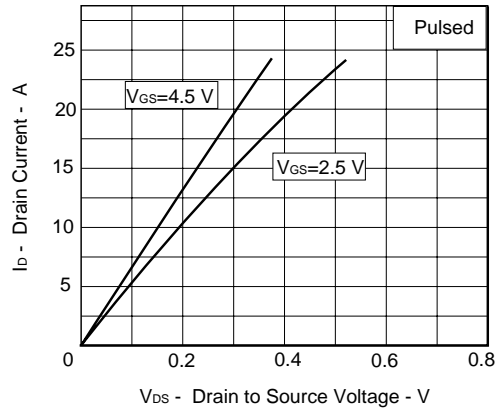
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



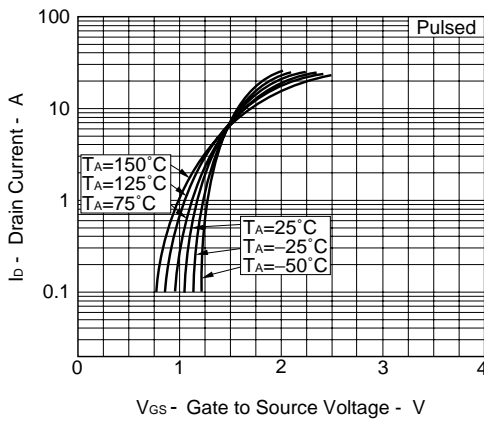
★ FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



FORWARD TRANSFER CHARACTERISTICS



[MEMO]

[MEMO]

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