Toshiba Bipolar Linear Integrated Circuit Silicon Monolithic

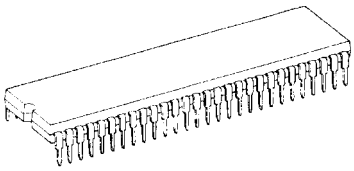
TA1316AN

YCbCr/YPbPr Signal and Sync Processor for Digital TV, Progressive Scan TV and Double Scan TV

TA1316AN is a component signal and sync processor for Digital TV, Progressive scan TV and Double scan TV.

TA1316AN provides high performance signal processors in the luminance and color difference blocks. The sync circuit can process 525I/P, 625I/P, 750P, 1125I/P, PAL100 Hz and NTSC120 Hz formats.

TA1316AN provides I²C bus interface, so various functions and controls are adjustable via the bus.



SDIP56-P-600-1.78

Weight: 5.55 g (typ.)

Features

Luminance Block

- Black stretch, DC restoration
- Dynamic γ correction
- SRT (LTI)
- Y group delay correction (shoot balance correction)
- APACON white peak limit
- White pulse limit (white letter improvement)
- Hi-bright color
- Color detail enhancer (CDE)
- VSM output

Color Difference Block

- Flesh color correction
- Dynamic Y/C correction
- Color SRT (CTI)
- Color γ
- White peak blue correction

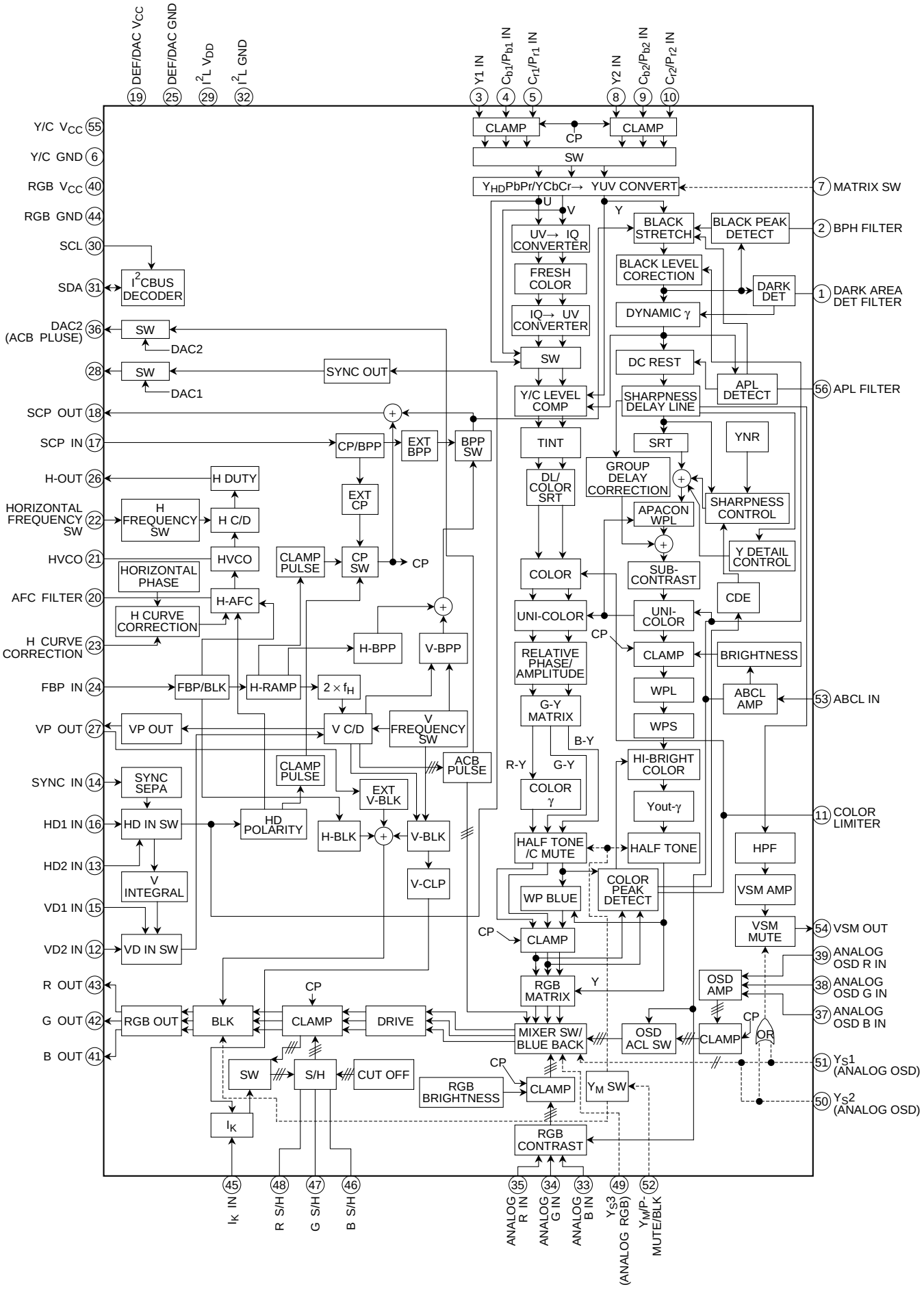
Text Block

- OSD blending SW
- ACB (only black level)
- 2 analog RGB inputs

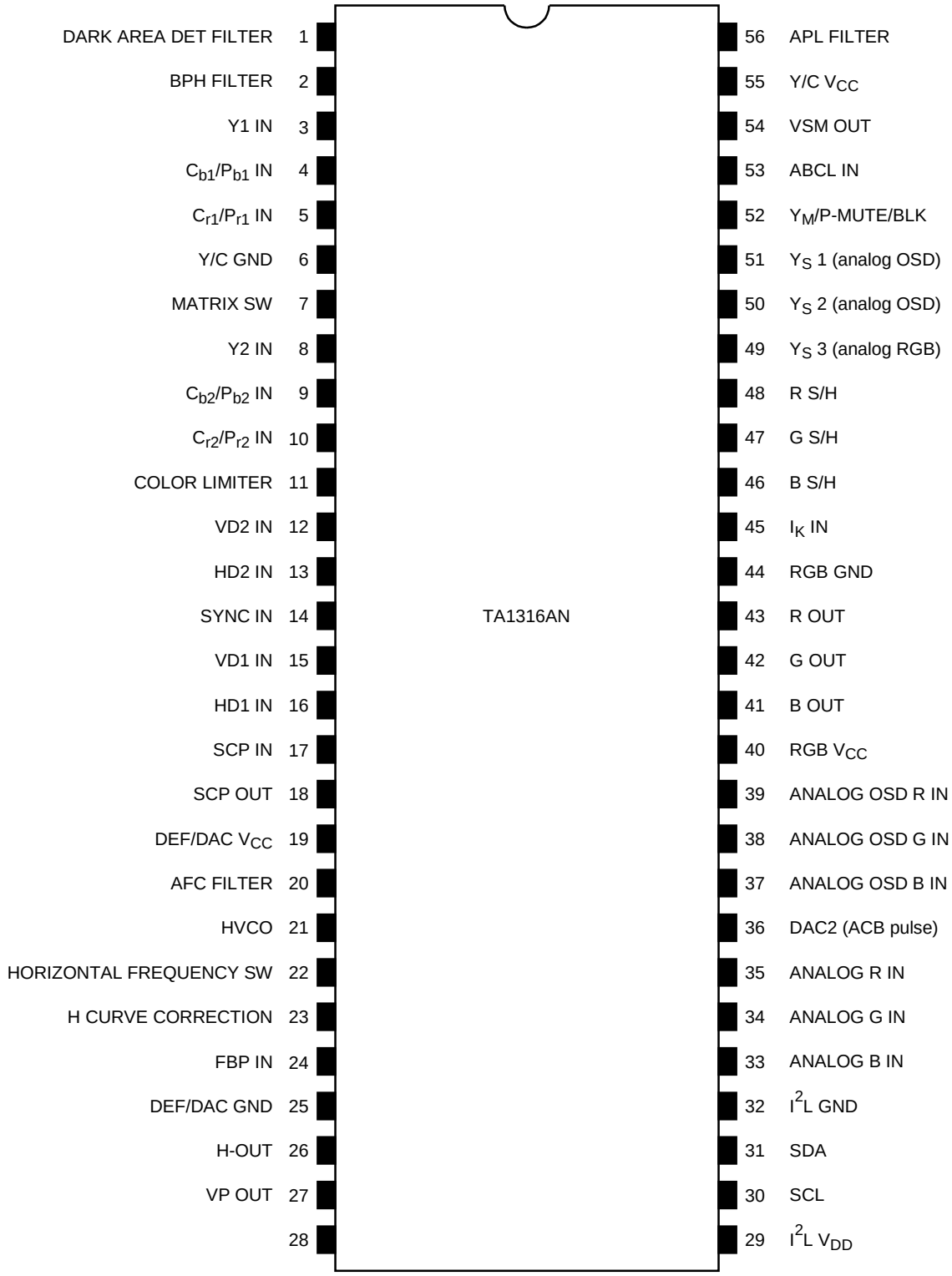
Synchronization Block

- Horizontal synchronization
  (15.75 kHz, 31.5 kHz, 33.75 kHz, 45 kHz)
- Vertical synchronization
  (525I/P, 625I/P, 750P, 1125I/P, PAL 100 Hz, NTSC 120 Hz)
- 2-and 3-level sync. separation circuit
- Accept both positive and negative HD/VD input
- Mask for copy-guard signal
- Vertical blanking

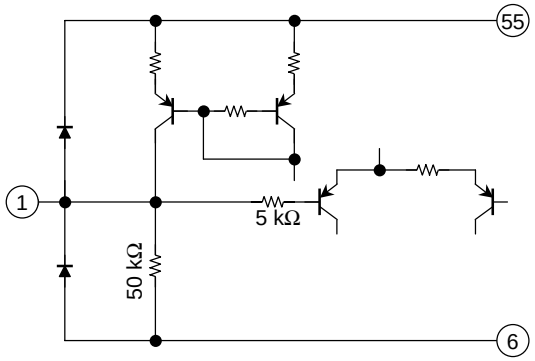
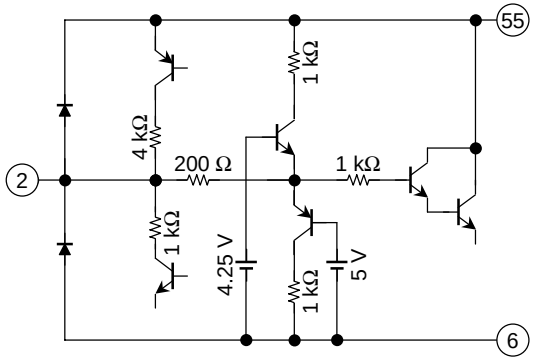
Block Diagram

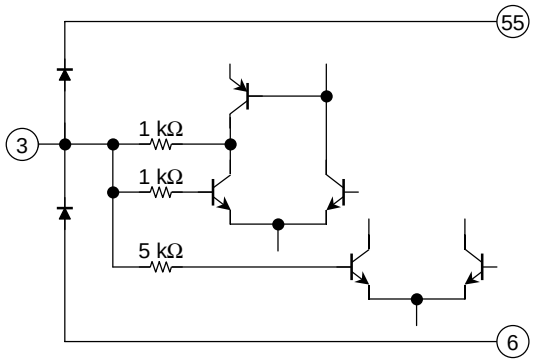
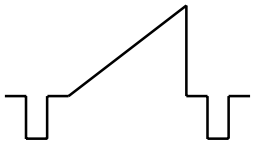
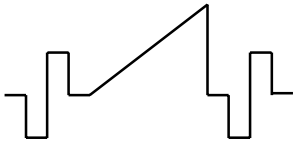
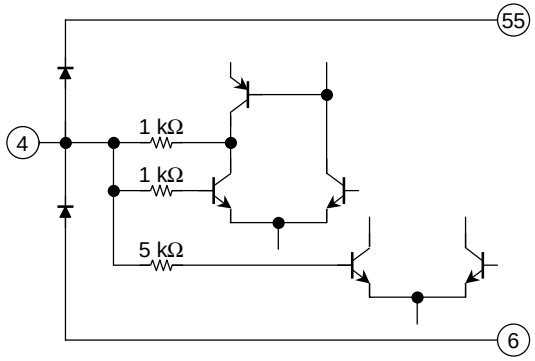


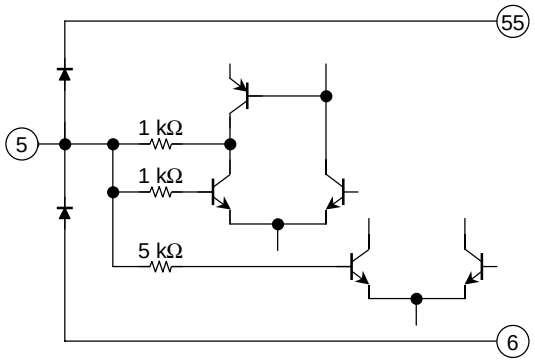
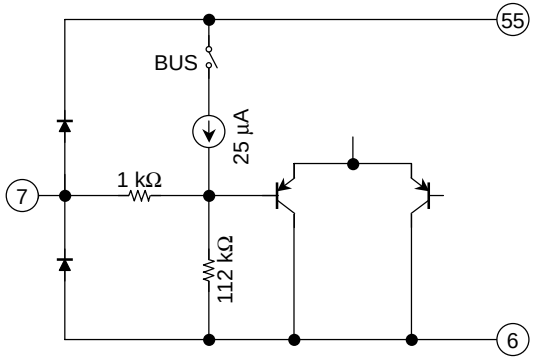
Pin Assignment

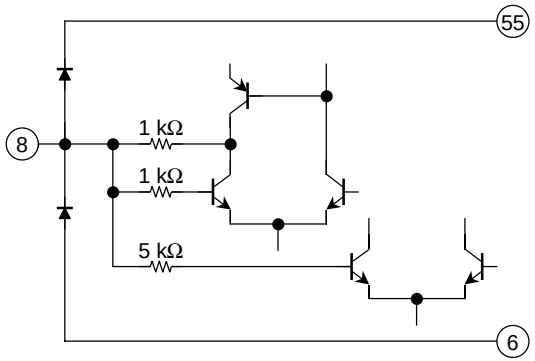
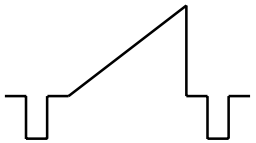
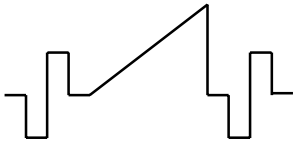
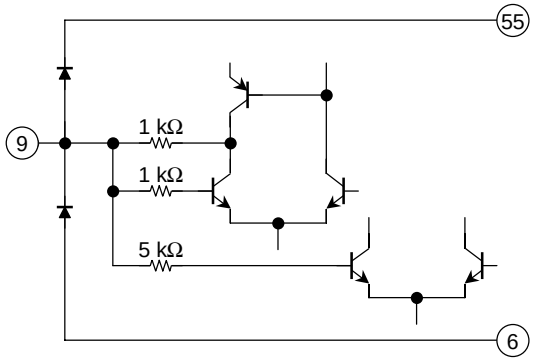


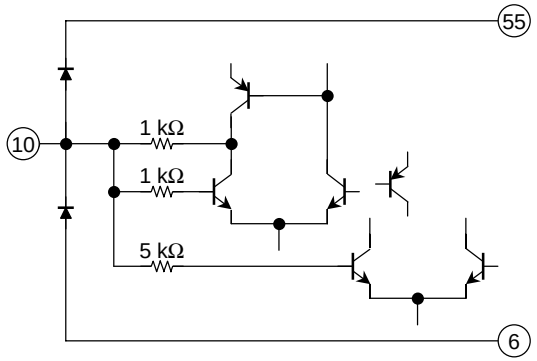
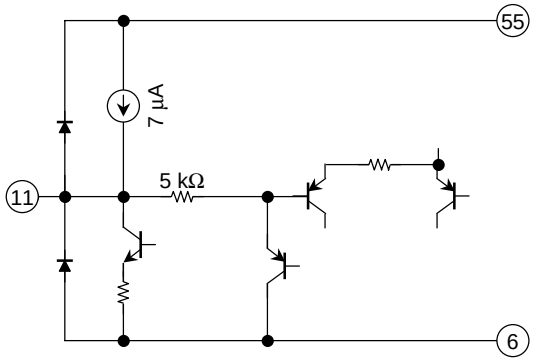
Pin Functions

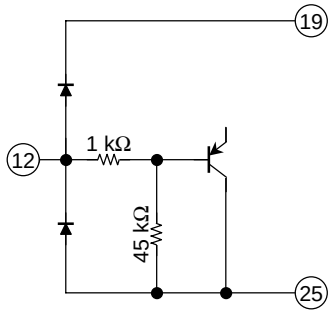
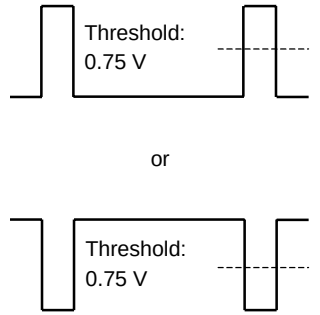
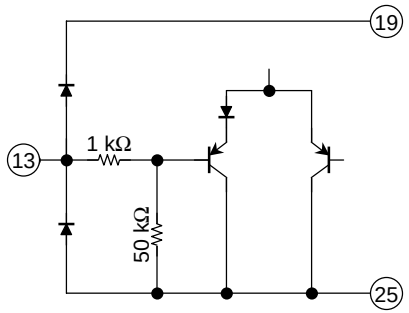
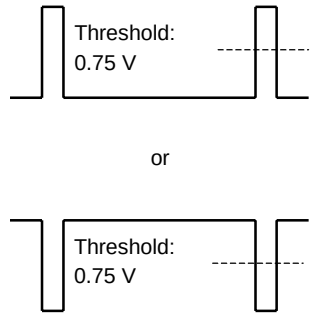
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
1	DARK AREA DET FILTER	Connect filter for detecting black area. Voltage value of this pin controls dynamic γ circuit gain.		DC
2	BPH FILTER	Connect filter for detecting black peak. Voltage value of this pin controls black stretch gain.		DC

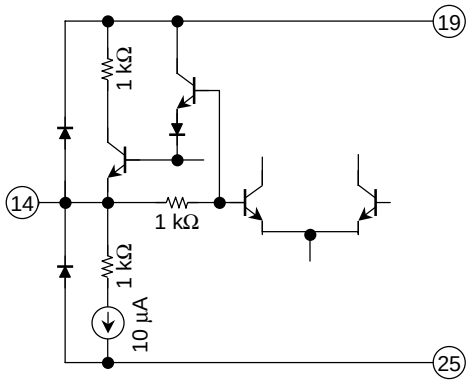
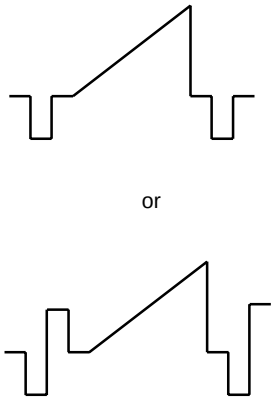
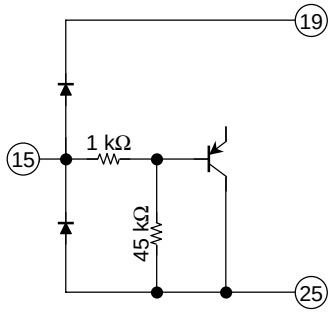
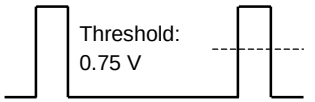
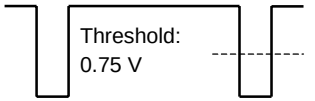
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
3	Y1 IN	Inputs Y1 signal via clamp capacitor. Recommended input amplitude: 1 V_{p-p} (including sync) at 100% color bar.		1 V_{p-p} (including sync) at 100% color bar  or 
4	C_{b1}/P_{b1} IN	Inputs C_{b1}/P_{b1} signal via clamp capacitor. Recommended input amplitude: 700 mV_{p-p} at 100% color bar.		700 mV_{p-p} at 100% color bar for C_{b1}/P_{b1}

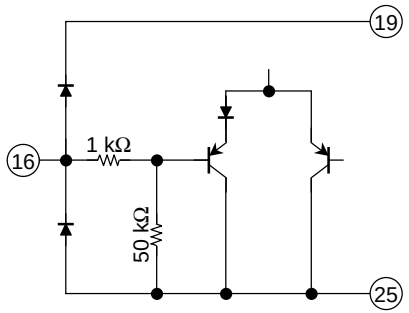
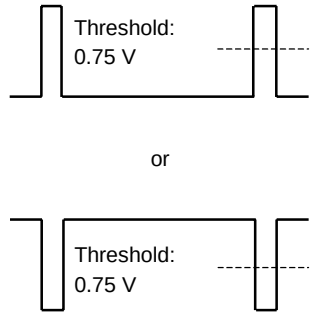
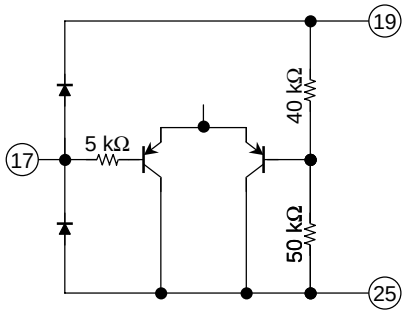
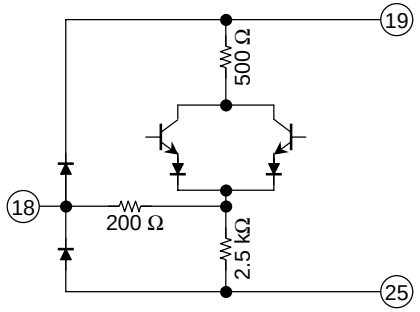
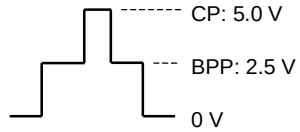
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
5	C_{r1}/P_{r1} IN	Inputs C_{r1}/P_{r1} signal via clamp capacitor. Recommended input amplitude: 700 mV_{p-p} at 100% color bar.		100 mV_{p-p} at 100% color bar for C_{r1}/P_{r1}
6	Y/C GND	GND pin for Y/C block.	—	—
7	MATRIX SW	Matrix switching pin for YCbCr or YPbPr input. Switches matrix according to voltage value input to this pin when BUS control "YUV INPUT MODE" = 00 or 01. Then, control by pin has priority over control by BUS (see table 4). When pin is not used, connect 0.01 μF capacitor between pin and GND.		When YUV INPUT MODE = 00 or 01, 0~0.6 V: YCbCr → Internal YUV 0.9~5 V: YPbPr → Internal YUV Open: BUS control

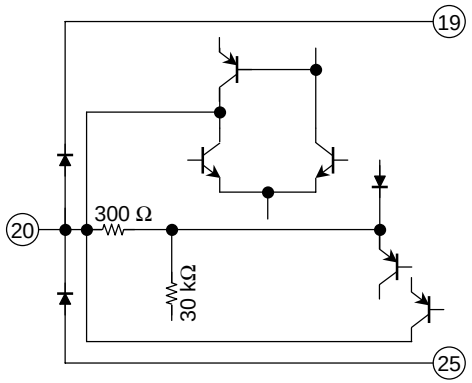
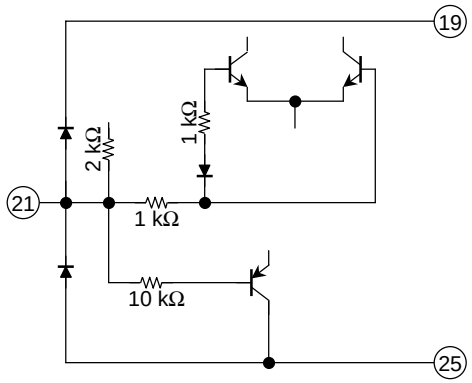
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
8	Y2 IN	Inputs Y2 signal via clamp capacitor. Recommended input amplitude: 1 V_{p-p} (including sync) at 100% color bar.		1 V_{p-p} (including sync) at 100% color bar  or 
9	Cb2/Pb2 IN	Inputs C_{b2}/P_{b2} signal via clamp capacitor. Recommended input amplitude: 700 mV_{p-p} at 100% color bar.		700 mV_{p-p} at 100% color bar for C_{b2}/P_{b2}

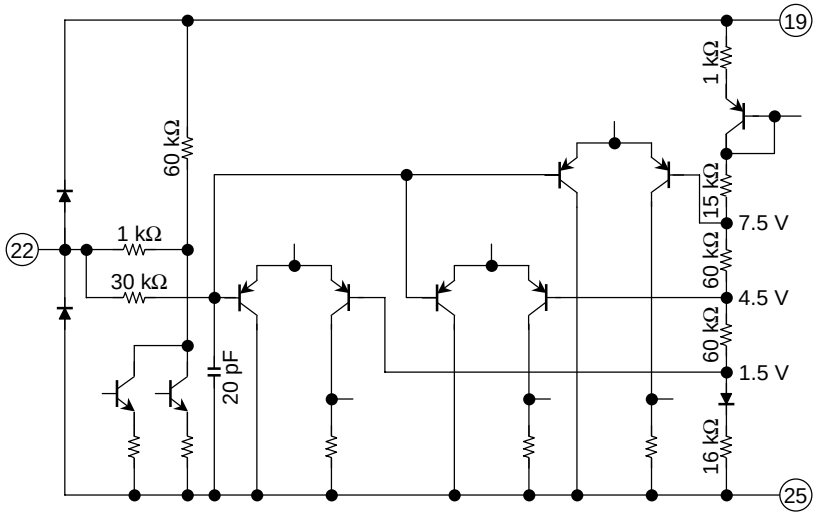
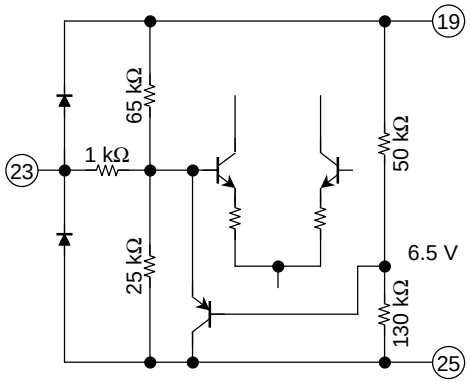
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
10	C_{r2}/P_{r2} IN	Inputs C_{r2}/P_{r2} signal via clamp capacitor. Recommended input amplitude: 700 mV_{p-p} at 100% color bar.		700 mV_{p-p} at 100% color bar for C_{r2}/P_{r2}
11	COLOR LIMITER	Connect filter for detecting color limit.		DC

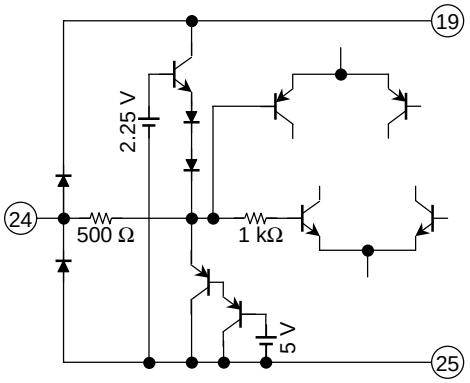
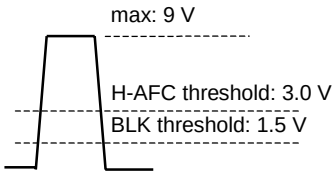
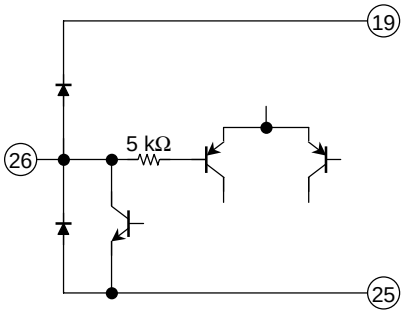
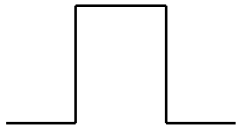
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
12	VD2 IN	Inputs vertical sync signal VD2. Signal input can have both positive and negative polarity.		
13	HD2 IN	Inputs horizontal sync signal HD2. Signal input can have both positive and negative polarity.		

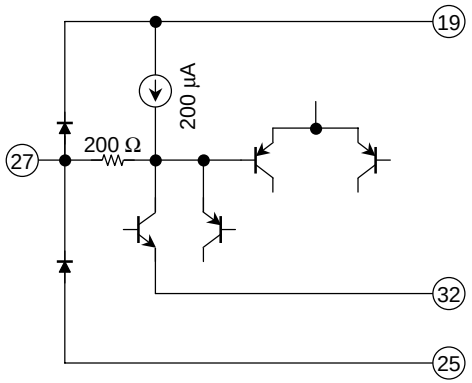
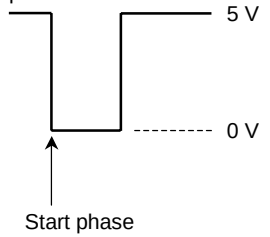
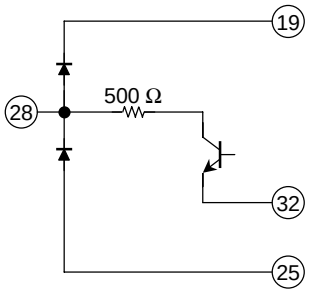
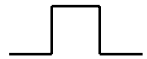
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
14	SYNC IN	Inputs sync signal via clamp capacitor.		White 100%: 1 V_{p-p}  or
15	VD1 IN	Inputs vertical sync signal VD1. Signal input can have both positive and negative polarity.		 or 

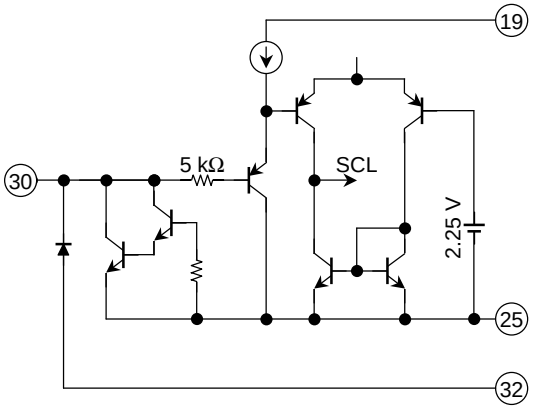
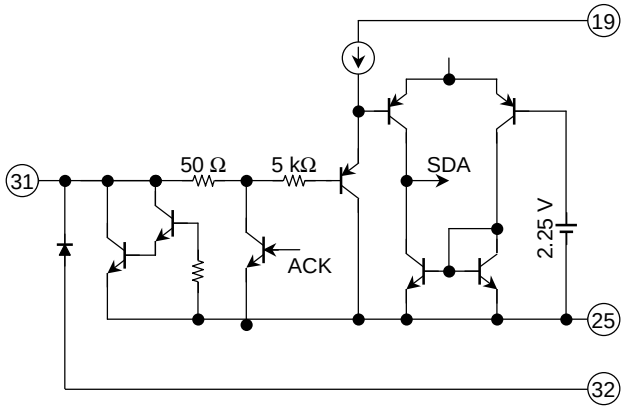
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
16	HD1 IN	Inputs horizontal sync signal HD1. Input signal can have both positive and negative polarity.		
17	SCP IN	Inputs SCP from up converter. Input signals are clamp pulse (CP) and black peak detection stop pulse (BPP).		2.2 V~2.8 V: BPP 4.7 V~9 V: CP
18	SCP OUT	Outputs SCP. Output signals are clamp pulse (CP) and black peak detection stop pulse (BPP). (Note) Don't use Horizontal-BPP (H-BPP) for the timing pulse of picture period on the screen (e.g. H-BLK) because H-BPP width will be changed by the temperature.		

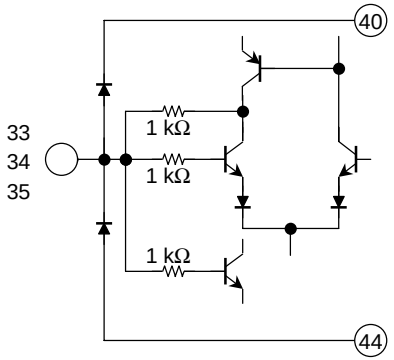
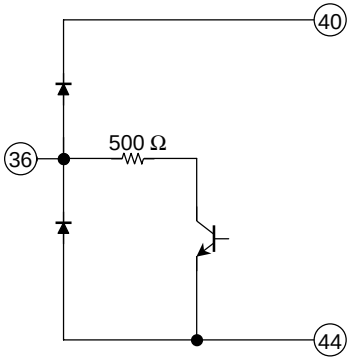
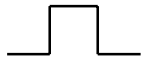
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
19	DEF/DAC V_{CC}	V_{CC} pin for DEF/DAC block. To ascertain the correct voltage for V_{CC}, please refer to the table entitled Maximum Ratings.	—	—
20	AFC FILTER	Connect filter for detecting AFC.		DC
21	HVCO	Connect ceramic oscillator for horizontal oscillation. Use Murata CSBLA503KECZF30 oscillator.		—

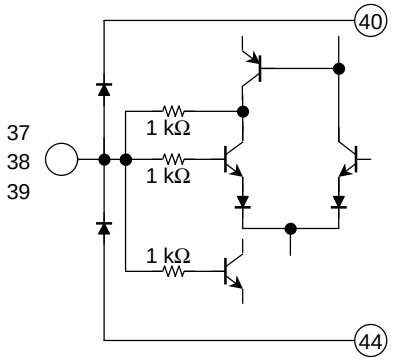
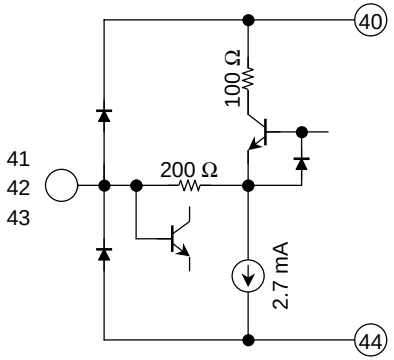
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
22	HORIZONTAL FREQUENCY SW	Horizontal frequency select pin. Selects horizontal frequency according to voltage value input to this pin. When selecting horizontal frequency by BUS control, leave pin open. Control by pin has priority over control by BUS. When this IC will be used on CRT, the frequency of H-out (pin 26) should be controlled by DC voltage which is divided from voltage of DEF V_{CC} (pin 19) by resisters.		At BUS control (horizontal frequency): output voltage value 00 (15.75 kHz): DC 9 V 01 (31.5 kHz): DC 6 V 10 (33.75 kHz): DC 3 V 11 (45 kHz): DC 0 V At pin 22 control, horizontal frequency and input voltage value 0~1.0 V: 45 kHz 2.0~4.0 V: 33.75 kHz 5.0~7.0 V: 31.5 kHz 8.0~9.0 V: 15.75 kHz
23	H CURVE CORRECTION	Corrects curve at high-tension fluctuation. Input AC component of high-tension fluctuation. When pin is not used, connect 0.01 μF capacitor between pin and GND.		DC

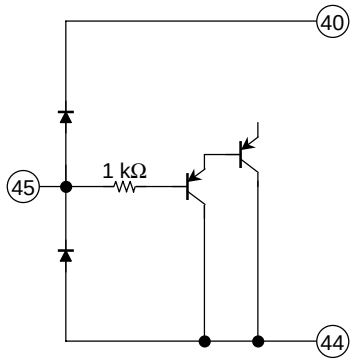
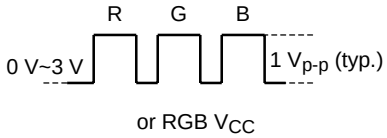
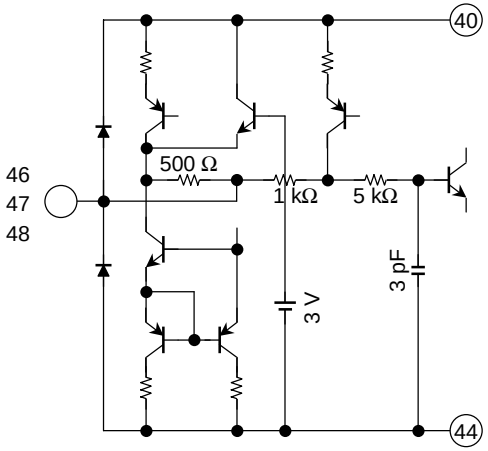
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
24	FBP IN	Input FBP and H-BLK for horizontal AFC.		
25	DEF/DAC GND	GND pin for DEF/DAC block.	—	—
26	H-OUT	Horizontal output pin. Open collector output.		

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
27	VP OUT	Outputs vertical pulse. When a current is applied to the pin, external blanking is carried out by ORing this signal with the internal blanking signal. (Note) When H-POSITION will be changed, VP width will change. Use the start phase of VP.		VP output:  V-BLK input current: 780 µA~1 mA
28	DAC1 (SYNC OUT)	Outputs 1-bit DAC or composite SYNC signal after sync separation. Open-collector output (The output level for this pin cannot be guaranteed since leakage from internal signals may occur.)		DC or SYNC OUT 
29	I^2L V_{DD}	V_{DD} pin for I^2L block. Connect 2 V (typ.). Power to pin 29 should be supplied from pin 19 via zener diode through resister.	—	—

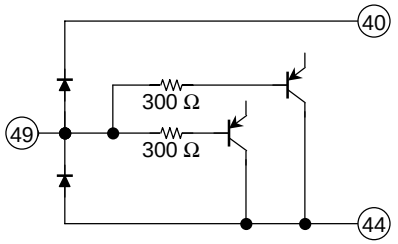
Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
30	SCL	SCL pin for I^2C BUS.		—
31	SDA	SDA pin for I^2C BUS.		—
32	I^2L GND	GND pin for I^2L block.	—	—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
33 34 35	ANALOG B IN ANALOG G IN ANALOG R IN	Inputs analog R/G/B signal via clamp capacitor. Recommended input amplitude: 0.7 V_{p-p} (no sync) at 100% white		100 IRE: 0.7 V_{p-p}
36	DAC2 (ACB pulse)	Outputs 1-bit DAC or ACB pulse Open-collector output		DC or ACB pulse 

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
37 38 39	ANALOG OSD B IN ANALOG OSD G IN ANALOG OSD R IN	Inputs analog OSD signal via clamp capacitor. Recommended input amplitude: 0.7 V_{p-p} (no sync) at 100% white		100 IRE: 0.7 V_{p-p}
40	RGB V_{CC}	V_{CC} pin for text/RGB block. To ascertain the correct voltage for V_{CC}, please refer to the table entitled Maximum Ratings.	—	—
41 42 43	B OUT G OUT R OUT	Outputs R/G/B signal. Recommended output amplitude: 100 IRE = 2.3 V_{p-p}		100 IRE: 2.3 V_{p-p} Conditions: UNI-COLOR = max SUB-CONT = Cent Y IN = 0.7 V_{p-p}
44	RGB GND	GND pin for text/RGB block.	—	—

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
45	I_K IN	Inputs the feedback signal from CRT. (BLK level should be 0 V to 3 V.) When ACB is not used, connect this pin to the RGB V_{CC} pin.		 or RGB V_{CC}
46 47 48	B S/H G S/H R S/H	Sample-and-hold (S/H) pin. In ACB mode connect a 2.2-μF capacitor. In CUTOFF mode connect a 0.01-μF capacitor.		DC

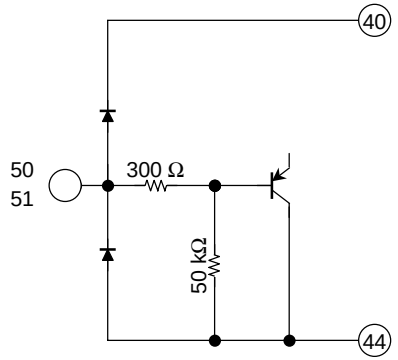
<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>Interface Circuit</th><th>Input Signal/Output Signal</th></tr>
<tr><td>49</td><td>Y_S3
(analog RGB)</td><td>Selects input between internal RGB and external analog RGB according to voltage value input to this pin.

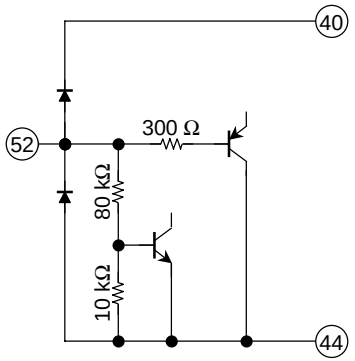
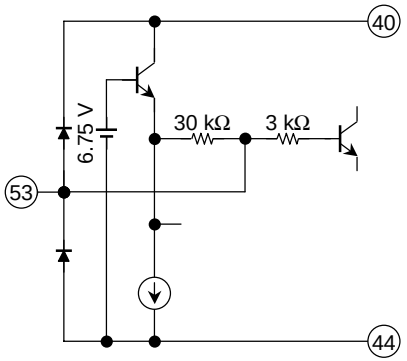
When analog RGB is selected, mutes VSM output.</td><td> 
</td><td>0~0.5 V: Internal
1.5~9 V: Analog RGB, VSM mute</td></tr>
<tr><td>50

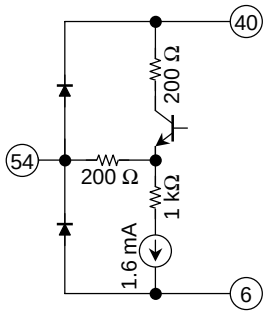
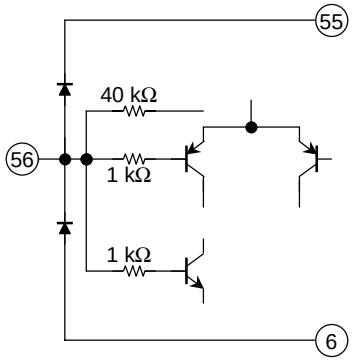
51</td><td>Y_S2
(analog OSD)

Y_S1
(analog OSD)</td><td>Switches between internal RGB and OSD input signals.

Voltage applied to Y_S1 and Y_S2 adjusts blend ratio of internal RGB and OSD signals.

When Y_S1 or Y_S2 is High, mutes VSM output.
<table>
<tr><th>Y_S2</th><th>Y_S1</th><th>Blend ratio
Int RGB:
OSD RGB</th></tr>
<tr><td>L</td><td>L</td><td>10:0</td></tr>
<tr><td>H</td><td>L</td><td>7:3</td></tr>
<tr><td>L</td><td>H</td><td>5:5</td></tr>
<tr><td>H</td><td>H</td><td>0:10</td></tr>
</table></td><td> 
</td><td>0~0.5 V: Internal
1.1~1.7 V: VSM mute
2.9~9 V: OSD, VSM mute</td></tr>
</table>

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
52	Y_M/P-MUTE/BLK	Fast half-tone switch for internal RGB signal. Also performs image mute or blanking.		0~0.5 V: Internal 1.2~1.8 V: Half-tone 2.7~4.0 V: P-mute 7~9 V: Blanking
53	ABCL IN	ABL and ACL input pin. Can set gain and start point for ABL and dynamic ABL by BUS control.		DC

Pin No.	Pin Name	Function	Interface Circuit	Input Signal/Output Signal
54	VSM OUT	Outputs Y signal for VSM which passes through HPF circuit (primary differential circuit). Mutes output signal using pins 49, 50 and 51.		—
55	Y/C V_{CC}	V_{CC} pin for Y/C block. To ascertain the correct voltage for V_{CC}, please refer to the table entitled Maximum Ratings.	—	—
56	APL FILTER	Connect filter for correcting DC restoration. Leaving this pin open enables user to monitor Y signal after black stretch and dynamic γ.		—

Bus Control Map

Write Mode

Slave Address: 88H

Sub-Add	D7	D6	D5	D4	D3	D2	D1	D0	Preset
00	H-FREQ		H-DUTY	YUV-SW	DAC1	DAC2	SYNC INPUT-SW		1000 0000
01	HORIZONTAL POSITION							CLP-PHS	1000 0000
02	ACB-MODE		SCP-SW	HBP-PHS	SYNC SEP-LEVEL		TEST		1000 0000
03	V-BLK PHASE					VERTICAL FREQUENCY			1000 0000
04	COMPRESSION-BLK PHASE-1				COMPRESSION-BLK PHASE-2				1000 0000
05	P-MODE1	UNI-COLOR							1000 0000
06	BRIGHTNESS								1000 0000
07	OSD-ACL	COLOR							1000 0000
08	TINT							RGB-ACL	1000 0000
09	PICTURE SHARPNESS							YNR	1000 0000
0A	RGB BRIGHTNESS							DCRR-SW	1000 0000
0B	HI BRT	RGB CONTRAST							1000 0000
0C	SUB CONTRAST					WPS	YUV INPUT MODE		1000 0000
0D	DRIVE GAIN1							DR-R	1000 0000
0E	DRIVE GAIN2							DR-B/G	1000 0000
0F	R CUT OFF								1000 0000
10	G CUT OFF								1000 0000
11	B CUT OFF								1000 0000
12	R-Y/B-Y GAIN				R-Y/B-Y PHASE				1000 0000
13	G-Y/B-Y GAIN				G-Y/B-Y PHASE				1000 0000
14	COLOR SRT GAIN			C-SRT FREQ		COLOR γ		CLT	1000 0000
15	C.D.E.		Y/C GAIN COMP1		Y/C GAIN COMP2		FRESH-COLOR		1000 0000
16	VSM PHASE			VSM GAIN			APACON PEAK FREQ		1000 0000
17	DC REST POINT			DC REST RATE			DC REST LIMIT		1000 0000
18	BLACK STRETCH POINT			APL VS BSP		B.L.C.	B.D.L	BS-ARE	1000 0000
19	SHR-TRACKING		WPL-LEVEL			WPL-FREQ			1000 0000
1A	DYNAMIC ABL POINT			DYNAMIC ABL GAIN			P-MODE2		1000 0000
1B	ABL POINT			ABL GAIN			RGB OUT MODE		1000 0000
1C	DYNC γ-POINT		DYNC γ GAIN VS DARK AREA			STATIC γ-GAIN		Y-OUT γ	1000 0000
1D	OSD BRIGHT		OSD CONTRAST		Y/C-DL1	APACON WPL			1000 0000
1E	Y DETAIL CONTROL					WP BLUE POINT			1000 0000
1F	Y GROUP DELAY CORRECTION				Y/C-DL2	WP BLUE GAIN			1000 0000

Read Mode

Slave Address: 89H

	D7	D6	D5	D4	D3	D2	D1	D0
0	POR	IK-IN	RGB-OUT	YUV-IN	H-OUT	VP-OUT	RGB-IN	SYNC-IN

Bus Control Functions

Write Mode

Parameter	Explanation	Preset
H-FREQUENCY	Selects horizontal oscillation frequency. 00: 15.75 kHz, 01: 31.5 kHz, 10: 33.75 kHz, 11: 45 kHz Control by pin 22 has priority over BUS control. When this IC will be used on CRT, the frequency of H-out should be controlled by pin 22.	33.75 kHz
H-DUTY	Switches horizontal output duty. 0: 41%, 1: 47%	41%
YUV-SW	Switches YUV input. 0: INPUT-1 ($Y1/C_{b1}/C_{r1}$), 1: INPUT-2 ($Y2/C_{b2}/C_{r2}$)	INPUT-1
DAC 1	Switches DAC control output. Don't use this function	Open
DAC 2	Switches DAC control output. 0: On (low), 1: Open (high) When TEST = 00, controls 1-bit DAC when output is open-collector. When TEST = 01, outputs ACB reference pulse from pin 36.	On
SYNC INPUT-SW	Selects sync input. 00: Selects HD1/VD1 input. 01: Selects HD2/VD2 input. 10/11: Selects SYNC input.	HD/VD1
HORIZONTAL POSITION	Adjusts horizontal picture phase. 0000000 (–10.5%)~1111111 (+10.5%) (Note) When H-POSITION will be changed, VP width (pin 27) will change.	Center
CLP-PHS	Switches clamp pulse phase. 0: 0.7-μs (2.5%) width with 1.1-μs (3.8%) delay from HD stop phase 1: 0.7-μs (2.4%) width with 0.2-μs (0.7%) delay from HD stop phase While quiescent, 0.8-μs (2.7%) width with 1.2-μs (4.2%) delay from FBP start phase Also switches CP phase of SCP-OUT (pin 18).	1.1-μs delay
ACB MODE	Sets ACB mode. Selects reference level for convergence. 00: ACB off (cutoff BUS control), 01: ACB on (5 IRE), 10: ACB on (10 IRE), 11: ACB on (20 IRE)	ACB on (10 IRE)
SCP-SW	Switches SCP (sandcastle pulse) mode. 0: Internal mode, 1: External input mode Also switches SCP-OUT (pin 18). (Note) Don't use H-BPP for the timing pulse, because H-BPP width of internal mode will be changed by the temperature.	Inside IC
HBP-PHS	Switches horizontal black peak detection pulse phase. 0: ±6.3% of FBP, 1: ±3.5% of FBP	6.3% width
SYNC SEP-LEVEL	Selects SYNC separation level. 00: 8.5%, 01: 20%, 10: 30%, 11: 40%	min
TEST	Test mode When TEST = 00, controls 1-bit DAC when output is open-collector. When TEST = 01, outputs H-SYNC from pin 28 and ACB reference pulse from pin 36. Do not use TEST = 10/11 because this is used for IC Shipment Test mode.	00

Parameter	Explanation	Preset
V-BLK PHASE	Adjusts vertical BLK stop phase. 00000 (16H) ~11110 (46H) (1 H/STEP), 11111: Internal V-BLK off	32 H
V-FREQUENCY	Vertical free-running frequency. Sets vertical pull-in range (Table 1).	1281 H
COMPRESSION-BLK PHASE-1/2	Adjusts compression BLK phase. Adjusts BLK at top and bottom (Table 2).	Off
P-MODE1/2	Selects picture mode. Selects between picture mute, half-tone, blue background, and Y mute (Table 3).	P-MUTE 1
UNI-COLOR	Adjusts unicolor. 0000000 (−16.5dB) ~111 (0dB)	min
BRIGHTNESS	Adjusts brightness. 00000000 (−40 IRE) ~11111111 (+40 IRE)	Center
OSD-ACL	Turns OSD-ACL on/off. 0: Off, 1: On	On
COLOR	Adjusts color. 0000000: Color mute, 0000001 (−20dB or more) ~1111111 (+4.6dB)	C-MUTE
TINT	Adjusts tint. 0000000 (−32 deg) ~1111111 (+32 deg)	Center
RGB-ACL	Switches analog RGB-ACL sensitivity. 0: −6dB, 1: Normal	−6 dB
PICTURE-SHARPNESS	Adjusts sharpness. 0000000 (−10dB or more) ~1111111 (+17dB (at peak FREQ))	Center
YNR	YNR: Turns luminance (Y) noise reduction (NR) on/off. 0: Off, 1: On Lower two bits of PICTURE-SHARPNESS (09-D2/D1) = 00: Trap (at peak FREQ) = 11: Flat YNR level is controlled by lower two bits (09-D2) of PICTURE-SHARPNESS. DL-APACON gain control by PICTURE-SHARPNESS is invalid.	Off
RGB-BRIGHTNESS	Adjusts RGB brightness. 0000000 (−20 IRE) ~1111111 (+20 IRE)	Center
DCRR-SW	Switches DC restoration rate. 0: 100% or more, 1: 100% or less	100% or more
HI BRT	Turns high bright color on/off. 0: Off, 1: On	On
RGB-CONTRAST	Adjusts RGB contrast. 0000000 (−16.5dB) ~1111111 (0dB)	min
SUB-CONTRAST	Adjusts sub-contrast. 00000 (−3.5dB) ~11111 (+2.6dB)	Center
WPS	Adjusts WPS level. 0: 110 IRE 1: 130 IRE	110 IRE
YUV INPUT MODE	Selects Y/color difference signal input mode. 00: Y/Cb/Cr, 01: Y/Pb/Pr, 10: Through, 11: Y/U/V (TA1270) Control by pin takes priority at 00 and 01 (table 4). (Ref.) Y/Cb/Cr: ITU-R BT 601 Y/Pb/Pr: ITU-R BT 709 (1125/60/2:1)	Y/Cb/Cr

Parameter	Explanation	Preset
DRIVE GAIN1/2	Adjusts drive gain 1 and drive gain 2. 0000000 (–5dB) ~1111111 (+3dB)	Center
DR-R DR-B/G	Switches reference RGB drive gain (Table 5).	R
R/G/B CUT OFF	Adjusts R/G/B cutoff. 1) RGB-OUT when ACB off 00000000 (1.9 V) ~11111111 (2.9 V) 2)SENS-IN when ACB on 00000000 (0.5 V_{p-p}) ~11111111 (1.5 V_{p-p})	Center
R-Y/B-Y GAIN	Adjusts R-Y/B-Y relative amplitude. 0000 (0.54) ~1111 (0.85)	Center
R-Y/B-Y PHASE	Adjusts R-Y/B-Y relative phase. 0000 (90 deg) ~1111 (111.5 deg)	min
G-Y/B-Y GAIN	Adjusts G-Y/B-Y relative amplitude. 0000 (0.28) ~1111 (0.38)	Center
G-Y/B-Y PHASE	Adjusts G-Y/B-Y relative phase. 0000 (232 deg) ~1111 (256 deg)	min
COLOR SRT GAIN	Adjusts color SRT gain. 000 (min) ~111 (max)	Center
C-SRT-FREQ	Selects color SRT peak frequency. 00: 4.5 MHz, 01: 5.8 MHz, 10: 8.5 MHz, 11: Off	4.3 MHz
COLOR γ	Selects color γ correction point. 00: Off, 01: 0.23 V_{p-p}, 10: 0.40 V_{p-p}, 11: 0.58 V_{p-p}	Off
CLT	Switches color limiter level. 0: 1.65 V_{p-p}, 1: 2 V_{p-p}	1.65 V_{p-p}
CDE	Adjusts color detail enhancer. 00: min 11: max	Center
Y/C GAIN COMP1/2	Selects dynamic Y/C compensation. COMP1, 00: Off, 01: min, 10: mid, 11: max COMP2, 00: Off, 01: min, 10: mid, 11: max	All off
FRESH-COLOR	Selects flesh color. 00: Off, 01: ±33.7 deg, Normal, 10: ±9.5 deg, High, 11: ±9.5 deg, Normal	Off
VSM-PHASE	Adjusts VSM phase. 000 (–37.5 ns) ~101 (normal) ~111 (+15 ns)	–7.5 ns
VSM GAIN	Adjusts VSM gain. 000: OFF, 001: +3 dB, 111: +19 dB	Off
APACON PEAK f_0	Selects APACON peak frequency. 00: 13.5 MHz, 01: 9.5 MHz, 10: 7.3 MHz, 11: 4.7 MHz	13.5 MHz
DC REST POINT	DC restoration point 000: 0%, 111: 51%	Center
DC REST RATE	Adjusts DC restoration rate. 000 (100%) ~111 (135% (65%))	100%
DC REST LIMIT	Selects DC restoration limit point. 00: 57%, 01: 71%, 10: 78%, 11: 78%	min

Parameter	Explanation	Preset
BLACK STRETCH POINT	Adjusts black stretch point 1. 000: OFF, 001 (34 IRE) ~111 (53 IRE)	Center
APL VS BSP	Adjusts black stretch point 2. 00 (0 IRE) ~11 (24 IRE) up	0 IRE
B.L.C	Turns black level automatic correction on/off. Max: 8.5 IRE, black stretch has priority. 0: Off, 1: On	Off
B.D.L.	Switches black detection level. 0: 3 IRE, 1: 0 IRE	3 IRE
BS-ARE	Turns black stretch area on/off. 0: On, 1: Off	On
SHR-TRACKING	SHR tracking (adjusts SRT component gain.) 00 (SRT-GAIN max) ~11 (SRT-GAIN min)	Center
WPL-LEVEL	Adjusts white letter improvement amplitude. 000: min 111: max	min
WPL-FREQ	Adjusts white letter improvement start frequency. 000 (5 MHz) ~111 (16 MHz)	5 MHz
DYNAMIC ABL POINT	Adjusts dynamic ABL detection voltage. 000 (min) ~111 (max)	Center
DYNAMIC ABL GAIN	Adjusts dynamic ABL sensitivity. 000 (min) ~111 (max)	min
ABL POINT	Adjusts ABL detection voltage. 000 (min) ~111 (max)	Center
ABL GAIN	Adjusts ABL sensitivity. 000 (min) ~111 (max)	min
RGB-OUT MODE	Switches RGB output mode (switch for RGB output mode for test and adjustment). 00: Normal, 01: R only, 10: G only, 11: B only	Normal
DYNCγ-POINT	Switches dynamic Y γ point. 00: 20 IRE, 01: 21.5 IRE, 10: 23.5 IRE, 11: 25 IRE	23.5 IRE
DYNCγ GAIN VS DARK AREA	Turns dynamic Y γ gain VS dark area on/off. 000 (min) ~ 111 (max (when 25 IRE or below is 25% or more of area ratio, +3dB))	min
STATICγ-GAIN	Turns static Y γ dark area gain on/off. 00: Off (0dB) 11: max (1.5dB, at this time, DYNCγ gain is +1.5dB max)	Off
Y-outγ	Turns Y-out γ on/off. 0: Off, 1: On	Off
OSD BRIGHT	Adjusts OSD brightness. 00: 5 IRE, 01: 0 IRE, 10: –5 IRE, 11: –10 IRE	–5 IRE
OSD-CONTRAST	Adjusts OSD contrast. 00 (min (–9.5dB)) ~11 (max (0dB))	min
Y/C DL1/2	Adjust Y/C relative phase: Y phase before RGB matrix is changed. Y/C DL2 = 0 and Y/C DL1 = 0: –10 ns, Y/C DL2 = 0 and Y/C DL1 = 1: –5 ns Y/C DL2 = 1 and Y/C DL1 = 0: 0 ns, Y/C DL2 = 1 and Y/C DL1 = 1: +5 ns	–10 ns
APACON WPL	Adjusts APACON white peak limiter. 000 (Off) ~111 (Maximum effect of positive limiter)	Off

Parameter	Explanation	Preset
Y DETAIL CONTROL	Controls Y detail: Adjusts differential signal for frequency other than picture sharpness. 00000 (min (trap)) ~11111 (max (+6dB)) Peak frequency linked to APACON PEAK FREQ 00: 5.5 MHz, 01: 3.7 MHz, 10: 14.5 MHz, 11: 10 MHz	Center
WP BLUE POINT	Adjusts white peak blue point. 000 (60 IRE) ~111 (112 IRE)	min
Y-GROUP DELAY CORRECTION	Corrects Y group delay. 0000: Decreases preshoot gain (increases overshoot gain). 1111: Decreases overshoot gain (increases preshoot gain).	Center
WP BLUE GAIN	Adjusts white peak blue gain. 000 (min (+2.3 dB)) ~111 (max (+10 dB))	min

Table 1: Vertical Frequency

Data	V PULL-IN Range	V-BPP		Format/V-FREQUENCY, H-FREQUENCY
		Start Phase	Stop Phase	
000	48~1281H	1100H	V-BLK P. (C.BLK P.) +20 H	1125P/30 Hz (33.75 kHz)
001	48~849H	730H		750P/60 Hz (45 kHz)
010	48~725H	600H		625P/50 Hz (31.5 kHz)
011	48~660H	545H		1125I/60 Hz (33.75 kHz)
100	48~613H	500H		525P/60 Hz (31.5 kHz)
101	48~363H	290H		PAL/SECAM/50 Hz (15.625 kHz), 100 Hz (31.5 kHz)
110	48~307H	240H		NTSC/60 Hz (15.734 kHz), 120 Hz (31.5 kHz)
111	VP-OUT HI	—	—	—

Table 2: Compression-BLK Phase

V-FREQUENCY	PHASE-1 (start phase)	PHASE-2 (stop phase)
000	1088H~1118H	50H~78H (0000: C-BLK OFF)
001	720H~750H	
010	592H~622H	
011	528H~558H	
100	488H~518H	
101	280H~310H	
110	224H~254H	
111	C-BLK OFF	

Table 3: P-Mode

05-D7	1A-D1	1A-D0	MODE	Details
0	0	0	NORMAL 1	Can mute picture or half-tone main signal using Y_M pin. Can insert analog RGB-IN using Ys3; OSD-IN using Ys1/Ys2. Analog RGB-IN > P-Mute
0	0	1	Y-MUTE	Mutes main signal Y in whole picture using BUS. Can insert analog RGB-IN using Ys3; OSD-IN using Ys1/Ys2. Analog RGB-IN > P-Mute
0	1	0	Y_M 1	Half-tones main signal in whole picture using BUS. Can insert P-Mute using Y_M pin. Can insert analog RGB-IN using Ys3. Blends OSD-IN with main H/T signal using Ys1/Ys2. Analog RGB-IN > P-Mute
0	1	1	BB	Blue-backs main signal using BUS. Can insert P-Mute using Y_M pin. Can insert analog RGB-IN using Ys3; OSD-IN using Ys1/Ys2. Analog RGB-IN > P-Mute
1	0	0	P-MUTE 1	Mutes main signal in whole picture using BUS. Can insert analog RGB-IN using Ys3; OSD-IN using Ys1/Ys2. Analog RGB-IN > P-Mute
1	0	1	Y_M2	Cannot be used.
1	1	0	P-MUTE 2	Cannot be used.
1	1	1	NORMAL 2	Cannot be used.

Output priority: main signal < BB < P-MUTE < RGB-IN < OSD-IN

Table 4: YUV INPUT MODE

YUV INPUT MODE	Pin 7	MATRIX
00	LOW	YCbCr → Internal YUV
	HIGH	YPbPr → Internal YUV
	OPEN	YCbCr → Internal YUV
01	LOW	YCbCr → Internal YUV
	HIGH	YPbPr → Internal YUV
	OPEN	YPbPr → Internal YUV
10	—	Through
11	—	YUV → Internal YUV

Table 5: DR-R, DR-B/G

0D-D0	0E-D0	Reference Axis	Drive Gain1	Drive Gain2
0	0	R	G	B
0	1	R	G	B
1	0	G	R	B
1	1	B	G	R

Read Mode

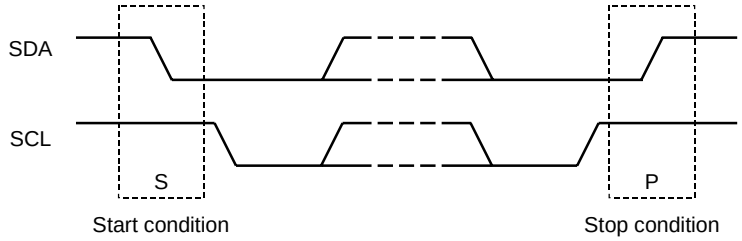
Parameter	Explanation
POR	Power-on reset 0: Register preset, 1: Normal After power-on, 0 is read on first read; 1 on subsequent reads.
IK-IN	IK input detection: detects input to pin 45. 0: NG (no input), 1: OK (input)
RGB-OUT	RGB-OUT self-check result: detects output from pins 41, 42 and 43. 0: NG (no output), 1: OK (output) Returns OK when signal is detected on all three outputs. If signals are small, does not return OK.
YUV-IN	YUV-IN self-check result: detects input to pins 3, 4 and 5 or pins 8, 9 and 10. 0: NG (no input), 1: OK (input) Returns OK when AC signal is detected on all three inputs. If signals are small or are DC voltage, does not return OK.
H-OUT	H-OUT self-check result: detects output from pin 26. 0: NG (no output), 1: OK (output)
VP-OUT	VP-OUT self-check result: detects output from pin 27. 0: NG (no output), 1: OK (output)
RGB-IN	RGB-IN self-check result: detects input to pins 33, 34 and 35. 0: NG (no input), 1: OK (input) Returns OK when AC signal is detected on all three inputs. If signals are small or are DC voltage, does not return OK.
SYNC-IN	SYNC-IN self-check result: detects input to pin 14. 0: NG (no input), 1: OK (input)

Data Transfer Format via I^2C BUS

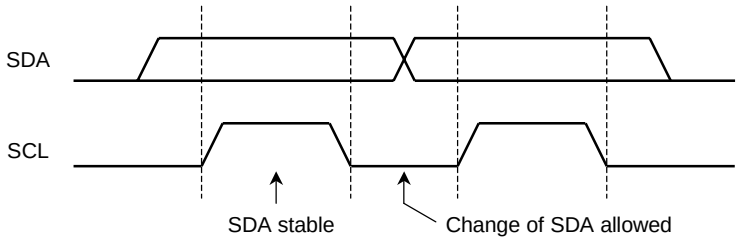
Slave Address: 88H

A6	A5	A4	A3	A2	A1	A0	W/R
1	0	0	0	1	0	0	0/1

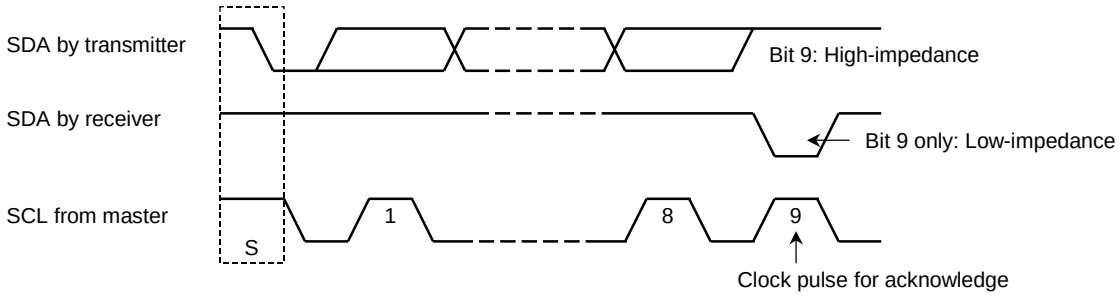
Start and Stop Condition



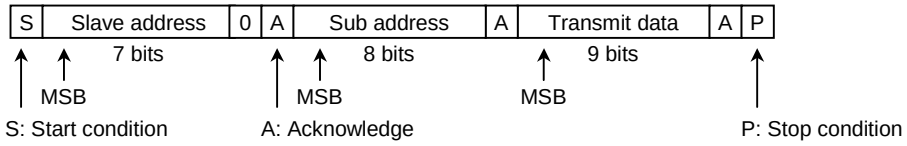
Bit Transfer



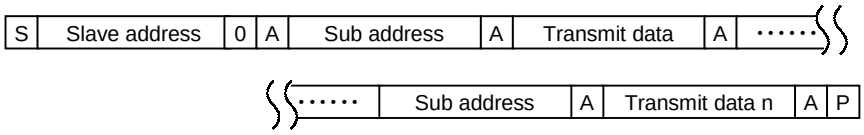
Acknowledge



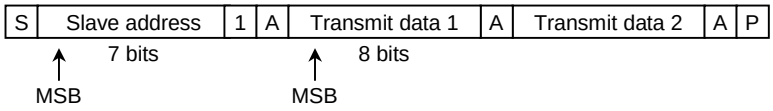
Data Transmit Format 1



Data Transmit Format 2



Data Receive Format

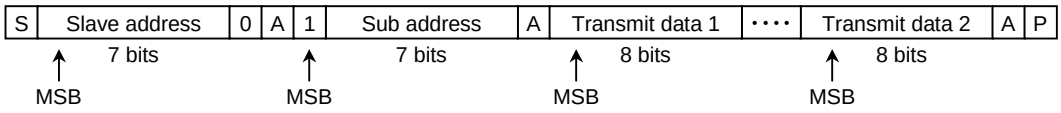


At the moment of the first acknowledge, the master transmitter becomes a master receiver and a slave transmitter.

The Stop condition is generated by the master.

Details are provided in the Philips I^2C specifications.

Optional Data Transmit Format: Automatic Increment Mode



In this transmission method, data is set on automatically incremented sub-address from the specified sub-address.

Purchase of TOSHIBA I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating			Unit
		PCB A	PCB B	PCB C	
Power supply voltage	V_{CC}max	12	12	12	V
Input pin signal voltage	e_{in}max	9	9	9	V_{p-p}
Power dissipation	P_D (Note1)	2551	2717	3378	mW
Power dissipation reduction rate	1/θja	20.4	21.7	27.0	mW/°C
Operating temperature	T_{opr}	−20~65	−20~65	−20~65	°C
Storage temperature	T_{stg}	−55~150	−55~150	−55~150	°C
Power supply voltage (Pins 19, 40, 55)	min	8.5	8.7	8.7	V
	typ.	8.8	9.0	9.0	
	max	9.1	9.3	9.3	

Note 1: Please see the following Figure.
Note, however, that the conditions apply only to the case where the device is mounted on board A (180 mm × 125 mm × 1.6 mm, one-sided); board B (329 mm × 249 mm × 1.6 mm, two-sided); or board C (276 mm × 192 mm × 1.6 mm, six-layered). When mounting the IC, select boards no smaller than these. When using under the conditions of board A, set the IC's power supply voltage (pins 19, 40, 55) to 8.8 V (±0.3 V) Because the IC's thermal capacity margin is narrow, when designing a set, incorporate heat discharge features into the design. Note that the power dissipation varies widely depending on the board mounting conditions.

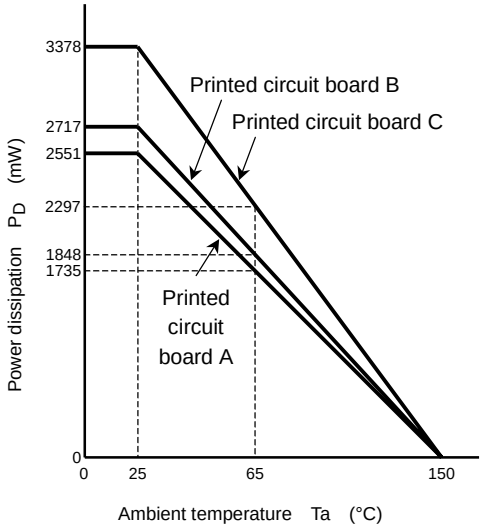


Figure 1 Characteristics of decrease in power dissipation

Note 2: Pins 3, 4, 5, 7, 8, 9, 10, 11, 20, 21, 22, 23, 30, 31, 33, 34, 36, 39, 45, 46, 49, 50, 51, 52 and 53 are susceptible to damage from surge voltages and should thus be handled with extreme care.

Note 3: Power supply sequence

At power-on, power should be supplied to the IC's power supply pins according to the following sequence: first to pin 29 (I^2L V_{DD}), then to pin 19 (DEF/DAC V_{CC}), and finally to pin 40/pin 55 (RGB V_{CC}/YC V_{CC}). Power to pin 29 should be supplied from pin 19 via zener diode through resister.

If power is not supplied to all the power pins or if power is not supplied in the above sequence, BUS preset will be unsettled and the IC may not function properly.

Especially, when the frequency of H-out (pin 26) will be unsettled, H deflection output transistor may be broken.

When this IC will be used on CRT, the frequency of H-out should be controlled by pin 22.

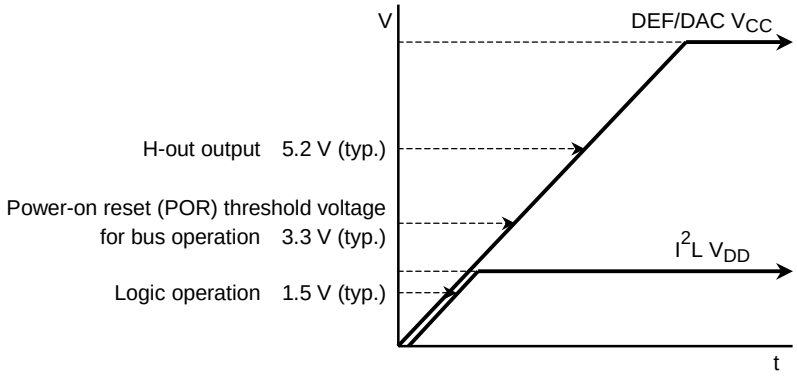


Figure (Note 3) Timing from immediately after power-on to time at which H-out is output (at Ta = 25°C)

Note 4: V_{CC} condition at Power-OFF

At power-off, the last pulse of H-out (pin 26) will become unknown, if I^2L V_{DD} (pin 29) is over 1.7 V at the timing of H-out stop.

I^2L V_{DD} should be below 1.7 V when DEF/DAC V_{CC} (pin 19) will be 6.2 V, which is the maximum voltage when H-out stops.

Refer to Figure (Note 4-1).

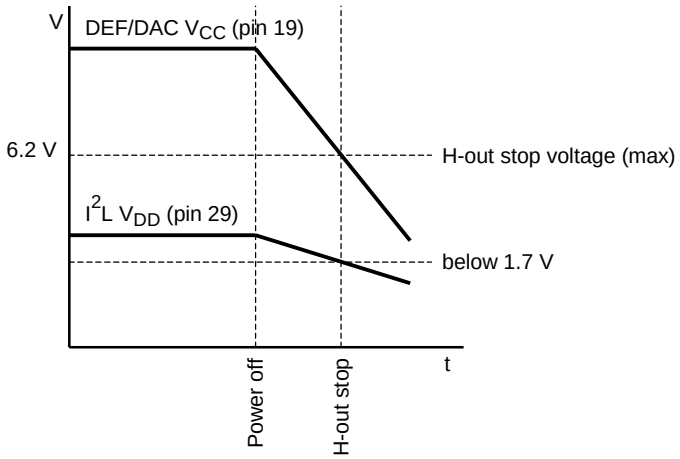


Figure (Note 4-1) V_{CC} condition at power-off

If it is not in the condition of Figure (Note 4-1), it is recommended that H-out will be made LOW at power-off by external control like micro-processor ang so on. Refer to Figure (Note 4-2).

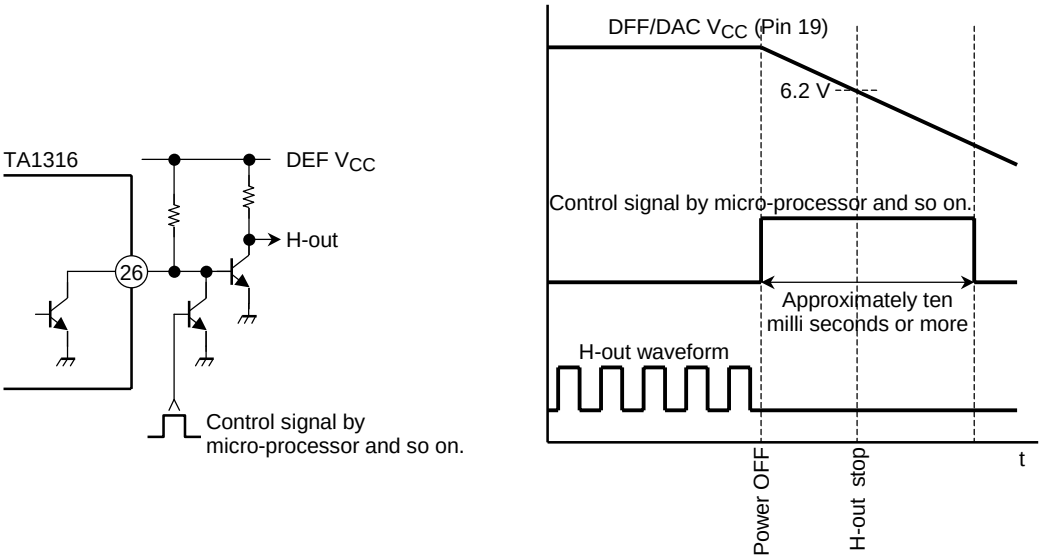


Figure (Note 4-2) Example how to stop H-out

Recommended Operating Conditions

Characteristics	Description		Min	Typ.	Max	Unit
Supply voltage (V_{CC})	Pins 19, 40 and 55	Board A (Note1)	8.5	8.8	9.1	V
		Boards B and C (Note1)	8.7	9.0	9.3	
	Pin 29		1.8	2.0	2.2	
Y input level	Pins 3 and 8: 100% color bar, including sync (picture signal: 0.7 V_{p-p})		—	1.0	—	V_{p-p}
Color difference signal input level	Pins 4, 5, 9 and 10: 100% color bar, no sync		—	0.7	—	
Matrix switching voltage	Pin 7		2.0	3.0	5.0	V
HD/VD input level	Pins 12, 13, 15 and 16		2.0	5.0	9.0	V_{p-p}
SYNC input level	Pin 14: 100% color bar, including sync		0.9	1.0	1.1	
SCP input level	Pin 17	CP	4.7	5.0	9.0	V
		BPP	2.2	2.5	2.8	
Horizontal frequency switching voltage	Pin 22	15.75 kHz	8.0	9.0	9.0	
		31.5 kHz	5.0	6.0	7.0	
		33.75 kHz	2.0	3.0	4.0	
		45 kHz	0	0	1.0	
FBP input level	Pin 24	H-AFC	4.0	5.0	9.0	
		H-BLK	1.7	2.25	2.8	
H-OUT input current	Pin 26		—	9.0	15.0	mA
DAC input current	Pins 28 and 36		—	0.3	1.0	
SCL/SDA pull-up voltage	Pins 30 and 31		3.3	5.0	9.0	V
SDA input current	Pin 31		—	—	2	mA
Analog RGB input level	Pins 35, 34 and 33: White 100%		—	0.7	—	V_{p-p}
Analog OSD input level	Pins 37, 38 and 39: White 100%		—	0.7	—	
Y_S3 switching voltage	Pin 49		1.5	5.0	9.0	V
Y_S1/2 switching voltage	Pins 51 and 50	OSD	2.9	5.0	9.0	
		VSM MUTE	1.1	1.5	1.7	
Y_M switching voltage	Pin 52	BLK	7.0	9.0	9.0	
		P-MUTE	2.7	3.2	4.0	
		HALF TONE	1.2	1.5	1.8	
External V-BLK input current	Pin 27		0.78	—	1	mA

Note1: For the parameter values for boards A, B and C, please refer to the table entitled Maximum Ratings.

Electrical Characteristics (V_{CC} = 9 V/2 V, Ta = 25°C, unless otherwise specified)

Current Dissipation

Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
DEF/DAC V_{CC}	I_{CC1}	—	21.0	24.2	26.9	mA
RGB V_{CC}	I_{CC2}	—	55.3	63.6	70.8	
I^2L V_{DD}	I_{CC3}	—	21.0	24.1	26.8	
Y/C V_{CC}	I_{CC4}	—	39.3	45.3	50.3	

Pin Voltage

Test Condition

(1) BUS = Preset

(2) SW1 = B, SW2 = B, SW3 = C, SW4 = B, SW5 = B, SW7 = A, SW8~10 = B, SW14 = B, SW20 = ON, SW23 = B, SW24 = A, SW26 = A, SW33~35 = A, SW37~39 = A, SW54 = OFF, SW56 = ON

Pin No.	Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
2	BPH FILTER	V_2	—	5.5	5.8	6.1	V
3	Y1 IN	V_3	—	4.7	5.0	5.3	
4	Cb/Pb1 IN	V_4	—	4.7	5.0	5.3	
5	Cr/Pr1 IN	V_5	—	4.7	5.0	5.3	
7	MATRIX SW	V_7	—	2.0	3.0	4.0	
8	Y2 IN	V_8	—	4.7	5.0	5.3	
9	Cb/Pb2 IN	V_9	—	4.7	5.0	5.3	
10	Cr/Pr2 IN	V_{10}	—	4.7	5.0	5.3	
11	COLOR LIMITER	V_{11}	—	6.65	6.9	7.15	
12	VD2 IN	V_{12}	—	0	0	0.3	
13	HD2 IN	V_{13}	—	0	0	0.3	
14	SYNC IN	V_{14}	—	1.6	2.0	2.4	
15	VD1 IN	V_{15}	—	0	0	0.3	
16	HD1 IN	V_{16}	—	0	0	0.3	
17	SCP IN	V_{17}	—	3.9	4.4	4.9	
20	AFC FILTER	V_{20}	—	5.8	6.5	7.2	
21	HVCO	V_{21}	—	5.0	5.3	5.6	
23	H CURVE CORRECTION	V_{23}	—	2.2	2.5	2.8	
33	ANALOG B IN	V_{33}	—	3.65	3.95	4.25	
34	ANALOG G IN	V_{34}	—	3.65	3.95	4.25	
35	ANALOG R IN	V_{35}	—	3.65	3.95	4.25	
37	ANALOG OSD B IN	V_{37}	—	3.65	3.95	4.25	
38	ANALOG OSD G IN	V_{38}	—	3.65	3.95	4.25	
39	ANALOG OSD R IN	V_{39}	—	3.65	3.95	4.25	
46	B S/H	V_{46}	—	3.5	4.0	4.5	
47	G S/H	V_{47}	—	3.5	4.0	4.5	
48	R S/H	V_{48}	—	3.5	4.0	4.5	
49	Y_S3	V_{49}	—	0.0	0.1	0.2	
50	Y_S2	V_{50}	—	0.0	0.1	0.2	
51	Y_S1	V_{51}	—	0.0	0.1	0.2	
52	Y_M	V_{52}	—	0.0	0.1	0.2	
53	ABCL IN	V_{53}	—	5.85	6.1	6.35	
54	VSM OUT	V_{54}	—	4.2	4.4	4.6	
56	APL FILTER	V_{56}	—	4.8	5.0	5.2	

Luminance Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Y input dynamic range	D_{RY}	—	—	0.7	1.0	1.5	V_{p-p}
Black detection level shift	V_B	—	(Note P01)	−15	−5	5	mV
	V_{B3}	—		35	45	55	
Black stretch amplifier maximum gain	G_{BS}	—	(Note P02)	2.5	3.0	3.5	dB
Black stretch start point 1	P_{BST1}	—	(Note P03)	31	34	37	IRE
	P_{BST2}	—		50	53	56	
Black stretch start point 2	P_{BS1}	—	(Note P04)	0	5	10	IRE
	P_{BS2}	—		19	24	29	
Dynamic ABL detection voltage	DV_{001}	—	(Note P05)	30	50	70	mV
	DV_{010}	—		80	100	120	
	DV_{100}	—		190	220	250	
Dynamic ABL sensitivity	S_{DAMIN}	—	(Note P06)	—	0.005	0.02	V/V
	S_{DAMAX}	—		0.29	0.32	0.35	
Black level correction	BLC	—	(Note P07)	7.0	8.5	10	IRE
Dynamic Y γ correction point	P_{DGP00}	—	(Note P08)	17	20	23	IRE
	P_{DGPA}	—		0.5	1.5	2.5	
	P_{DGPB}	—		2	3.5	5	
	P_{DGPC}	—		3	5	7	
Dynamic Y γ gain	G_{DG}	—	(Note P09)	2	3	4	dB
Static Y γ dark area gain	G_{SG}	—	(Note P10)	1.3	1.7	2.2	dB
DC restoration gain	ADT_{100}	—	(Note P11)	0.9	1.1	1.2	times
	ADT_{135}	—		1.2	1.35	1.5	
	ADT_{65}	—		0.55	0.7	0.85	
DC restoration start point	V_{DT0}	—	(Note P12)	−5	0	5	%
	V_{DT1}	—		47	51	55	
DC restoration limit point	P_{DTL11}	—	(Note P13)	54	57	61	%
	P_{DTL10}	—		67	71	75	
	P_{DTL01}	—		74	78	82	
	P_{DTL00}	—		74	78	82	
Sharpness control peak frequency	F_{AP00}	—	—	12.2	13.5	14.9	MHz
	F_{AP01}	—		8.5	9.5	10.5	
	F_{AP10}	—		6.5	7.3	8.1	
	F_{AP11}	—		4.2	4.7	5.2	
Sharpness control range	G_{MAX00}	—	(Note P14)	13	16	18	dB
	G_{MIN00}	—		−15	−8	−4	
	G_{MAX01}	—		14	17	19	
	G_{MIN01}	—		−20	−14	−7	
	G_{MAX10}	—		14	17	19	
	G_{MIN10}	—		−25	−16	−7	
	G_{MAX11}	—		14	18	20	
	G_{MIN11}	—		−30	−20	−8	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Sharpness control center characteristic	G_{CEN00}	—	(Note P15)	7.5	10	12.5	dB
	G_{CEN01}	—		8	11	13	
	G_{CEN10}	—		8	11	13	
	G_{CEN11}	—		9	12	14	
YNR characteristic	G_{YNRT00}	—	(Note P16)	−15	−8	−4	dB
	G_{YNRF00}	—		−3	−1	1	
	G_{YNRT01}	—		−20	−12	−8	
	G_{YNRF01}	—		−3	−1	1	
	G_{YNRT10}	—		−20	−13	−8	
	G_{YNRF10}	—		−2	−0.5	1.5	
	G_{YNRT11}	—		−25	−12	−8	
	G_{YNRF11}	—		−2	0	2	
Control of SRT response to 2T pulse input	T_{SRT00}	—	(Note P17)	0.05	0.4	0.7	dB
	T_{SRT01}	—		0.5	1	2	
	T_{SRT10}	—		1.5	2	4	
	T_{SRT11}	—		3.5	5	7	
VSM peak frequency	F_{VSM}	—	—	15	19	22.8	MHz
VSM gain	G_{V000}	—	(Note P18)	—	−39	−35	dB
	G_{V001}	—		2	3	4	
	G_{V010}	—		5.5	6.5	7.5	
	G_{V011}	—		9.5	11	12	
	G_{V100}	—		12.5	13.8	15	
	G_{V101}	—		14.5	16	17.5	
	G_{V110}	—		15.5	16.8	18.5	
	G_{V111}	—		17.5	18.6	19.5	
Threshold voltage of VSM muting	V_{SR49}	—	Pins 49, 50 and 51	0.62	0.72	0.85	V
	V_{SR50}	—		0.62	0.72	0.85	
	V_{SR51}	—		0.62	0.72	0.85	
Response time for VSM muting	T_{VM49A}	—	(Note P19)	0	30	100	ns
	T_{VM49B}	—		0	30	100	
	T_{VM50A}	—		0	30	100	
	T_{VM50B}	—		0	30	100	
	T_{VM51A}	—		0	30	100	
	T_{VM51B}	—		0	30	100	
VSM limit	V_{LU}	—	(Note P20)	0.58	0.65	0.75	V_{p-p}
	V_{LD}	—		0.55	0.62	0.75	
Delay time from Y input to R output	T_{YR}	—	(Note P21)	96	120	144	ns
Y delay time switch	YDLA	—	(Note P22)	3	5	7	ns
	YDLB	—		7	10	13	
	YDLC	—		11	15	19	
Transfer distortion correction	G_{AMIN}	—	(Note P23)	−5	−3.2	−2.0	dB
	G_{BMIN}	—		1	2	3.5	
	G_{AMAX}	—		0.3	1.0	1.7	
	$G_{BMA\ X}$	—		−3.0	−1.5	−1.0	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color detail enhancer	G_{CDE00}	—	(Note P24)	5.5	6.8	8	dB
	G_{CDE01}	—		5.5	6.8	8	
	G_{CDE10}	—		5.5	6.8	8	
	G_{CDE11}	—		5.5	6.8	8	
Y detail frequency	F_{YD00}	—	—	4.4	5.5	6.6	MHz
	F_{YD01}	—		2.9	3.7	4.5	
	F_{YD10}	—		11.6	14.5	17.4	
	F_{YD11}	—		8	10	12	
Y detail control range	$G_{YDMAX00}$	—	(Note P25)	6	9	12	dB
	$G_{YDMAX01}$	—		7	10	13	
	$G_{YDMAX10}$	—		2.5	5.5	8.5	
	$G_{YDMAX11}$	—		3	6	9	
	$G_{YDCEN00}$			3.5	6.5	9.5	
	$G_{YDCEN01}$			4	7	10	
	$G_{YDCEN10}$			−2	0.8	2	
	$G_{YDCEN11}$			−1	1	2	
	$G_{YDMIN00}$	—		0	1.5	3	
	$G_{YDMIN01}$	—		0	2	4	
	$G_{YDMIN10}$	—		−8	−5	−2	
	$G_{YDMIN11}$	—		−18	−15	−12	
APACON white peak limiter	G_{WPL1}	—	(Note P26)	−10	−7	−4	dB
	G_{WPL2}	—		−7	−4.8	−2	
	G_{WPL3}	—		−5	−2.3	−0.5	

Color Difference 1/YUV Input and Matrix Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color difference signal input dynamic range	D_{BB}	—	—	0.7	0.9	1	V_{p-p}
	D_{RR}	—		0.7	0.9	1	
Color difference signal tint control characteristic	T_{RMAX}	—	—	25	29	33	°
	T_{RMIN}	—		–37	–33	–29	
	T_{BMAX}	—		27	31	35	
	T_{BMIN}	—		–36	–32	–28	
Matrix fast SW threshold voltage	V_{MSW}	—	Pin 7	0.65	0.72	0.8	V
Color SRT peak frequency	F_{B00}	—	—	3.6	4.5	5.4	MHz
	F_{B01}	—		4.6	5.8	7.0	
	F_{B10}	—		6.8	8.5	10.2	
	F_{R00}	—		3.6	4.5	5.4	
	F_{R01}	—		4.6	5.8	7.0	
	F_{R10}	—		6.8	8.5	10.2	
Color SRT gain	GS_{B00CEN}	—	(Note S01)	5	8	11	dB
	GS_{B00MAX}	—		9	12	15	
	GS_{B01CEN}	—		2	5	8	
	GS_{B01MAX}	—		5	8	11	
	GS_{B10CEN}	—		1	2	5	
	GS_{B10MAX}	—		1	3	6	
	GS_{R00CEN}	—		5	8	11	
	GS_{R00MAX}	—		9	12	15	
	GS_{R01CEN}	—		2	5	8	
	GS_{R01MAX}	—		5	8	11	
	GS_{R10CEN}	—		1	2	5	
	GS_{R10MAX}	—		1	3	6	
Delay time from Cb1 input to B output	T_B	—	—	104	130	156	ns
Delay time from Cr1 input to R output	T_R	—	—	104	130	156	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color difference signal amplitude correction	GC_{BDY1}	—	(Note S02)	0.3	0.5	0.7	dB
	GC_{BDY2}	—		0.7	1.0	1.3	
	GC_{BDY3}	—		0.7	1.0	1.3	
	GC_{BBS1}	—		0.2	0.4	0.6	
	GC_{BBS2}	—		−1.0	−0.6	−0.5	
	GC_{BBS3}	—		−3.6	−3.3	−3.0	
	GC_{RDY1}	—		0.3	0.5	0.7	
	GC_{RDY2}	—		1.4	1.6	1.8	
	GC_{RDY3}	—		1.4	1.6	1.8	
	GC_{RBS1}	—		0.1	0.3	0.5	
	GC_{RBS2}	—		−1.2	−1.0	−0.8	
	GC_{RBS3}	—		−3.7	−3.3	−2.9	
YUV gain	G_{Y00}	—	(Note S03)	4.5	5.5	6	dB
	G_{Y01}	—		4.5	5.5	6	
	G_{Y10}	—		4.5	5.5	6	
	G_{Y11}	—		4.5	5.5	6	
	G_{BA}	—		0.2	0.4	0.5	
	G_{BB}	—		1.0	1.1	1.3	
	G_{BC}	—		1.0	1.1	1.3	
	G_{RA}	—		0.8	1.0	1.2	
	G_{RB}	—		−1.6	−1.4	−1.2	
	G_{RC}	—		−3.4	−3.2	−3.0	

Color Difference 2 Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Color difference signal contrast adjustment characteristic	ΔV_{uCY}	—	(Note A01)	15.5	17.0	18.5	dB
Color adjustment characteristic	Δv_{cCY+}	—	(Note A02)	3.6	4.6	5.6	dB
	ΔvcCY–	—		–35	–25	–18	
R-Y relative phase and amplitude	θ_{RMAX}	—	—	109	111.5	114	°
	θ_{RCNT}	—		98.5	101	103.5	
	θ_{RMIN}	—		88	90	92	
	V_R/V_{BMAX}	—		0.82	0.85	0.88	times
	V_R/V_{BCNT}	—		0.68	0.71	0.74	
	V_R/V_{BMIN}	—		0.51	0.54	0.57	
G-Y relative phase and amplitude	θ_{GMAX}	—	—	253	256	259	°
	θ_{GCNT}	—		245	248	251	
	θ_{GMIN}	—		229	232	235	
	V_G/v_{BMAX}	—		0.35	0.38	0.41	times
	V_G/v_{BCNT}	—		0.30	0.33	0.36	
	V_G/v_{BMIN}	—		0.25	0.28	0.31	
Color difference signal half-tone characteristic	GHT_{RY}	—	(Note A03)	0.47	0.50	0.53	times
	GHT_{GY}	—		0.47	0.50	0.53	
	GHT_{BY}	—		0.47	0.50	0.53	
Color γ characteristic	$V_{\gamma 1}$	—	(Note A04)	0.09	0.23	0.37	V_{p-p}
	$V_{\gamma 2}$	—		0.26	0.40	0.54	
	$V_{\gamma 3}$	—		0.44	0.58	0.72	
	Δ_γ	—		0.60	0.70	0.80	—
Color limiter characteristic	CLT_0	—	(Note A05)	1.45	1.65	1.85	V_{p-p}
	CLT_1	—		1.80	2.00	2.20	
High bright color gain	HBC_1	—	(Note A06)	0.02	0.04	0.06	times

Text Block

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
AC gain (Y1in~R/G/B out)	G_R	—	(Note T01)	3.39	3.80	4.28	times
	G_G	—		3.39	3.80	4.28	
	G_B	—		3.39	3.80	4.28	
AC gain axial difference	$G_{G/R}$	—	—	0.94	1.00	1.06	—
	$G_{B/R}$	—		0.94	1.00	1.06	
Frequency characteristic (Y1in~R/G/B out)	G_{fR}	—	Flat gain (–3 dB point at 10 MHz)	24	30	—	MHz
	G_{fG}	—		24	30	—	
	G_{fB}	—		24	30	—	
Frequency characteristics (Cb1/Cr1in~R/G/B out)	G_{fCb}	—	—	11	14.5	—	MHz
	G_{fCr}	—		11	14.5	—	
Unicolor adjustment characteristic	ΔV_u	—	(Note T02)	15.5	16.5	17.5	dB
Brightness adjustment characteristic	V_{brMAX}	—	(Note T03)	4.10	4.45	4.80	V
	V_{brCNT}	—		3.05	3.40	3.75	
	V_{brMIN}	—		1.95	2.30	2.65	
White peak slice level	V_{wps1}	—	(Note T04)	2.30	2.45	2.65	V_{p-p}
	V_{wps2}	—		2.70	2.90	3.10	
Black peak slice level	V_{bps}	—	(Note T05)	1.05	1.20	1.35	V
RGB output S/N	N_{41}	—	(Note T06)	—	–55	–49	dB
	N_{42}	—		—	–55	–49	
	N_{43}	—		—	–55	–49	
Half-tone characteristic	G_{HT1}	—	(Note T07)	0.45	0.50	0.55	times
	G_{HT2}	—		0.45	0.50	0.55	
Half-tone ON voltage	V_{HT}	—	Pin 52	0.65	0.85	1.05	V
Vertical blanking pulse output level	V_{VR}	—	—	0.30	0.80	1.30	V
	V_{VG}	—		0.30	0.80	1.30	
	V_{VB}	—		0.30	0.80	1.30	
Horizontal blanking pulse output level	V_{HR}	—	—	0.30	0.80	1.30	V
	V_{HG}	—		0.30	0.80	1.30	
	V_{HB}	—		0.30	0.80	1.30	
Blanking pulse delay time	td_{ON}	—	(Note T08)	—	0.00	0.30	μs
	td_{OFF}	—		—	0.08	0.30	
Sub-contrast variable range	Δv_{su+}	—	—	2.1	2.6	3.1	dB
	Δv_{su-}	—		–4.0	–3.5	–3.0	
Cutoff voltage variable range	CUT+	—	—	0.42	0.47	0.52	V
	CUT–	—		0.42	0.47	0.52	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Drive adjustment variable range	DR_{R1+}	—	(Note T09)	2.5	3.0	3.5	dB
	DR_{R1-}	—		−5.5	−5.0	−4.5	
	DR_{R2+}	—		2.5	3.0	3.5	
	DR_{R2-}	—		−5.5	−5.0	−4.5	
	DR_{G1+}	—		2.5	3.0	3.5	
	DR_{G1-}	—		−5.5	−5.0	−4.5	
	DR_{G2+}	—		2.5	3.0	3.5	
	DR_{G2-}	—		−5.5	−5.0	−4.5	
	DR_{G3+}	—		2.5	3.0	3.5	
	DR_{G3-}	—		−5.5	−5.0	−4.5	
	DR_{B1+}	—		2.5	3.0	3.5	
	DR_{B1-}	—		−5.5	−5.0	−4.5	
	DR_{B2+}	—		2.5	3.0	3.5	
	DR_{B2-}	—		−5.5	−5.0	−4.5	
	DR_{B3+}	—		2.5	3.0	3.5	
	DR_{B3-}	—		−5.5	−5.0	−4.5	
Output voltage at picture muting	MU_{RD}	—	—	1.5	1.7	1.9	V
	MU_{GD}	—		1.5	1.7	1.9	
	MU_{BD}	—		1.5	1.7	1.9	
P mute ON voltage	V_{MUTE}	—	Pin 52	1.90	2.15	2.40	V
Output voltage at blue back	BB_R	—	—	1.0	1.2	1.4	V
	BB_G	—		1.0	1.2	1.4	
	BB_B	—		1.1	1.25	1.4	V_{p-p}
Pin 53 input impedance	Zin	—	(Note T10)	24	30	36	kΩ
ACL characteristic	ACL_1	—	(Note T11)	−7.5	−5.5	−3.5	dB
	ACL_2	—		−16.0	−14.5	−12.0	
ABL point	ABL_{P1}	—	(Note T12)	0.10	0.15	0.20	V
	ABL_{P2}	—		−0.01	0.04	0.09	
	ABL_{P3}	—		−0.07	−0.02	0.03	
	ABL_{P4}	—		−0.17	−0.12	−0.07	
	ABL_{P5}	—		−0.27	−0.22	−0.17	
	ABL_{P6}	—		−0.36	−0.31	−0.26	
	ABL_{P7}	—		−0.44	−0.39	−0.34	
	ABL_{P8}	—		−0.50	−0.45	−0.40	
ABL gain	ABL_{G1}	—	(Note T13)	−0.06	−0.02	0.00	V
	ABL_{G2}	—		−0.17	−0.12	−0.07	
	ABL_{G3}	—		−0.34	−0.29	−0.24	
	ABL_{G4}	—		−0.52	−0.47	−0.42	
	ABL_{G5}	—		−0.68	−0.63	−0.59	
	ABL_{G6}	—		−0.85	−0.80	−0.75	
	ABL_{G7}	—		−1.01	−0.96	−0.91	
	ABL_{G8}	—		−1.09	−1.04	−0.99	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
RGB output mode	V_{43R}	—	(Note T14)	2.15	2.40	2.65	V
	V_{42R}	—		0.30	0.80	1.30	
	V_{41R}	—		0.30	0.80	1.30	
	V_{43G}	—		0.30	0.80	1.30	
	V_{42G}	—		2.15	2.40	2.65	
	V_{41G}	—		0.30	0.80	1.30	
	V_{43B}	—		0.30	0.80	1.30	
	V_{42B}	—		0.30	0.80	1.30	
	V_{41B}	—		2.15	2.40	2.65	
Y-OUT γ characteristic	γ_1	—	(Note T15)	56	66	76	IRE
	γ_2	—		72	82	92	
	Δ_1	—		0.49	1.24	1.99	dB
	Δ_2	—		−1.67	−0.92	−0.17	
	Δ_3	—		−4.59	−3.84	−3.09	
Blue stretch circuit characteristic	BS_{Pmin}	—	(Note T16)	55.0	60.0	65.0	IRE
	BS_{Pcnt}	—		92.5	97.5	102.5	
	BS_{Pmax}	—		107	112	117	
	BS_{Gmin}	—		1.75	2.25	2.75	dB
	BS_{Gcnt}	—		6.4	7.4	8.4	
	BS_{Gmax}	—		9	10	11	
Forced blanking input threshold voltage	V_{BLKIN}	—	Pin 52	5.50	6.00	6.50	V
ACB pulse phase and amplitude	θ_{ACBR}	—	(Note T17)	—	1	—	H
	θ_{ACBG}	—		—	2	—	
	θ_{ACBB}	—		—	3	—	
	V_{ACB1R}	—		0.04	0.07	0.10	V_{p-p}
	V_{ACB1G}	—		0.04	0.07	0.10	
	V_{ACB1B}	—		0.04	0.07	0.10	
	V_{ACB2R}	—		0.16	0.21	0.26	
	V_{ACB2G}	—		0.16	0.21	0.26	
	V_{ACB2B}	—		0.16	0.21	0.26	
	V_{ACB3R}	—		0.41	0.46	0.51	
	V_{ACB3G}	—		0.41	0.46	0.51	
	V_{ACB3B}	—		0.41	0.46	0.51	
IK input amplitude	IK_R	—	(Note T18)	0.73	0.93	1.13	V_{p-p}
	IK_G	—		0.73	0.93	1.13	
	IK_B	—		0.73	0.93	1.13	
IK input cover range	DIK_{in+}	—	(Note T19)	3.00	3.30	3.60	V
	DIK_{in-}	—		−0.50	−0.30	−0.10	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog RGB gain	G_{TXR}	—	(Note T20)	3.03	3.40	3.83	times
	G_{TXG}	—		3.03	3.40	3.83	
	G_{TXB}	—		3.03	3.40	3.83	
Analog RGB gain triaxial difference	$G_{TXG/R}$	—	—	0.94	1.00	1.06	—
	$G_{TXB/R}$	—		0.94	1.00	1.06	
Analog RGB frequency characteristic	Gf_{TXR}	—	At −3dB	30	35	—	MHz
	Gf_{TXG}	—		30	35	—	
	Gf_{TXB}	—		30	35	—	
Analog RGB input dynamic range	DR_{35}	—	—	0.80	1.20	1.50	V_{p-p}
	DR_{34}	—		0.80	1.20	1.50	
	DR_{33}	—		0.80	1.20	1.50	
Analog RGB white peak slice level	TXV_{WPSR}	—	(Note T21)	2.30	2.55	2.80	V_{p-p}
	TXV_{WPSG}	—		2.30	2.55	2.80	
	TXV_{WPSB}	—		2.30	2.55	2.80	
Analog RGB black peak limit level	V_{BPSR}	—	(Note T22)	1.05	1.20	1.35	V
	V_{BPSG}	—		1.05	1.20	1.35	
	V_{BPSB}	—		1.05	1.20	1.35	
RGB contrast adjustment characteristic	Δv_{uTXR}	—	(Note T23)	15.5	16.5	18.5	dB
	Δv_{uTXG}	—		15.5	16.5	18.5	
	Δv_{uTXB}	—		15.5	16.5	18.5	
Analog RGB brightness adjustment characteristic	$V_{brTXmax}$	—	(Note T24)	3.0	3.2	3.4	V
	$V_{brTXcnt}$	—		2.5	2.7	2.9	
	$V_{brTXmin}$	—		2.0	2.2	2.4	
Analog RGB mode switch voltage	V_{TXON}	—	Pin 49	0.65	0.85	1.05	V
Analog RGB mode switching transfer characteristic	τ_{RYS}	—	(Note T25)	—	15	50	ns
	tP_{RYS}	—		—	20	50	
	Δt_{RYS}	—		—	0	10	
	τ_{FYS}	—		—	10	50	
	tP_{RYS}	—		—	30	50	
	Δt_{RYS}	—		—	0	10	
Text ACL characteristic	$TXACL_1$	—	(Note T26)	−2.00	−1.00	−0.05	dB
	$TXACL_2$	—		−7.5	−5.5	−3.5	
	$TXACL_3$	—		−6.0	−4.0	−2.0	
	$TXACL_4$	—		−17	−15	−13	
Analog OSD gain	G_{OSDR}	—	(Note T27)	2.95	3.30	3.70	times
	G_{OSDG}	—		2.95	3.30	3.70	
	G_{OSDB}	—		2.95	3.30	3.70	
Analog OSD gain triaxial difference	$G_{OSDG/R}$	—	—	0.94	1.00	1.06	—
	$G_{OSDB/R}$	—		0.94	1.00	1.06	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog OSD frequency characteristic	Gf_{OSDR}	—	At −3dB	35	40	—	MHz
	Gf_{OSDG}	—		35	40	—	
	Gf_{OSDB}	—		35	40	—	
Analog OSD input dynamic range	DR_{35}	—	—	0.80	1.20	1.50	V_{p-p}
	DR_{34}	—		0.80	1.20	1.50	
	DR_{33}	—		0.80	1.20	1.50	
Analog OSD input white peak slice level	$OSDV_{WPSR}$	—	(Note T28)	2.45	2.70	2.95	V_{p-p}
	$OSDV_{WPSG}$	—		2.45	2.70	2.95	
	$OSDV_{WPSB}$	—		2.45	2.70	2.95	
Analog OSD input black peak limit level	$OSDV_{BPSR}$	—	(Note T29)	1.30	1.45	1.60	V
	$OSDV_{BPSG}$	—		1.30	1.45	1.60	
	$OSDV_{BPSB}$	—		1.30	1.45	1.60	
Analog OSD contrast adjustment characteristic	$V_{UOSDR11}$	—	(Note T30)	0.58	0.64	0.71	V_{p-p}
	$V_{UOSDG11}$	—		0.58	0.64	0.71	
	$V_{UOSDB11}$	—		0.58	0.64	0.71	
	$V_{UOSDR10}$	—		0.47	0.53	0.59	
	$V_{UOSDG10}$	—		0.47	0.53	0.59	
	$V_{UOSDB10}$	—		0.47	0.53	0.59	
	$V_{UOSDR01}$	—		0.32	0.38	0.46	
	$V_{UOSDG01}$	—		0.32	0.38	0.46	
	$V_{UOSDB01}$	—		0.32	0.38	0.46	
	$V_{UOSDR00}$	—		0.21	0.23	0.25	
	$V_{UOSDG00}$	—		0.21	0.23	0.25	
	$V_{UOSDB00}$	—		0.21	0.23	0.25	
Analog OSD brightness adjustment characteristic	V_{brOSD0}	—	(Note T31)	2.20	2.40	2.60	V
	V_{brOSD1}	—		2.05	2.25	2.45	
	V_{brOSD2}	—		1.95	2.15	2.35	
	V_{brOSD3}	—		1.80	2.00	2.20	
Analog OSD mode switch voltage	V_{OSDON1}	—	Pin 51	2.05	2.30	2.55	V
	V_{OSDON2}	—	Pin 50	2.05	2.30	2.55	

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Analog OSD mode switching transfer characteristic	τ_{RYS1}	—	(Note T32)	—	15	50	ns
	tP_{RYS1}	—		—	20	50	
	ΔtP_{RYS1}	—		—	0	10	
	τ_{FYS1}	—		—	10	50	
	tP_{RYS1}	—		—	30	50	
	ΔtP_{RYS1}	—		—	0	10	
	τ_{RYS2}	—		—	15	50	
	tP_{RYS2}	—		—	20	50	
	ΔtP_{RYS2}	—		—	0	10	
	τ_{FYS2}	—		—	10	50	
	tP_{RYS2}	—		—	30	50	
	ΔtP_{RYS2}	—		—	0	10	
	t_{ROSD}	—		—	20	50	
	tP_{ROSD}	—		—	15	50	
	ΔtP_{ROSD}	—		—	0	10	
	τ_{FOSD}	—		—	20	50	
	tP_{ROSD}	—		—	20	50	
	ΔtP_{ROSD}	—		—	0	10	
OSD ACL characteristic	$OSDACL_1$	—	(Note T33)	—	0.00	—	dB
	$OSDACL_2$	—		—	0.00	—	
	$OSDACL_3$	—		−8.0	−5.5	−3.0	
	$OSDACL_4$	—		−17	−15	−13	
OSD blending characteristic	$\alpha 41TV_1$	—	(Note T34)	−7	−6	−5	dB
	$\alpha 42TV_1$	—		−7	−6	−5	
	$\alpha 43TV_1$	—		−7	−6	−5	
	$\alpha 41TV_2$	—		−4	−3	−2	
	$\alpha 42TV_2$	—		−4	−3	−2	
	$\alpha 43TV_2$	—		−4	−3	−2	
	$\alpha 41TV_3$	—		—	−55	−50	
	$\alpha 42TV_3$	—		—	−55	−50	
	$\alpha 43TV_3$	—		—	−55	−50	
	$\alpha 41OSD_1$	—		−6.5	−5.5	−4.5	
	$\alpha 42OSD_1$	—		−6.5	−5.5	−4.5	
	$\alpha 43OSD_1$	—		−6.5	−5.5	−4.5	
	$\alpha 41OSD_2$	—		−12.0	−10.5	−9.0	
	$\alpha 42OSD_2$	—		−12.0	−10.5	−9.0	
	$\alpha 43OSD_2$	—		−12.0	−10.5	−9.0	
	$\alpha 41OSD_3$	—		—	−40	−30	
	$\alpha 42OSD_3$	—		—	−40	−30	
	$\alpha 43OSD_3$	—		—	−40	−30	
Crosstalk between inputs	—	—	—	—	−50	−40	dB

Deflection Block

Parameter	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Sync input horizontal sync phase	S_{PH}	—	(Note HA01)	0.55	0.65	0.75	μs
HD 1/2 input horizontal sync phase	$HD_{1PH/2PH}$	—	(Note HA02)	0.58	0.68	0.78	μs
Polarity detection range	HD_{DUTY1}	—	(Note HA03)	—	0.5	2.0	%
	HD_{DUTY2}	—		62	67	72	
	HD_{DUTY3}	—		—	99.5	98	
	HD_{DUTY4}	—		47.5	52.5	57.5	
Sync input threshold amplitude	V_{thS00}	—	(Note HA04)	4	8.5	14	%
	V_{thS01}	—		14	20	26	
	V_{thS10}	—		24	30	36	
	V_{thS11}	—		34	40	46	
HD 1/2 input threshold voltage	$V_{thHD1/2}$	—	(Note HA05)	0.7	0.8	0.9	V_{p-p}
Horizontal picture phase adjustment variable range	ΔH_{SFT-}	—	(Note HA06)	9.5	10.5	11.5	%
	ΔH_{SFT+}	—		9.5	10.5	11.5	
Curve correction amount	$\Delta H_{\#23}$	—	(Note HA07)	2.9	3.4	3.9	%
Clamp pulse phase, width and level	CP_{S0}	—	(Note HA08)	3.1	3.8	4.5	%
	CP_{W0}	—		2.0	2.5	3.0	
	CP_{V0}	—		4.7	5.0	5.3	V
	CP_{S1}	—		0	0.7	1.5	%
	CP_{W1}	—		1.9	2.4	2.9	
	CP_{V1}	—		4.7	5.0	5.3	V
	CP_{S2}	—		3.2	4.2	5.2	%
	CP_{W2}	—		2.2	2.7	3.2	
	CP_{V2}	—		4.7	5.0	5.3	V
Black peak detection pulse phase and level	HBP_{S0a}	—	(Note HA09)	4.3	6.3	8.9	%
	HBP_{S0b}	—		4.3	6.3	8.9	
	HBP_{V0}	—		2.2	2.5	2.8	V
	HBP_{S1a}	—		1.5	3.5	5.9	%
	HBP_{S1b}	—		1.5	3.5	5.9	
	HBP_{V1}	—		2.2	2.5	2.8	V
	HBP_{s45a}	—		6.0	8.5	11.5	%
	HBP_{s45b}	—		6.0	8.5	11.5	%
	HBP_{sv45}	—		2.2	2.5	2.8	%
FBP threshold	V_{thFBP}	—	(Note HA10)	2.5	3.0	3.5	V
HVCO oscillation start voltage	V_{VCO}	—	Monitor pin 21 = V_{CC}	3.5	4.0	4.5	V
H-OUT start voltage	V_{HON}	—	Monitor pin 26 = V_{CC}	4.5	5.2	6.2	V

Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
H-OUT pulse duty		TH_{00A}	—	(Note HB01)	39	41	43	%
		TH_{01A}	—		38	40	42	
		TH_{10A}	—		38	40	42	
		TH_{00B}	—		45	47	49	
		TH_{01B}	—		44.5	46.5	48.5	
		TH_{10B}	—		45	47	49	
Horizontal free-running frequency		F00	—	(Note HB02)	15.59	15.75	15.91	kHz
		F01	—		31.19	31.5	31.82	
		F10	—		33.41	33.75	34.09	
		F11	—		44.52	45.0	45.48	
Horizontal oscillation frequency variable range		$F00_{MIN}$	—	(Note HB03)	14.48	14.78	15.08	kHz
		$F00_{MAX}$	—		16.37	16.70	17.03	
		$F01_{MIN}$	—		28.97	29.56	30.15	
		$F01_{MAX}$	—		32.72	33.39	34.06	
		$F10_{MIN}$	—		30.91	31.54	32.17	
		$F10_{MAX}$	—		34.91	35.62	36.33	
		$F11_{MIN}$	—		43.20	44.00	44.80	
		$F11_{MAX}$	—		47.85	48.65	49.45	
Horizontal oscillation control sensitivity		BH00	—	Hz/0.1 V (Note HB04)	176	220	264	—
		BH01	—		352	440	528	
		BH10	—		376	470	564	
		BH11	—		520	650	780	
H-OUT output voltage		$V26_H$	—	(Note HB05)	4.8	5.1	5.2	V
		$V26_L$	—		—	0.1	0.3	
Horizontal oscillation frequency pin (pin 22) control voltage threshold		$V22_L$	—	—	1.3	1.5	1.7	V
		$V22_M$	—		4.3	4.5	4.7	
		$V22_H$	—		7.3	7.5	7.7	
DAC switching voltage	DAC2	$VDAC_{2H}$	—	TEST = (00), DAC2 = (1)	8.5	9.0	—	
		$VDAC_{2L}$	—	TEST = (00), DAC2 = (0)	—	0.3	0.7	
VP output pulse width		VP_W	—	(Note V01)	4	4.5	5	H
Vertical free-running (maximum pull-in range)	000	VPt0	—		1278	1281	1284	H
	001	VPt1	—		846	849	852	
	010	VPt2	—		722	725	728	
	011	VPt3	—		657	660	663	
	100	VPt4	—		610	613	616	
	101	VPt5	—		360	363	366	
	110	VPt6	—		304	307	310	
Vertical minimum pull-in range		T_{VPULL}	—	(Note V02)	47	48	49	H

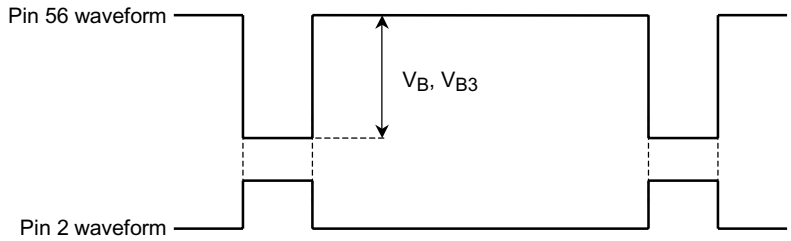
Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vertical black peak detection pulse	000	$VBPP_{0E}$	—	(Note V03)	51	52	53	H
		$VBPP_{0S}$	—		1099.5	1100.5	1101.5	
	001	$VBPP_{1E}$	—		51	52	53	
		$VBPP_{1S}$	—		729.5	730.5	731.5	
	010	$VBPP_{2E}$	—		49.5	50.5	51.5	
		$VBPP_{2S}$	—		599.5	600.5	601.5	
	011	$VBPP_{3E}$	—		49.5	50.5	51.5	
		$VBPP_{3S}$	—		544.5	545.5	546.5	
	100	$VBPP_{4E}$	—		51	52	53	
		$VBPP_{4S}$	—		499.5	500.5	501.5	
	101	$VBPP_{5E}$	—		51	52	53	
		$VBPP_{5S}$	—		289.5	290.5	291.5	
	110	$VBPP_{6E}$	—		51	52	53	
		$VBPP_{6S}$	—		239.5	240.5	241.5	
Vertical blanking stop phase		V_{BLKMIN}	—	(Note V04)	15	16	17	H
		V_{BLKMAX}	—		45	46	47	
VP output voltage	High	V_{27VPH}	—	Pin 27 voltage	4.6	5.0	5.4	V
	Low	V_{27VPL}	—		—	0.1	0.5	
Delay time from SYNC input to VP output		15.75 kHz	—	—	10.0	11.6	13.4	μs
		31.5 kHz	—		4.8	5.8	7.6	
		33.75 kHz	—		4.4	5.4	7.2	
		45 kHz	—		3.1	4.1	5.9	

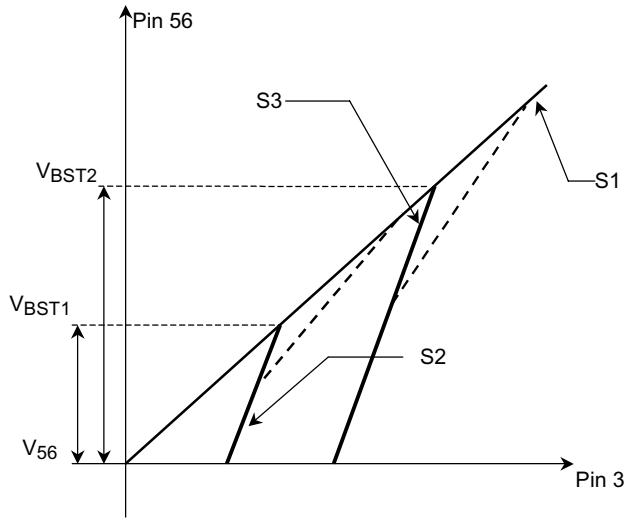
Parameter		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Compression BLK1 (start phase)	000	$CBLK1_{000min}$	—	—	1087	1088	1089	H
		$CBLK1_{000max}$	—		1117	1118	1119	
	001	$CBLK1_{001min}$	—		719	720	721	
		$CBLK1_{001max}$	—		749	750	751	
	010	$CBLK1_{010min}$	—		591	592	593	
		$CBLK1_{010max}$	—		621	622	623	
	011	$CBLK1_{011min}$	—		527	528	529	
		$CBLK1_{011max}$	—		557	558	559	
	100	$CBLK1_{100min}$	—		487	488	489	
		$CBLK1_{100max}$	—		517	518	519	
	101	$CBLK1_{101min}$	—		279	280	281	
		$CBLK1_{101max}$	—		309	310	311	
	110	$CBLK1_{110min}$	—		223	224	225	
		$CBLK1_{110max}$	—		253	254	255	
Compression BLK2 (stop phase)	000	$CBLK2_{000min}$	—	—	49	50	51	H
		$CBLK2_{000max}$	—		77	78	79	
	001	$CBLK2_{001min}$	—		49	50	51	
		$CBLK2_{001max}$	—		77	78	79	
	010	$CBLK2_{010min}$	—		49	50	51	
		$CBLK2_{010max}$	—		77	78	79	
	011	$CBLK2_{011min}$	—		49	50	51	
		$CBLK2_{011max}$	—		77	78	79	
	100	$CBLK2_{100min}$	—		49	50	51	
		$CBLK2_{100max}$	—		77	78	79	
	101	$CBLK2_{101min}$	—		49	50	51	
		$CBLK2_{101max}$	—		77	78	79	
	110	$CBLK2_{110min}$	—		49	50	51	
		$CBLK2_{110max}$	—		77	78	79	
External vertical blanking insert current	—	I_{EXTBLK}	—	Pin 27, current	520	625	780	μA

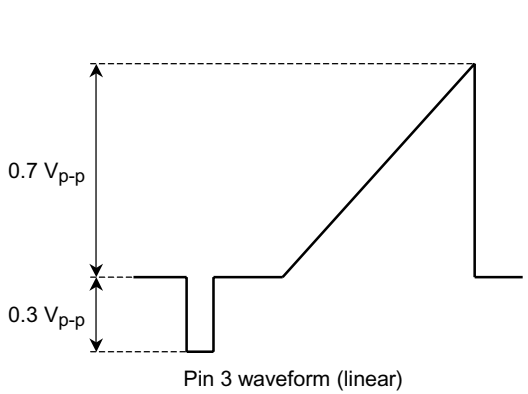
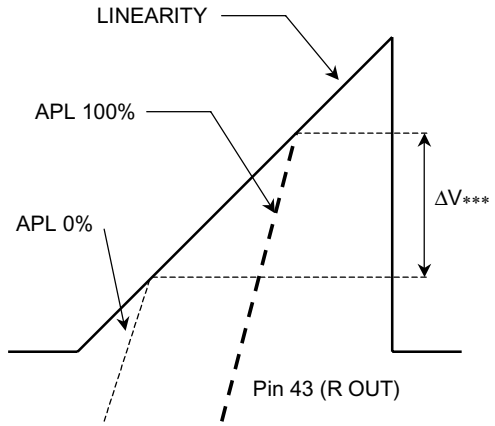
Test Conditions for Luminance

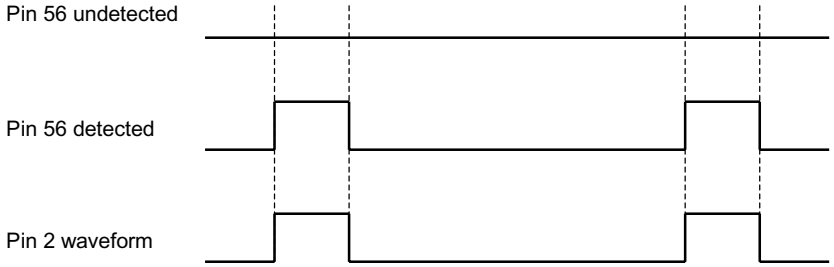
Common Test Conditions for Luminance

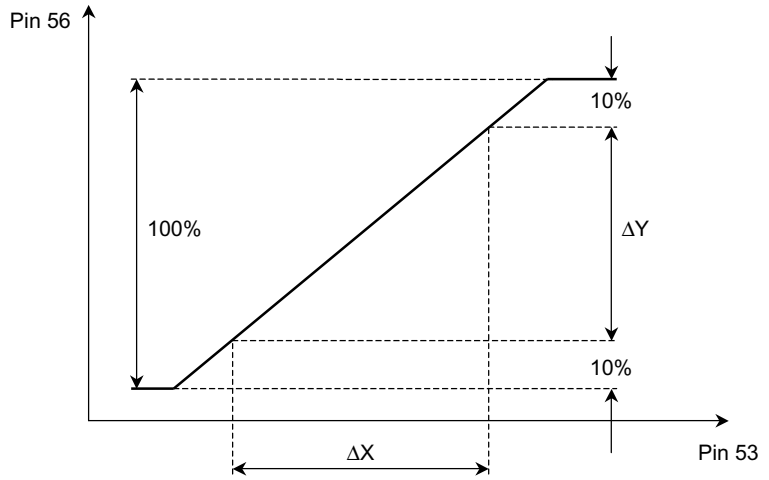
(1) SW4 = SW5 = B, SW7 = OPEN, SW8~SW10 = B, SW20 = ON, SW23 = B, SW33~SW39 = A, SW54 = 54 = ON
(2) After sending bus control data with preset values, set ACB MODE to off (00) and SYNC INPUT-SW to sync input (10).
(3) Input sync signal [signal in sync with input signal used for testing, except for sweep signal] to pin 14 (SYNC IN). Set horizontal frequency to that of pin 14.
(4) Set pin 7 to open, Y/color difference signal input mode (YUV INPUT MODE) to Through (10), SYNC SEP-LEVEL to 20% (01) and vertical free-running frequency to 307H (110).

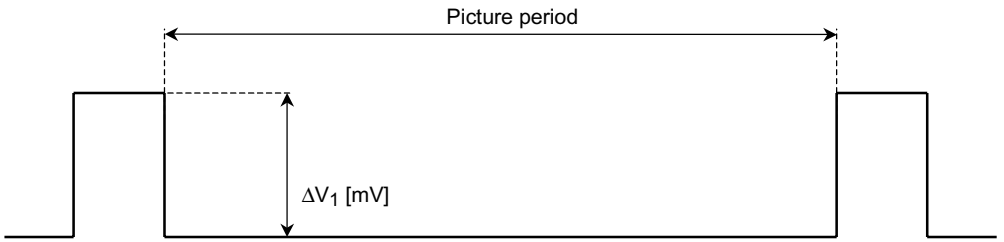
Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P01	Black detection level shift	B	C	C	OPEN	(1) Connect external power supply (PS) to pin 3 and monitor pins 2 and 56. (2) Set black stretch point 1 to off (000) and black detection level (BDL) to 0 IRE (1). (3) Increase PS voltage from 4.95 V in 1-mV steps. When pin 2 picture period (High) goes Low, measure pin 56 DC differential V_B. (4) Set black detection level (BDL) to 3 IRE (0). (5) Repeat step (3) above and measure pin 56 DC differential V_{B3}. 
P02	Black stretch amplifier maximum gain	B	A	A	OPEN	(1) Set SW2 to A (maximum gain) and input 500-kHz sine wave to TPA. (2) Adjust signal amplitude to 0.1 V_{p-p} using pin 3. (3) Set black stretch point 1 to off (000) and measure pin 56 amplitude V_A. (4) Set black stretch point 1 to 001 (black stretch on) and measure pin 56 amplitude V_B. (5) Calculate GBS using the following formula. $GBS = 20 \times \ell og \ (V_B \div V_A)$ [dB]

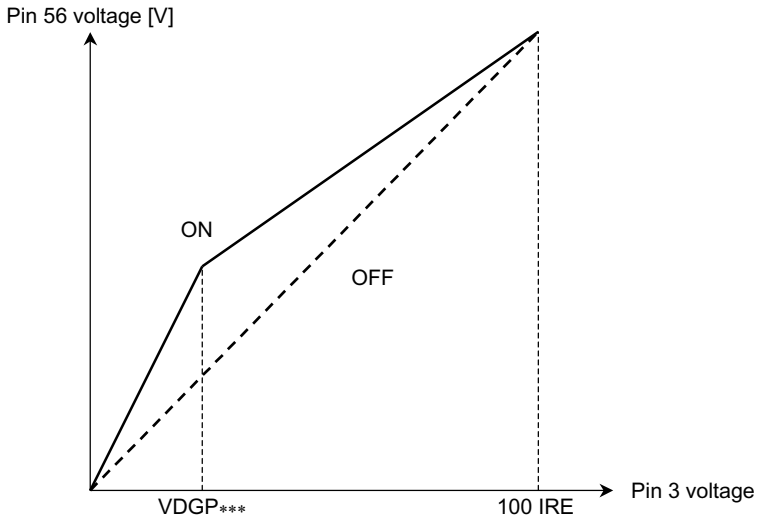
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P03	Black stretch start point 1	B	A	C	OPEN	(1) Set SW2 to A (maximum gain) and black stretch start point 1 to off (000). (2) Connect external power supply (PS) to pin 3, increase voltage from V_3, and plot resulting pin 56 voltage change S1. Define pin 56 voltages when V_3 and $V_3 + 0.7$ V are applied as V_0 and V_{100}. (3) Set black stretch start point 1 to 001 (minimum), increase PS voltage from V_3 as in (2) above and plot resulting pin 56 voltage change S2. (4) Set black stretch start point 1 to maximum (111), repeat step (2) above and plot resulting pin 56 voltage change S3. (5) Determine S1 and S2 intersection V_{BST1} and S1 and S3 intersection V_{BST2} using the graph below. Calculate P_{BST1} and P_{BST2} using the following formulae. V_Z [V] = V_{100} [V] – V_0 [V] P_{BST1} [(IRE)] = [(V_{BST1} [V] – V_{56} [V]) ÷ V_Z] × 100 (IRE) P_{BST2} [(IRE)] = [(V_{BST2} [V] – V_{56} [V]) ÷ V_Z] × 100 (IRE) 

Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P04	Black stretch start point 2	B	A	A	ON	(1) Set black stretch start point 1 to off (000), picture mute to off (P-MODE: Normal1 (000)) and apply 0 V to #1. Input TG7 linearity to TPA, adjust amplitude using pin 3 as shown below, set UNI-COLOR to center (1000000), then measure pin 43 (R OUT) amplitude V_{P43}. (2) Set black stretch start point 1 to 001 (black stretch on), connect external power supply (PS) to pin 56 and monitor pin 43 (R OUT). (3) When black stretch start point 2 data is a minimum (00), determine black stretch start point differential ΔV_{00} for PS = V_{56} (APL = 0%) and for PS = V_{56} + 1.0 V (APL = 100%), as shown below. (Using oscilloscope, adjust input waveform so that amplitude (gradient) is same as that of output waveform in VAR. Compare waveforms and determine point where output waveform bends.) (4) When black stretch start point 2 data is a maximum (11), determine black stretch start point differential ΔV_{11} as in (3) above. (5) Calculate using the following formulae. $P_{BS1} = (\Delta V_{00}/V_{P43}) \times 100$ $P_{BS2} = (\Delta V_{11}/V_{P43}) \times 100$  

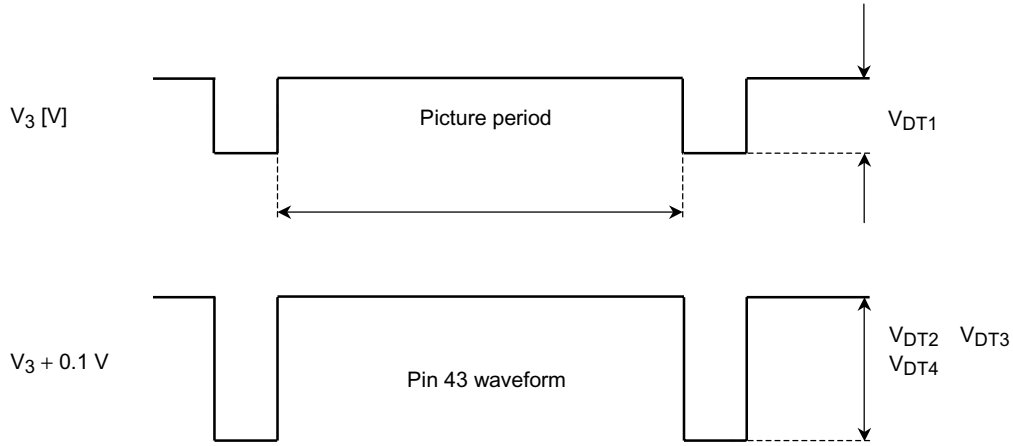
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P05	Dynamic ABL detection voltage	B	A	C	OPEN	(1) Set ABL GAIN to minimum (000), DYNAMIC ABL GAIN to maximum (111) and black stretch point 1 to off (000). (2) Connect external power supply (PS) to pin 53 and decrease voltage from 6.5 V. (3) When DYNAMIC ABL POINT bus data is 000, 001, 110 and 100, repeat step (2) above. When pin 56 picture period goes Low, measure PS voltages V_{000}, V_{001}, V_{010} and V_{100}. (4) Determine voltage differential between V_{000} and V_{001} (ΔV_{001}), between V_{000} and V_{010} (ΔV_{010}), and between V_{000} and V_{100} (ΔV_{100}). $DV_{***} = V_{000} - V_{001}$ (V_{010}, V_{100}) 

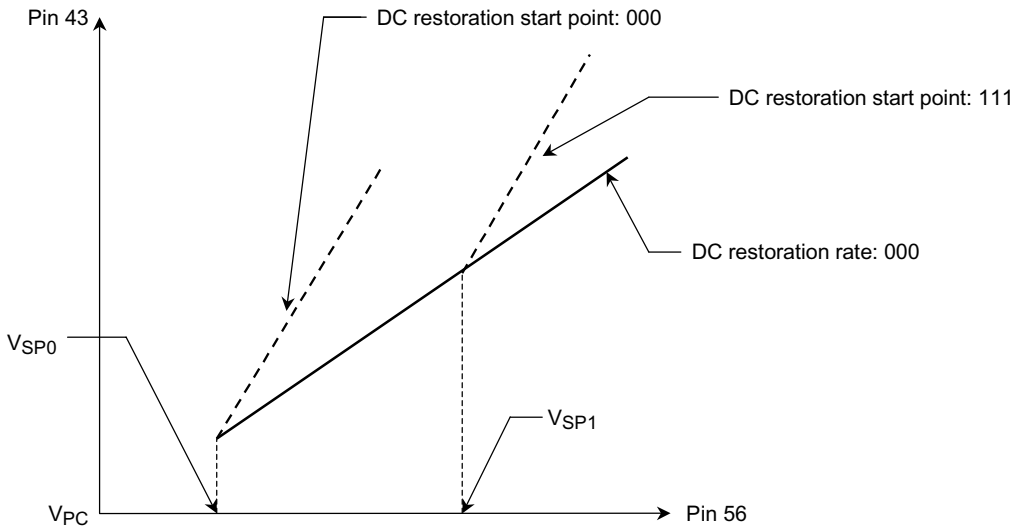
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P06	Dynamic ABL sensitivity	B	A	C	ON	(1) Set black stretch point 1 to off (000) and connect external power supply (PS) to pin 53. (2) When DYNAMIC ABL POINT is a minimum (000) and DYNAMIC ABL GAIN is a minimum (000) or a maximum (111), plot pin 53 voltage characteristic in relation to pin 56 voltage. (3) Determine gradients S_{DAMIN} and S_{DAMAX} using the graph below. $S_{DAMIN} = \Delta Y/\Delta X$ $S_{DAMAX} = \Delta Y/\Delta X$ 

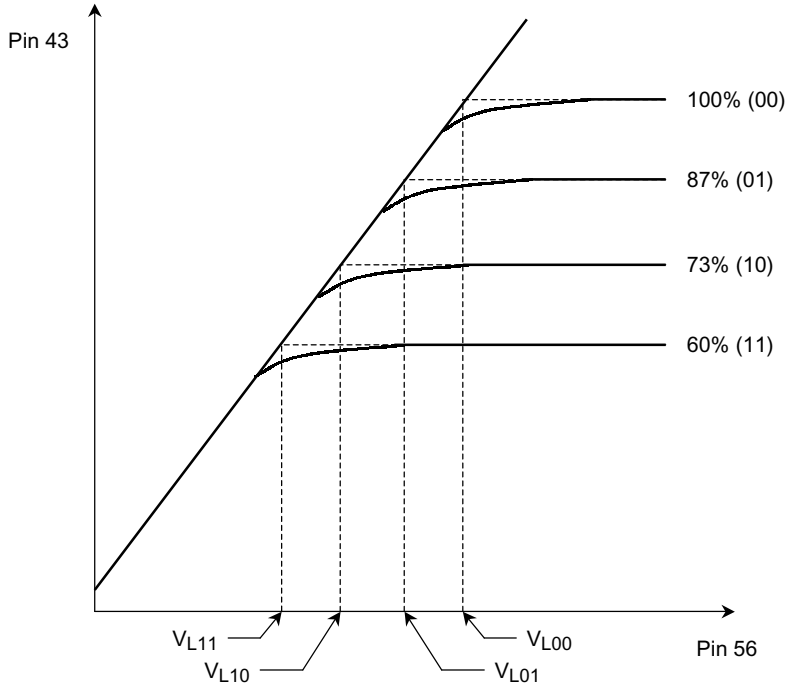
Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P07	Black level correction	B	A	C	OPEN	(1) Set black stretch point 1 to off (000) and monitor pin 56. (2) Set black level correction (BLC) to on (1), measure ΔV_1 (mV) and calculate BLC using the following formula. (V_Z: P09 value) $BLC = [\Delta V_1/(V_Z \times 10^3)] \times 100$ (IRE) 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P08	Dynamic Y γ correction point	A	B	A	OPEN	(1) Connect external power supply (PS1) to pin 3 and (PS2) to TP1. Set PS2 to 0 V. (2) Set dynamic Y γ point switch (DYNCγ-POINT) to 19 IRE (00), dynamic Y γ gain VS dark area (DYNCγ GAIN VS DARK AREA) to off (000) and dynamic Y γ dark area gain to off (00). (3) When PS1 is increased from V_3 to V_3 + 0.7 V, set V_3 to 0 V and plot voltage change in pin 56. (V_3 is pin voltage of pin 3.) (4) Set DYNCγ GAIN VS DARK AREA to maximum (111), static Y γ dark area gain (STATICγ-GAIN) to maximum (11) and PS2 to 1 V. (5) As in step (3) above, increase PS1 from V_3 to V_3 + 0.7 V and plot pin 56 voltage change. (6) Set DYNCγ-POINT to 21 IRE (01), 25 IRE (10) and 30 IRE (11), increase PS1 from V_3 to V_3 + 0.7 V and plot pin 56 voltage change. (7) Determine dynamic Y γ point when DYNCγ-POINT is set to 19 IRE (00) as V_{DGP00} using the graph below. Also determine dynamic Y γ point when DYNCγ-POINT is set to 21 IRE (01) as V_{DGP01}; to 25 IRE (10) as V_{DGP10}; to 30 IRE (10) as V_{DGP11}. (8) Using V_{DGP01}, V_{DGP10}, and V_{DGP11} thus determined, calculate P_{DGP00}, P_{DGP01}, P_{DGP10} and P_{DGP11} using the following formulae. $PDGP_{00} = (V_{DGP00}/0.7) \times 100$ $PDGP_{01} = (V_{DGP01}/0.7) \times 100$ $PDGP_{10} = (V_{DGP10}/0.7) \times 100$ $PDGP_{11} = (V_{DGP11}/0.7) \times 100$ $PDGPA = PDGP_{01} - PDGP_{00}$ $PDGPB = PDGP_{10} - PDGP_{00}$ $PDGPC = PDGP_{11} - PDGP_{00}$ 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P09	Dynamic Y γ gain	A	B	A	OPEN	(1) Connect external power supply (PS1) to pin 3 and (PS2) to TP1. Set PS2 to 0 V. (2) Set DYNCγ-POINT to 30 IRE (11), DYNCγ GAIN VS DARK AREA to off (000) and STATICγ-GAIN to off (00). (3) Set PS1 to V_3 and determine pin 56 voltage V_{DGOFF1}. (4) Set PS1 to V_3 + 0.16 V and determine pin 56 voltage V_{DGOFF2}. (5) Set DYNCγ GAIN VS DARK AREA to maximum (111), PS2 to 1 V and determine pin 56 voltage V_{GDON}. (6) Calculate G_{DG} using the following formula. $G_{DG} = 20 \times \ell og \ (V_{DGON} - V_{DGOFF1}/V_{DGOFF2} - V_{DGOFF1})$
P10	Static Y γ dark area gain	A	B	A	OPEN	(1) Connect external power supply (PS1) to pin 3 and (PS2) to TP1. Set PS2 to 0 V. (2) Set DYNCγ-POINT to 30 IRE (11), DYNCγ GAIN VS DARK AREA to off (000) and STATICγ-GAIN to off (00). (3) Set PS1 to V_3 and determine pin 56 voltage V_{SGOFF1}. (4) Set PS1 to V_3 + 0.16 V and determine pin 56 voltage V_{SGOFF2}. (5) Set STATICγ GAIN to maximum (11) and determine pin 56 voltage V_{SGON}. (6) Calculate G_{SG} using the following formula. $G_{SG} = 20 \times \ell og \ (V_{SGON} - V_{SGOFF1}/V_{SGOFF2} - V_{SGOFF1})$

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P11	DC restoration gain	B	B	C	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), DC restoration start point to minimum (000) and DC restoration limit point (DC REST LIMIT) to 100% (11) and connect external power supply PS1 to pin 3. (2) Measure DC level of pin 43 picture period. When use PS1 at V_3 as reference, Set PS1 to V_3 + 0.7 V and adjust DC level to 0.7 V using UNI-COLOR. (3) Set DC REST RATE to minimum (000) and measure V_{DT1} and V_{DT2} when pin 3 is at V_3 and at V_3 + 0.1 V (see figure below). (4) Measure V_{DT3} when pin 3 is at V_3 + 0.1 V. Set DC REST RATE to maximum (111) and measure V_{DT3}. (5) Set DC restoration rate switch (DCRR-SW) to 100% or less (1) and pin 3 to V_3 + 0.1 V, and measure V_{DT4}. Set DC REST RATE to maximum (111) and measure V_{DT4}. (6) Calculate ADT_{100}, ADT_{135} and ADT_{65} using the following formulae. $ADT_{100} = (V_{DT2}\ [V] - V_{DT1}\ [V]) \div 0.1\ [V]$ $ADT_{135} = (V_{DT3}\ [V] - V_{DT1}\ [V]) \div 0.1\ [V]$ $ADT_{65} = 1 - \{(V_{DT2}\ [V] - V_{DT4}\ [V]) \div 0.1\ [V]\}$ 

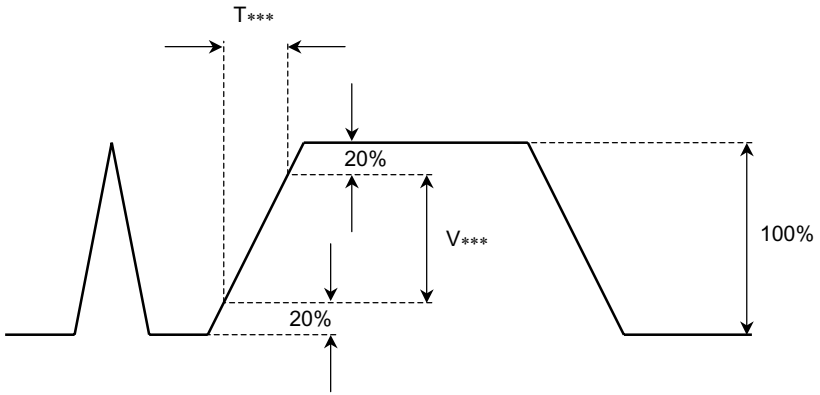
Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P12	DC restoration start point	B	B	C	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), DC restoration start point to minimum (000) and DC REST LIMIT to 100% (11), and connect external power supply PS1 to pin 3. (2) Measure DC level of pin 43 picture period. Use PS1 at V_3 as reference. When PS1 is set to V_3 + 0.7 V, adjust DC level to +1.0 V using UNI-COLOR. (3) Set DC REST RATE to minimum (000), increase PS1 from V_3 and plot voltage relationship between pin 56 (DC voltage) and pin 43 (picture period voltage). (4) Set DC REST RATE to maximum (111), increase PS1 from V_3 and plot voltage relationship between pins 56 and 43. (5) Set DC REST RATE to maximum (111), DC restoration start point to maximum (111), increase PS1 from V_3 and plot voltage relationship between pins 56 and 43. (6) Calculate V_{DT0} and V_{DT1} using the following formulae. $V_{DT0} = [(V_{SP0} - V_{56})/1\ V] \times 100\%$ $V_{DT1} = [(V_{SP1} - V_{56})/1\ V] \times 100\%$ 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P13	DC restoration limit point	B	B	C	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111) and DC restoration start point to minimum (000), and connect external power supply PS to pin 56. (2) Set DC REST RATE to maximum (111). (3) Increase PS from 5 V, monitor pin 43 and plot DC restoration. (4) Change DC REST LIMIT and repeat step (3) above. Determine V_{L11}, V_{L10}, V_{L01} and V_{L00} using the graph below. Calculate P_{DTL11}, P_{DTL10}, P_{DTL01} and P_{DTL00} using the following formulae. $P_{DTL11} = [(V_{L11} - V_{56})/1.0] \times 100\%$ $P_{DTL10} = [(V_{L10} - V_{56})/1.0] \times 100\%$ $P_{DTL01} = [(V_{L01} - V_{56})/1.0] \times 100\%$ $P_{DTL00} = [(V_{L00} - V_{56})/1.0] \times 100\%$ 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P14	Sharpness control range	B	B	A	ON	(1) Input sine wave (frequency variable) to TPA. (2) Set pin 3 amplitude to 20 mV_{P-P}. (3) Set UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11), APACON peak frequency (APACON PEAK f_0) to 15 M (00) and color detail enhancer (CDE) to center (10). (4) Set picture mute to off (P-MODE: Normal1 (000)) and monitor pin 43. (5) Set picture sharpness (PICTURE-SHARPNESS) to center (1000000) and measure amplitude V_{100} when input frequency is 100 kHz. (6) Set PICTURE-SHARPNESS to maximum (1111111) and measure amplitude V_{MAX00} when input frequency is F_{AP00}. Calculate G_{MAX00} using the following formula. (7) Set PICTURE-SHARPNESS to minimum (0000000) and measure amplitude V_{MIN00} when input frequency is F_{AP00}. Calculate G_{MIN00} using the following formula. (8) Set APACON PEAK f_0 to 8.8 M (01) and measure amplitudes V_{MAX01} and V_{MIN01} as in steps (6) and (7) when input frequency is F_{AP01}. Calculate G_{MAX01} and G_{MIN01} using the following formulae. (9) Set APACON PEAK f_0 to 7.5 M (10) and measure amplitudes V_{MAX10} and V_{MIN10} as in steps (6) and (7) when input frequency is F_{AP10}. Calculate G_{MAX10} and G_{MIN10} using the following formulae. (10) Set APACON PEAK f_0 to 5 M (11) and measure amplitudes V_{MAX11} and V_{MIN11} as in steps (6) and (7) when input frequency is F_{AP11}. Calculate G_{MAX11} and G_{MIN11} using the following formulae. $G_{MAX***} = 20 \times \ell og \ (V_{MAX***} \div V_{100})$ [dB] $G_{MIN***} = 20 \times \ell og \ (V_{MIN***} \div V_{100})$ [dB] *: When using a spectrum analyzer for monitoring, measure gain for low frequency.

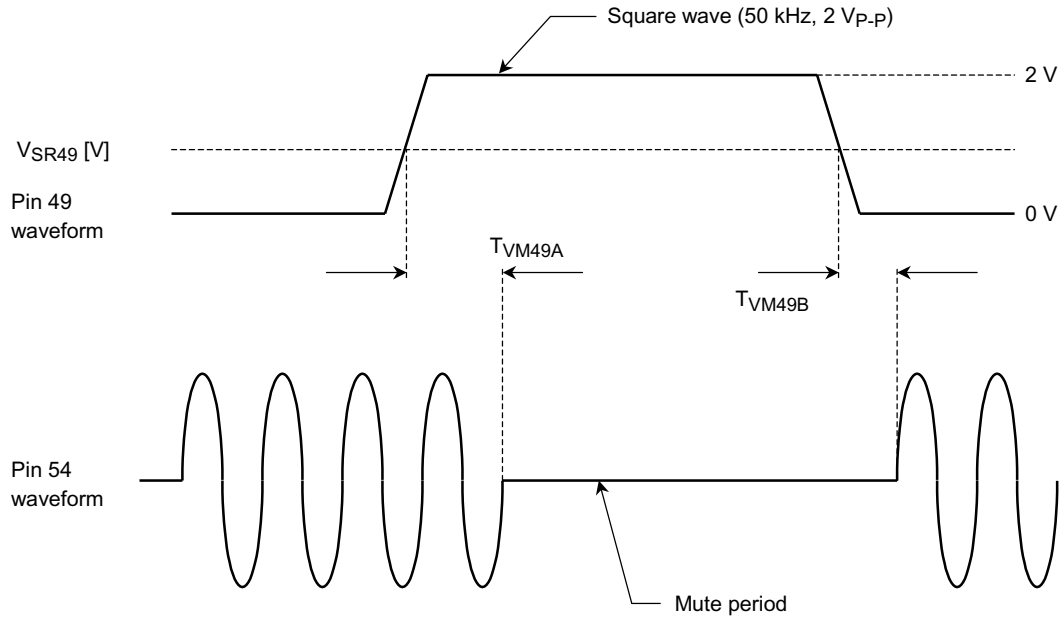
Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P15	Sharpness control center characteristic	B	B	A	ON	(1) Input sine wave (frequency variable) to TPA. (2) Set pin 3 amplitude to 20 mV_{P-P}. (3) Set UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11), APACON peak frequency (APACON PEAK f_0) to 15 M (00) and color detail enhancer (CDE) to center (10). (4) Set picture mute to off (P-MODE: Normal1 (000)) and monitor pin 43. (5) Set PICTURE-SHARPNESS to center (1000000) and measure amplitude V_{100} when input frequency is 100 kHz. (6) Measure pin 43 amplitude V_{CEN00} when input frequency is F_{AP00} with PICTURE-SHARPNESS set to center (1000000). Calculate G_{CEN00} using the following formula. (7) Set APACON PEAK f_0 to 8.8 M (01) and measure amplitude V_{CEN01} as in step (6) when input frequency is F_{AP01}. Calculate G_{CEN01} using the following formula. (8) Set APACON PEAK f_0 to 7.5 M (10) and measure amplitude V_{CEN10} as in step (6) when input frequency is F_{AP10}. Calculate G_{CEN10} using the following formula. (9) Set APACON PEAK f_0 to 5 M (11) and measure amplitudes V_{CEN11} as in step (6) when input frequency is F_{AP11}. Calculate G_{CEN11} using the following formula. $G_{CEN***} = 20 \times \ell og \ (V_{CEN***} \div V_{100})$ [dB] *: When using a spectrum analyzer for monitoring, measure gain for low frequency.

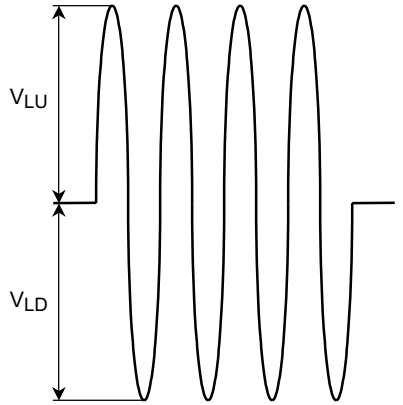
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P16	YNR characteristic	B	B	A	ON	(1) Input sine wave (frequency variable) to TPA. (2) Set pin 3 amplitude to 20 mV_{P-P}. (3) Set UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11), APACON peak frequency (APACON PEAK f_0) to 15 M (00) and color detail enhancer (CDE) to center (10). (4) Set picture mute to off (P-MODE: Normal1 (000)) and monitor pin 43. (5) Set PICTURE-SHARPNESS to center (1000000) and measure amplitude V_{100} when input frequency is 100 kHz. (6) Set YNR to on (1) and PICTURE-SHARPNESS to minimum (0000000). Measure pin 43 amplitude V_{TRAP00} when input frequency is F_{AP00} and calculate G_{YNRT00} using the following formula. (7) When PICTURE-SHARPNESS is set to 0000011 and measure pin 43 amplitude V_{FLAT00}. Calculate G_{YNRF00} using the following formula. (8) Set APACON PEAK f_0 to 8.8 M (01) and measure amplitude V_{TRAP01} as in step (7) when input frequency is F_{AP01}. Calculate G_{TRAP01} using the following formula. (9) Set APACON PEAK f_0 to 7.5 M (10) and measure amplitude V_{TRAP10} as in step (7) when input frequency is F_{AP10}. Calculate G_{TRAP10} using the following formula. (10) Set APACON PEAK f_0 to 5 M (11) and measure amplitude V_{TRAP11} as in step (7) when input frequency is F_{AP11}. Calculate G_{TRAP11} using the following formula. $G_{YNRT**} = 20 \times \ell og \ (V_{TRAP**}/V_{100})$ [dB] $G_{YNRF**} = 20 \times \ell og \ (V_{FLAT**}/V_{100})$ [dB] *: When using a spectrum analyzer for monitoring, measure gain for low frequency.

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P17	Control of SRT response to 2T pulse input	B	B	A	ON	(1) Input 2T pulse (0.7 V_{P-P}) signal to TPA and set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111), and SHR-TRACKING to SRT-GAIN minimum (11), CDE to center (10) and PICTURE-SHARPNESS to center (1000000). (2) Set APACON frequency to 15 M (00) and monitor pin 43. (3) Measure $T_{SRTMIN00}$ and $V_{SRTMIN00}$ as shown in the figure below. (4) Set SHR-TRACKING to SRT-GAIN maximum (00) and measure $T_{SRTMAX00}$ and $V_{SRTMAX00}$. (5) Set APACON frequency to 8.8 M (01), SHR-TRACKING to SRT-GAIN minimum (11) and maximum (00) as in step (4) above, and measure $T_{SRTMIN01}$, $V_{SRTMIN01}$, $T_{SRTMAX01}$ and $V_{SRTMAX01}$. (6) Set APACON frequency to 7.5 M (10), SHR-TRACKING to SRT-GAIN minimum (11) and maximum (00) as in step (4) above, and measure $T_{SRTMIN10}$, $V_{SRTMIN10}$, $T_{SRTMAX10}$ and $V_{SRTMAX10}$. (7) Set APACON frequency to 5 M (11), SHR-TRACKING to SRT-GAIN minimum (11) and maximum (00) as in step (4) above, and measure $T_{SRTMIN11}$, $V_{SRTMIN11}$, $T_{SRTMAX11}$ and $V_{SRTMAX11}$. (8) Calculate using the following formulae. $T_{SRT00} = 20 \times \ell og\ [((V_{SRTMAX00}/T_{SRTMAX00})/(V_{SRTMIN00}/T_{SRTMIN00})]$ $T_{SRT01} = 20 \times \ell og\ [(V_{SRTMAX01}/T_{SRTMAX01})/(V_{SRTMIN01}/T_{SRTMIN01})]$ $T_{SRT10} = 20 \times \ell og\ [(V_{SRTMAX10}/T_{SRTMAX10})/(V_{SRTMIN10}/T_{SRTMIN10})]$ $T_{SRT11} = 20 \times \ell og\ [(V_{SRTMAX11}/T_{SRTMAX11})/(V_{SRTMIN11}/T_{SRTMIN11})]$ 

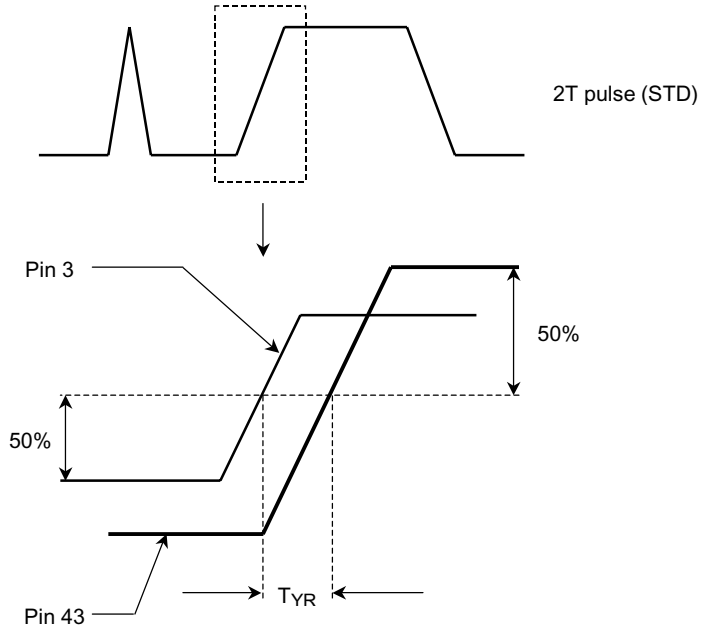
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P18	VSM gain	B	B	A	ON	(1) Input sine wave of frequency F_{VSM2} to TPA. (2) Set picture mute to off (P-MODE: Normal1 (000)), and pin 3 amplitude to 0.02 V_{P-P}. (3) Vary VSM GAIN from off (000) to maximum (111) and measure pin 54 amplitudes V_{001}, V_{010}, V_{011}, V_{100}, V_{101}, V_{110} and V_{111}. Set input amplitude to 0.7 V_{P-P} and measure pin 54 amplitude V_{000} when VSM GAIN is OFF (000). (4) Calculate using the following formulae. $G_{V000} = 20 \times \ell og\ (V_{000}/0.7)$ [dB] $G_{V001} = 20 \times \ell og\ (V_{001}/0.02)$ [dB] $G_{V010} = 20 \times \ell og\ (V_{010}/0.02)$ [dB] $G_{V011} = 20 \times \ell og\ (V_{011}/0.02)$ [dB] $G_{V100} = 20 \times \ell og\ (V_{100}/0.02)$ [dB] $G_{V101} = 20 \times \ell og\ (V_{101}/0.02)$ [dB] $G_{V110} = 20 \times \ell og\ (V_{110}/0.02)$ [dB] $G_{V111} = 20 \times \ell og\ (V_{111}/0.02)$ [dB]

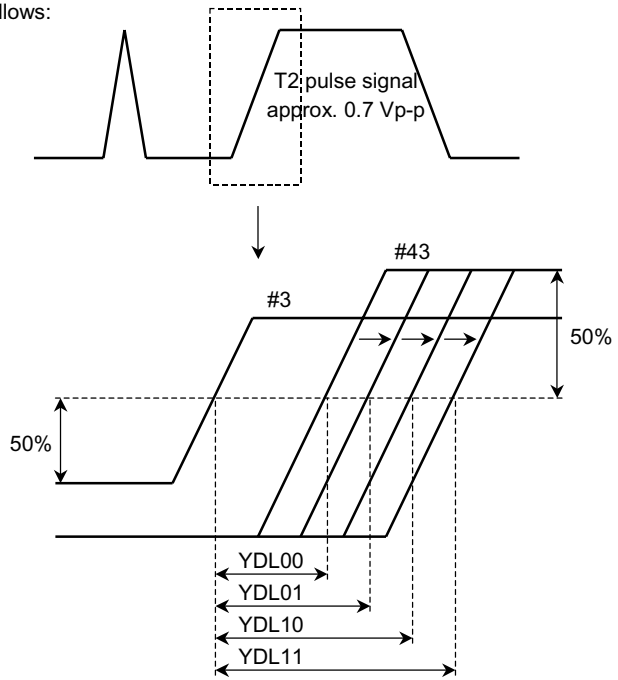
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P19	Response time for VSM fast muting	B	B	A	ON	(1) Input sine wave of frequency F_{VSM} to TPA. (2) Set picture mute to off (P-MODE: Normal1 (000)), VSM GAIN to 100 and pin 3 amplitude to 0.1 V_{P-P}. Monitor pin 54. (3) Input pulse as shown below to pin 49 and determine response times T_{VM49A} and T_{VM49B}. (4) Likewise input pulse to pin 50 and determine response times T_{VM50A} and T_{VM50B}. (5) Likewise input pulse to pin 51 and determine response times T_{VM51A} and T_{VM51B}.

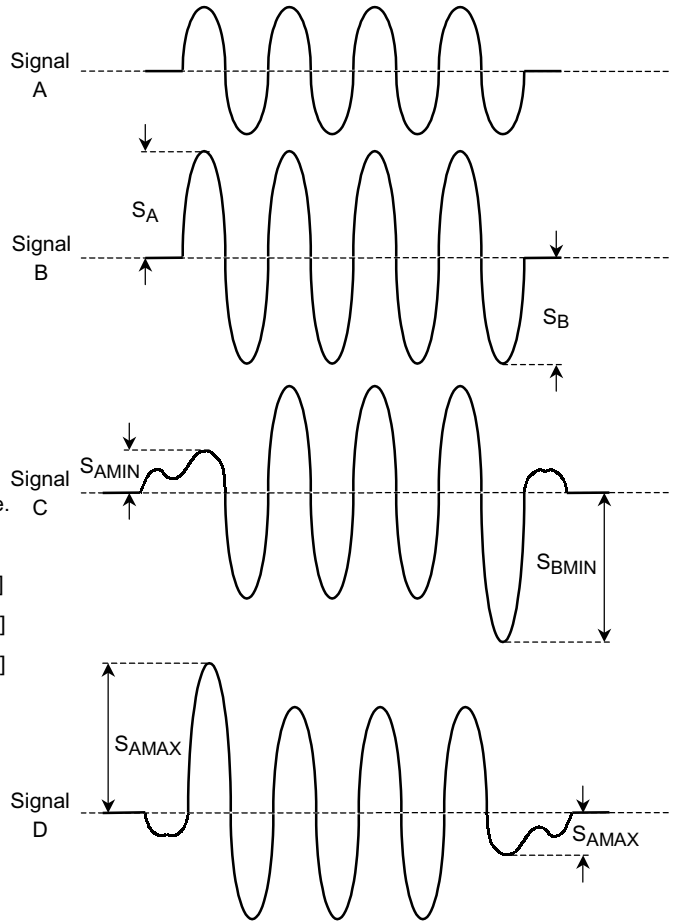


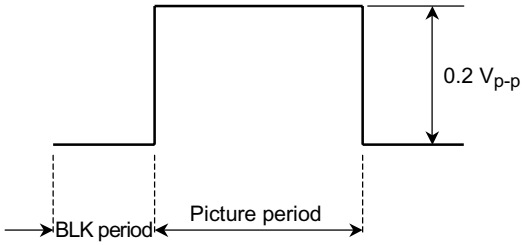
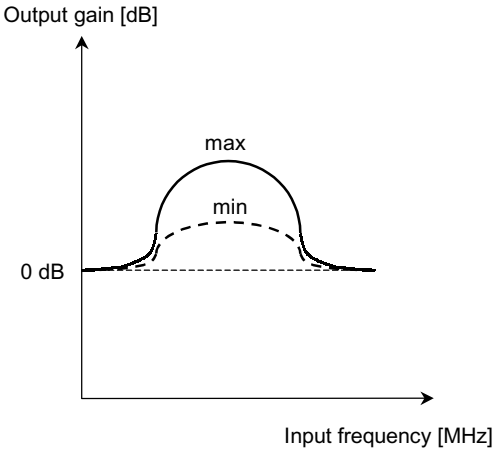
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P20	VSM limit	B	B	A	ON	(1) Input sine wave of frequency F_{VSM2} to TPA. (2) Set picture mute to off (P-MODE: Normal1 (000)), VSM GAIN to 111 and pin 3 amplitude to 0.7 V_{P-P}. (3) Measure pin 54 amplitudes V_{LU} and V_{LD} [V_{P-P}] as shown below. 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P21	Delay time from Y input to R output	B	B	A	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11) and input 2T pulse signal (STD) to TPA. (2) Set PICTURE-SHARPNESS to center (1000000). (3) Determine T_{YR} by monitioring pins 43 and 3 as shown below.

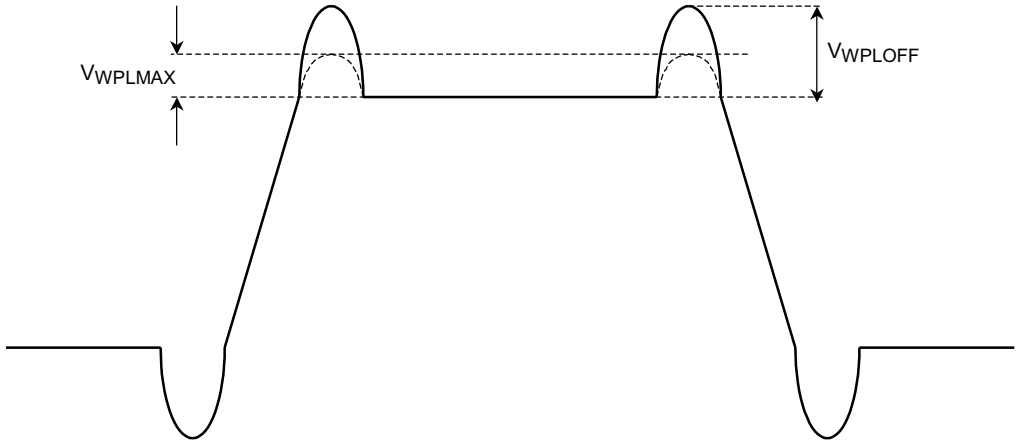


Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P22	Y delay time change	B	B	A	ON	(1) Set picture mute to off (P-MODE: Normal1, 000), UNI-COLOR to maximum (1111111) and SHR-TRACKING to SRT-GAIN minimum (11), and input T2 pulse signal (approx. 0.7 Vp-p) to TPA. (2) Set picture sharpness to center (1000000). (3) Monitor pin 3 and pin 43, and determine the time difference YDL00 for each signal at the 50% point as shown below. (4) Set Y/C-DL1 to +5 ns (1) and determine YDL01. (5) Set Y/C-DL1 to +0 ns (0) and Y/C-DL2 to +10 ns (1), and determine YDL10. (6) Set Y/C-DL1 to +5 ns (1) and Y/C-DL2 to +10 ns (1), and determine YDL11. (7) Determine YDLA, YDLB and YDLC as follows: YDLA = YDL01 − YDL00 YDLB = YDL10 − YDL00 YDLC = YDL11 − YDL00 

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P23	Transfer distortion correction	B	B	A	ON	(1) Input multi-burst signal (frequency equivalent to 4.2 MHz) of signal A to TPA. Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11) and CDE to minimum (00). (2) Set PICTURE-SHARPNESS to flat (near DEC[24]), APACON PEAK f_0 to 5 M (11) and monitor pin 43. (3) Input sine wave signal A (approx. 4.2 MHz) becomes signal B on pin 43 as shown at right. Determine S_A and S_B. (4) When Y-GROUP DELAY CORRECTION is set to minimum (0000), signal A becomes signal C on pin 43. Determine S_{AMIN} and S_{BMIN}. (5) When Y-GROUP DELAY CORRECTION is set to maximum (1111), signal A becomes signal D on pin 43. Determine S_{AMAX} and S_{BMAX}. (6) Calculate using the following formulae. $G_{AMIN} = 20 \times \ell og\ (S_{AMIN}/S_A)$ [dB] $G_{BMIN} = 20 \times \ell og\ (S_{BMIN}/S_B)$ [dB] $G_{AMAX} = 20 \times \ell og\ (S_{AMAX}/S_A)$ [dB] $G_{BMAX} = 20 \times \ell og\ (S_{BMAX}/S_B)$ [dB]  Note: The input sine wave starts and ends within the picture period. It is like a burst signal, not a continuous wave.

Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW1	SW2	SW3	SW56	
P24	Color detail enhancer	B	B	A	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11), COLOR to center (1000000), color limiter level (CLT) to 2 Vp (1) and C-SRT-FREQ to 4.5 M (10). Input SWEEP signal to TPA and set pin 3 amplitude to 20 mV_{P-P}. Set SW4 to A. Input signal (pin 4 amplitude: 0.2 V_{P-P}) to TP4 as shown in the figure below. (2) Set PICTURE-SHARPNESS to center (1000000) and Y DETAIL CONTROL to center (10000), and monitor pin 41 using a spectrum analyzer. (3) Set low-frequency area to 0dB when CDE is set to minimum (00) and measure peak level G_{CDEMIN}. (4) Set low-frequency area to 0dB when CDE is set to maximum (11) and measure peak level G_{CDEMAX}. (5) Calculate using the following formula. $G_{CDE00} = G_{CDEMAX00} - G_{CDEMIN00}$ (6) Set APACON PEAK f_0 to 15 M (00), 8.8 M (01), 7.5 M (10) and 5 M (11), and measure peak levels G_{CDE00}, G_{CDE01}, G_{CDE10} and G_{CDE11}.  

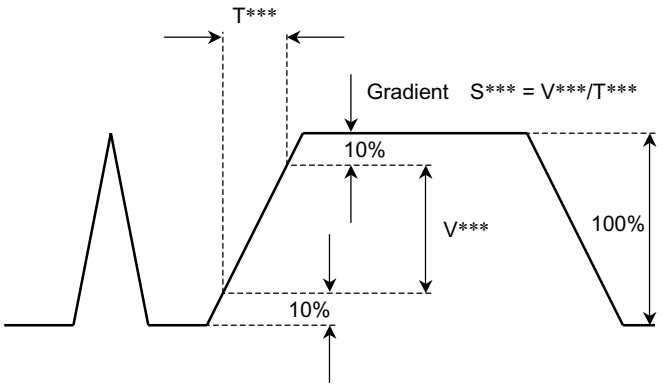
Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P25	Y detail control range	B	B	A	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to maximum (1111111), SHR-TRACKING to SRT-GAIN minimum (11) and CDE to center (10). Input SWEEP signal to TPA. (2) Set pin 3 amplitude to 20 mV_{P-P}. (3) Set PICTURE-SHARPNESS to minimum (0000000) and Y DETAIL CONTROL to maximum (11111), and monitor pin 43 using a spectrum analyzer. (4) Set low-frequency area to 0dB. Set APACON PEAK f_0 to 15 M (00), 8.8 M (01), 7.5 M (10) and 5 M (11), and measure peak levels $G_{YDMAX00}$, $G_{YDMAX01}$, $G_{YNMAX10}$ and $G_{YDMAX11}$. (5) Set Y DETAIL CONTROL to center (10000) and measure peak levels $G_{YDCEN00}$, $G_{YDCEN01}$, $G_{YDCEN10}$ and $G_{YDCEN11}$. (6) Set Y DETAIL CONTROL to minimum (00000) and measure peak levels $G_{YDMIN00}$, $G_{YDMIN01}$, $G_{YNDIN10}$ and $G_{YDMIN11}$.

Note No.	Parameter	Test Conditions SW mode SW1	SW2	SW3	SW56	Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
P26	APACON white peak limiter	B	B	A	ON	(1) Set picture mute to off (P-MODE: Normal1 (000)), UNI-COLOR to 1101000, SHR-TRACKING to SRT-GAIN maximum (00) and CDE to maximum (11). Input T pulse signal (0.7 V_{P-P}) to TPA. (2) Set PICTURE-SHARPNESS to maximum (111111) and APACON PEAK f_0 to 5 M (11), and monitor pin 43. (3) When APACON white peak limiter is off (000), measure positive spike amplitude $V_{WPLOFF1}$. (4) When APACON white peak limiter is at maximum (111), measure positive spike amplitude $V_{WPLMAX1}$. (5) Set UNI-COLOR to center (1000000). When APACON white peak limiter is off (000) and at maximum (111), measure positive spike amplitudes $V_{WPLOFF2}$ and $V_{WPLMAX2}$. (6) Set UNI-COLOR to minimum (0000000). When APACON white peak limiter is off (000) and at maximum (111), measure positive spike amplitudes $V_{WPLOFF3}$ and $V_{WPLMAX3}$. (7) Calculate using the following formulae. $G_{WPL1} = 20 \times \ell og\ (V_{WPLMAX1}/V_{WPLOFF1})$ [dB] $G_{WPL2} = 20 \times \ell og\ (V_{WPLMAX2}/V_{WPLOFF2})$ [dB] $G_{WPL3} = 20 \times \ell og\ (V_{WPLMAX3}/V_{WPLOFF3})$ [dB] 

Test Conditions for Color Difference Signal 1/YUV Input and Matrix

Common Test Conditions for Color Difference Signal 1/YUV Input and Matrix

(1) SW1 = B, SW2 = B, SW20 = ON, SW33~SW39 = A, SW54 = OPEN, SW56 = OPEN
(2) Send BUS control data with preset values.
(3) Set ACB MODE to off (0) and high bright color (HI BRT) to off (0).
(4) Input sync signal [signal in sync with input signal for testing, except for SWEEP signal] to pin 14 (SYNC IN) and set SYNC-INPUT to (10).

Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW3	SW4	SW5	SW7	
S01	Color SRT gain	C	A	A	OPEN	(1) Set Y mute to on (P-MODE: Y-MUTE (001)), YUV INPUT MODE to Through (10), BRIGHTNESS to center (10000000), COLOR to center (1000000) and UNI-COLOR to maximum (1111111).
		SW8	SW9	SW10	—	(2) Input 2T pulse signal to TP4 and set pin 4 amplitude to 350 mV_{P-P}.
		B	B	B	—	(3) Monitor pin 41 output waveform. When C-SRT-FREQ is 5 MHz (00), measure edge gradients SB00MIN, SB00CEN and SB00MAX when COLOR SRT GAIN is at minimum (000), center (100) and maximum (111) as in shown in the figure below. Set SB00MIN to 0 dB, determine $GS_{B00CEN} = 20 \times \ell og$ (SB00CEN/SB00MIN) and $GS_{B00MAX} = 20 \times \ell og$ (SB00MAX/SB00MIN).
						(4) Repeat step (3) above, setting C-SRT-FREQ to 6.7 MHz (01) and 10 MHz (10), and measure edge gradients when COLOR SRT GAIN is at minimum (000), center (100) and maximum (111). Determine GS_{B01CEN}, GS_{B10CEN}, GS_{B01MAX} and GS_{B10MAX}.
						(5) Input 2T pulse signal to TP5 and set pin 5 amplitude to 350 mV_{P-P}.
						(6) Monitor pin 43 output waveform. When C-SRT-FREQ is 5 MHz (00), measure edge gradients SR00MIN, SR00CEN and SR00MAX when COLOR SRT GAIN is at minimum (000), center (100) and maximum (111) as shown in the figure below. Set SR00MIN to 0dB, determine $GS_{R00CEN} = 20 \times \ell og$ (SR00CEN/SR00MIN) and $GS_{R00MAX} = 20 \times \ell og$ (SR00MAX/SR00MIN).
						(7) Repeat step (3) above, setting C-SRT-FREQ to 6.7 MHz (01) and 10 MHz (10), and measure edge gradients when COLOR SRT GAIN is at minimum (000), center (100) and maximum (111). Determine GS_{R01CEN}, GS_{R10CEN}, GS_{R01MAX} and GS_{R10MAX}. 

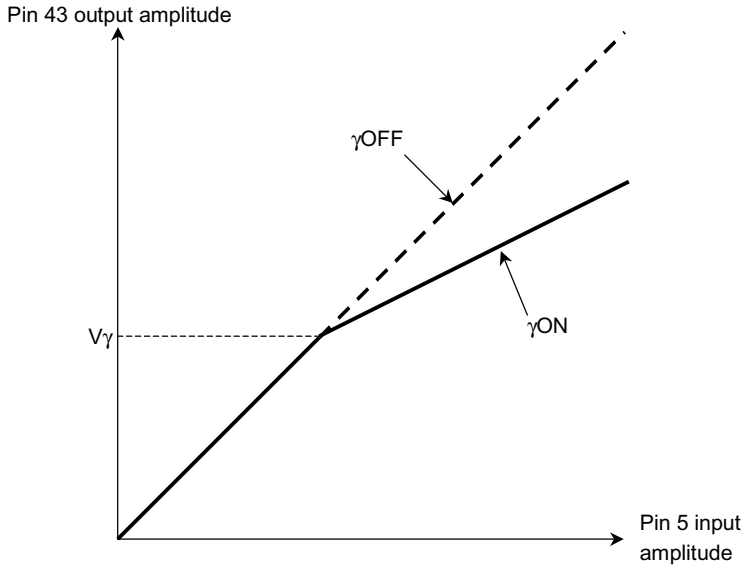
Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW3	SW4	SW5	SW7	
S02	Color difference signal amplitude correction	C	A	A	OPEN	(1) Input 100-kHz sine wave to TP4 and set pin 4 amplitude to 0.2 V_{P-P}.
		SW8	SW9	SW10	SW56	(2) Set Y mute to OFF (P-MODE: Normal1 (000)), YUV INPUT MODE to Through (10), BRIGHTNESS to center (10000000), COLOR to center (1000000), UNI-COLOR to maximum (1111111), Y/C GAIN COMP1 to minimum (00), Y/C GAIN COMP2 to minimum (00), black stretch point 1 to off (000), dynamic Y γ point to 30 IRE (11) and SW1 to A. Apply 0 V to TP1 using external power supply PS1 and 5.16 V to pin 3 using PS2.
		B	B	B	OPEN	(3) Monitor pin 41 output waveform and measure amplitude VBDY0.
						(4) Set Y/C GAIN COMP1 to maximum (11) and measure pin 41 amplitude VBDY1.
						(5) Set DYNCγ GAIN VS DARK AREA to maximum (111), STATICγ-GAIN to maximum (11) and external power supply PS1 to 1 V, and measure pin 41 amplitude VBDY2.
						(6) Set Y/C GAIN COMP2 to maximum (11) and measure pin 41 amplitude VBDY3.
						(7) Set Y/C GAIN COMP1 to minimum (00), Y/C GAIN COMP2 to minimum (00), DYNCγ GAIN VS DARK AREA to minimum (000), STATICγ-GAIN to minimum (00), PS1 to 0 V, PS2 to 5 V and SW2 to A. Measure pin 41 amplitude VBBS0.
						(8) Set Y/C GAIN COMP1 to maximum (11) and measure pin 41 amplitude VBBS1.
						(9) Set black stretch point 1 to maximum (111) and measure pin 41 amplitude VBBS2.
						(10) Set Y/C GAIN COMP2 to maximum (11) and measure pin 41 amplitude VBBS3.
						(11) Calculate using the following formulae. $GC_{BDY1} = 20 \times \ell og$ (VBDY1/VBDY0) $GC_{BDY2} = 20 \times \ell og$ (VBDY2/VBDY0) $GC_{BDY3} = 20 \times \ell og$ (VBDY3/VBDY0) $GC_{BBS1} = 20 \times \ell og$ (VBBS1/VBBS0) $GC_{BBS2} = 20 \times \ell og$ (VBBS2/VBBS0) $GC_{BBS3} = 20 \times \ell og$ (VBBS3/VBBS0)
						(12) Input 100-kHz sine wave to TP5, set pin 5 amplitude to 0.2 V_{P-P}, repeat steps (2) to (11) above and determine GC_{RDY1}, GC_{RDY2}, GC_{RDY3}, GC_{RSB1}, GC_{RSB2} and GC_{RSB3}.

Note No.	Parameter	Test Conditions				Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode				
		SW3	SW4	SW5	SW7	
S03	YUV gain	A/C	A/B	A/B	OPEN	(1) Set picture mute to off (P-MODE: Normal1 (000)), BRIGHTNESS to maximum (11111111), COLOR to center (1000000) and UNI-COLOR to maximum (1111111). (2) Set SW3 to A, and SW4 and SW5 to B; input a 100-kHz sine wave to TPA and set pin 3 amplitude to 0.2 V_{P-P}. (3) Set SW56 to open, YUV INPUT MODE to Y/Cb/Cr (00), Y/Pb/Pr (01), Through (10) and Y/U/V (11). Measure pin 56 amplitudes, VY00, VY01, VY10 and VY11. (4) Set SW3 to C, and SW4 to A and SW5 to B, input 100-kHz sine wave to TP4 and set pin 4 amplitude to 0.2 V_{P-P}. (5) Set YUV INPUT MODE to Y/Cb/Cr (00), Y/Pb/Pr (01), Through (10) and Y/U/V (11). Measure pin 41 amplitudes VB00, VB01, VB10 and VB11. (6) Set SW3 to C, and SW4 and SW5 to A; input a 100-kHz sine wave to TP5 and set pin 5 amplitude to 0.2 V_{P-P}. (7) Set YUV INPUT MODE to Y/Cb/Cr (00), Y/Pb/Pr (01), Through (10) and Y/U/V (11). Measure pin 43 amplitudes VR00, VR01, VR10 and VR11. (8) Calculate using the following formulae. $G_{Y00} = 20 \times \ell og$ (VY00/0.2) $G_{Y01} = 20 \times \ell og$ (VY01/0.2) $G_{Y10} = 20 \times \ell og$ (VY10/0.2) $G_{Y11} = 20 \times \ell og$ (VY11/0.2) $G_{BA} = 20 \times \ell og$ (VB01/VB00) $G_{BB} = 20 \times \ell og$ (VB10/VB00) $G_{BC} = 20 \times \ell og$ (VB11/VB00) $G_{RA} = 20 \times \ell og$ (VR01/VR00) $G_{RB} = 20 \times \ell og$ (VR10/VR00) $G_{RC} = 20 \times \ell og$ (VR11/VR00)
		SW8	SW9	SW10	—	
		B	B	B	—	

Test Conditions for Color Difference Signal 2

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
A01	Color difference signal contrast adjustment characteristic	C	A or B	A or B	A	A	A	A	A	A	(1) Set BRIGHTNESS to maximum and sub-address (12) data to F0. (2) Input signal 3 (f_0 = 100 kHz, picture period amplitude = 0.23 V_{P-P}) to pin 5. (3) Vary UNI-COLOR to maximum (7F), center (40) and minimum (00) and measure pin 43 picture period amplitudes V_{uCYMAX}, V_{uCYCNT} and V_{uCYMIN}. (4) Determine in decibels amplitude ratio ΔV_{uCY} of UNI-COLOR maximum to minimum. (5) Repeat steps (2) and (4) changing input to pin 4 (picture period amplitude = 0.2 V_{P-P}), and measure pin 41 output.
A02	Color adjustment characteristic	C	A or B	A or B	A	A	A	A	A	A	(1) Set BRIGHTNESS to maximum and sub-address (12) data to F0. (2) Input signal 3 (f_0 = 100 kHz, picture period amplitude = 0.115 V_{P-P}) to pin 5. (3) Vary COLOR to maximum (7F), center (40) and minimum (01), and measure pin 43 picture period amplitudes V_{CCYMAX}, V_{CCYCNT} and V_{CCYMIN}. (4) Determine in decibels amplitude ratio ΔV_{CCY} of maximum and minimum to COLOR center. (5) Repeat steps (2) and (4), changing input to pin 4 (picture period amplitude = 0.1 V_{P-P}), and measure pin 41 output.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
A03	Color difference signal half-tone characteristic	C	A or B	A or B	A	A	A	A	A	A	(1) Input signal 3 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 5. (2) Measure pin 43 output picture period amplitude vHTARY. (3) Apply 1.5 V to pin 52 from external power supply. (4) Measure pin 43 output picture period amplitude vHTBRY. (5) Determine GHT_{RY} = vHTBRY/vHTARY. (6) Repeat steps (1) to (5) above, changing pin to pin 42, and determine GHT_{GY} = vHTBGY/vHTAGY. (7) Input signal to pin 4, measure pin 4 and determine GHT_{BY} = vHTBBY/vHTABY.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
A04	Color γ characteristic	C	B	A	A	A	A	A	A	A	(1) Input signal 2 to pin 5. (2) Increase signal 2 amplitude A. When sub-address (14) data starts with γ correction, determine pin 43 output signal amplitudes $V\gamma_1$, $V\gamma_2$ and $V\gamma_3$. Graph the results in the following cases: (01) – γ off (03) – γ1 on (05) – γ2 on (07) – γ3 on (3) Determine Vγ where γ starts applying and gradient ratio Δγ at γ on when linearity at off is (1). 

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
A05	Color limiter characteristic	C	B	A	A	A	A	A	A	A	(1) Input signal 2 (picture period amplitude = 0.4 V_{P-P}) to pin 4. (2) When sub-address (14) data is 00 and 01, measure pin 43 output signal picture period amplitudes C_{LT0} and C_{LT1}.
A06	High bright color gain	C	B	A	A	A	A	A	A	A	(1) Input signal 2 (picture period amplitude = 0.2 V_{P-P}) to pin 4. (2) Adjust COLOR and set pin 41 output picture period amplitude to 1.2 V_{P-P}. (3) When sub-address (0B) data is 80, measure pin 41 output signal picture period amplitude V_{41}. (4) Calculate using the following formula. $HBC_1 = (1.2 - v_{41})/1.2$

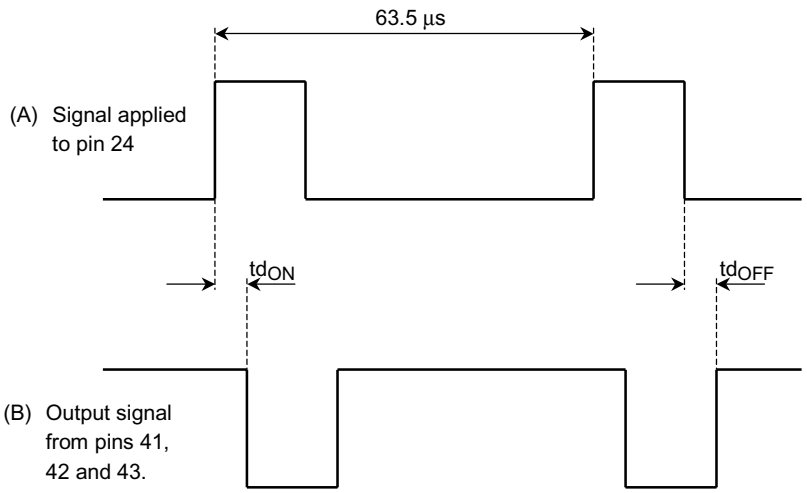
Test Conditions for Text

Common Test Conditions for Text

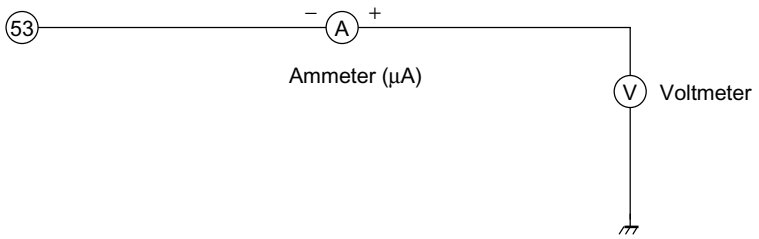
(1) Unless otherwise specified, measure bus data using preset values.
(2) Set the following data:
Sub-address (00) to data (02)
Sub-address (05) to data (7F)
Sub-address (09) to data (40)
Sub-address (0B) to data (7F)
Sub-address (0C) to data (82)
Sub-address (12) to data (F0)
Sub-address (19) to data (F8)
Sub-address (1A) to data (E0)
Sub-address (1B) to data (E0)
Sub-address (1D) to data (78)
Sub-address (1E) to data (87)

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T01	AC gain	A	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, amplitude of picture period voltage = 0.2 V_{P-P}) to pin 3. (2) Measure pins 41, 42 and 43 picture period amplitudes V_{41}, V_{42} and V_{43}. (3) Determine AC gain using the following formulae. $G_R = V_{43}/0.2$ $G_G = V_{42}/0.2$ $G_B = V_{41}/0.2$
T02	Unicolor adjustment characteristic	A	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, amplitude of picture period voltage = 0.2 V_{P-P}) to pin 3. (2) Vary UNI-COLOR data to maximum (7F), center (40) and minimum (00), and measure pin 43 picture period amplitudes V_{uMAX}, V_{uCNT} and V_{uMIN}. (3) Determine amplitude ratio ΔV_u of V_{uMAX} to V_{uCNT} (in decibels).
T03	Brightness adjustment characteristic	A	B	B	A	A	A	A	A	A	(1) Input signal 2 to pin 3 and set pin 43 picture period amplitude to 1 V_{P-P}. (2) Vary BRIGHTNESS to maximum (7F), center (80) and minimum (00), and measure pin 43 voltages V_{brMAX}, V_{brCNT} and V_{brMIN}.
T04	White peak slice level	C	B	B	A	A	A	A	A	A	(1) Set SUB-CONTRAST to maximum. (2) Apply external power supply to pin 3 and increase voltage from 5.8 V. (3) When pin 43 picture period is clipped, measure pin 43 picture period amplitude voltage V_{WPS1}. (4) Repeat steps from (1) to (3) above (for V_{WPS2}), changing sub-address (0C) data to 06.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T05	Black peak slice level	C	B	B	A	A	A	A	A	A	(1) Apply external power supply to pin 3 and gradually decrease voltage from 5.8 V. (2) When picture period is clipped, measure V_{bps} voltage for pins 41, 42 and 43.
T06	RGB output S/N	C	B	B	A	A	A	A	A	A	(1) Adjust BRIGHTNESS so that pin 41 picture period voltage is 2.4 V. (2) Set COLOR to minimum. (3) Measure pins 41, 42 and 43 picture period noise levels n41, n42 and n43 (V_{P-P}) using oscilloscope. (4) Calculate S/N. $N_{41} = -20 \times \ell og\ [2.3/(0.2 \times n41)]$ $N_{42} = -20 \times \ell og\ [2.3/(0.2 \times n42)]$ $N_{43} = -20 \times \ell og\ [2.3/(0.2 \times n43)]$
T07	Half-tone characteristic	A	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, amplitude of picture period voltage = 0.2 V_{P-P}) to pin 3. (2) Measure pin 41 picture period amplitude v41A. (3) Apply 1.5 V to pin 52 from external power supply. (4) Measure pin 41 picture period amplitude v41B. (5) Determine G_{HT1} = v41B/v41A. (6) Stop applying voltage to pin 52, set sub-address (1A) data to E2 and measure pin 41 picture period amplitude v41C. (7) Determine G_{HT2} = v41C/v41A.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T08	Blanking pulse delay time	C	B	B	A	A	A	A	A	A	(1) Apply signal shown in Figure (A) to pin 24 (BLK IN) and determine td_{ON} and td_{OFF} from output signal from pins 41, 42 and 43 (Figure (B)). 

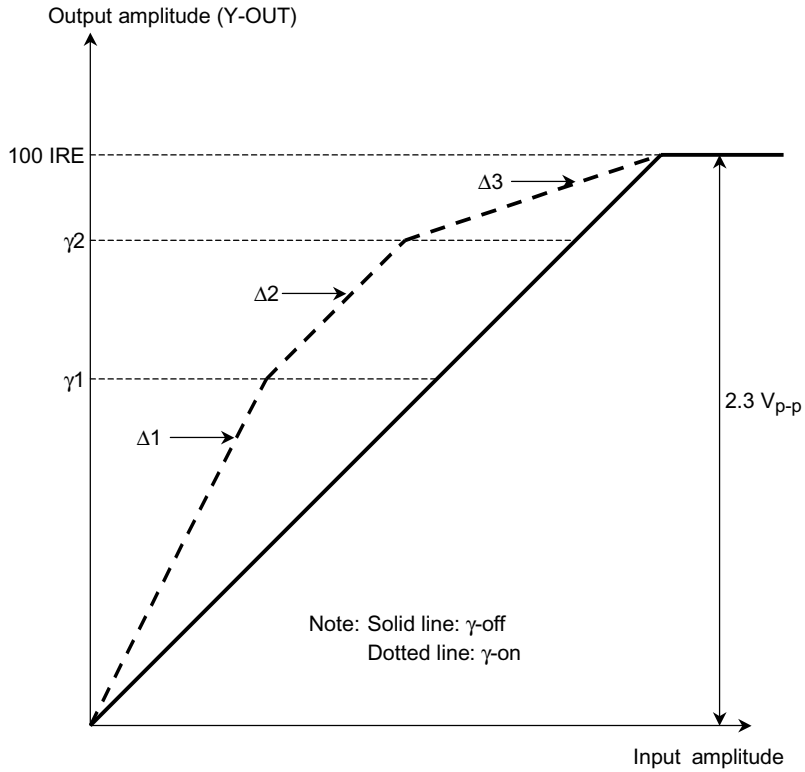
Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T09	Drive adjustment variable range	A	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3. (2) Change sub-address (0D) data to maximum (FE), center (80) and minimum (00), and measure pin 42 picture period amplitude. (3) Determine in decibels amplitude ratios of maximum and minimum to drive center (DRG_{G1+}, DR_{G1-}). (4) Repeat steps (1) to (3) above, changing sub-address (0E) data to instead, and determine in decibels pin 41 picture period amplitude ratios (DR_{B1+}, DR_{B2-}). (5) Repeat steps (1) to (3) above, changing sub-address (0E) data to center (81), and determine in decibels pin 42 picture period amplitude ratios (DR_{G2+}, DR_{G2-}). (6) Repeat steps (1) to (3) above, changing sub-address (0E) data to maximum (FF), center (81) and minimum (01), and determine in decibels pin 41 amplitude ratios (DR_{B2+}, DR_{B2-}). (7) Repeat steps (1) to (3) above, changing sub-address (0D) data to maximum (FF), center (81) and minimum (01), and determine in decibels pin 43 amplitude ratios (DR_{R1+}, DR_{R1-}). (8) Repeat steps (1) to (3) above, setting sub-address (0D) data to 81 and changing sub-address (0E) data, and determine in decibels pin 41 picture period amplitude ratios (DR_{B3+}, DR_{B3-}). (9) Repeat steps (1) to (3) above, setting sub-address (0E) data to 81 and changing sub-address (0D) data to maximum (FF), center (81) and minimum (01), and determine in decibels pin 42 picture period amplitude ratios (DR_{G3+}, DR_{G3-}). (10) Repeat steps (1) to (3) above, setting sub-address (0D) data to 81 and changing sub-address (0E) data to maximum (FF), center (81) and minimum (01), and determine in decibels pin 43 picture period amplitude ratios (DR_{R2+}, DR_{R2-}).

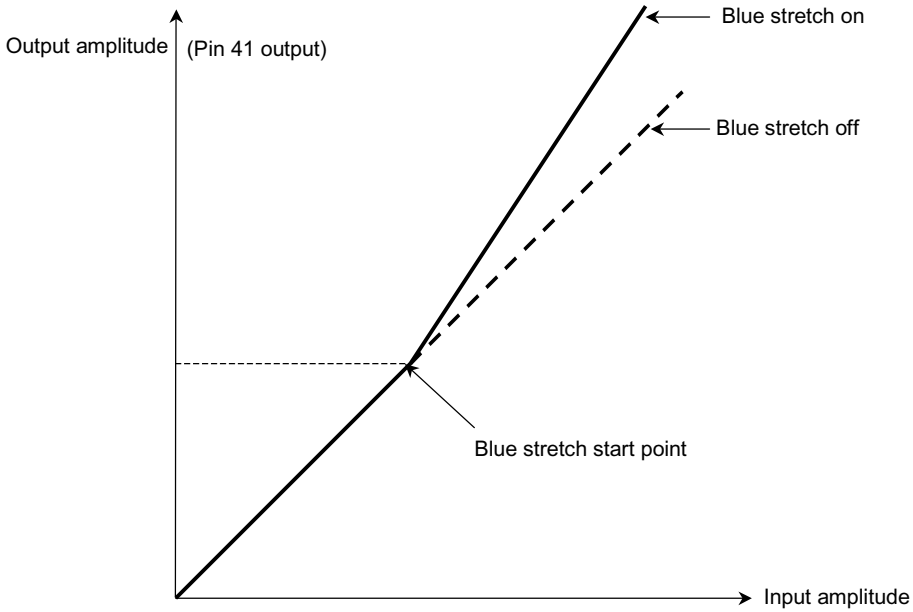
Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T10	Pin 53 input impedance	C	B	B	A	A	A	A	A	A	(1) Connect external power supply, voltmeter and ammeter as shown below. Adjust voltage so that current value is 0. (2) Increase pin 53 voltage by 0.2 V and measure current value of ammeter I_{in}. (3) Determine Z_{in53} = 0.2 V/I_{in} (Ω). 
T11	ACL characteristic	C	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3. (2) Measure pin 43 picture period amplitude vACL1. (3) Apply external power supply (pin 53 DC voltage − 0.5 V) to pin 53 and measure pin 43 picture period amplitude vACL2. (4) Apply external power supply (pin 53 DC voltage − 1 V) to pin 53 and measure pin 43 picture period amplitude vACL3. (5) Calculate using the following formulae. $ACL_1 = -20 \times \log$ (vACL2/vACL1) $ACL_2 = -20 \times \log$ (vACL3/vACL1)

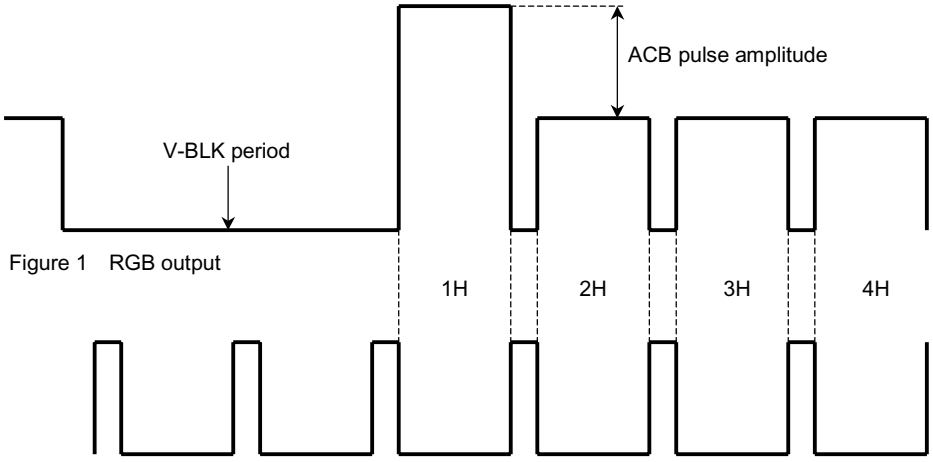
Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T12	ABL point	C	B	B	A	A	A	A	A	A	(1) Measure pin 53 DC voltage VABL1. (2) Set sub-address (1B) data to 1C. (3) Apply external power supply to pin 53 and decrease voltage from 6.5 V. When pin 43 voltage starts changing, measure pin 53 voltage VABL2. (4) Repeat step (3) above, making the following changes: Set sub-address (1B) data to 3C, 5C, 7C, 9C, BC, DC and FC and measure the following voltages on pin 53: VABL3, VABL4, VABL5, VABL6, VABL7, VABL8 and VABL9. (5) ABL_{P1} = VABL2 – VABL1 ABL_{P5} = VABL6 – VABL1 ABL_{P2} = VABL3 – VABL1 ABL_{P6} = VABL7 – VABL1 ABL_{P3} = VABL4 – VABL1 ABL_{P7} = VABL8 – VABL1 ABL_{P4} = VABL5 – VABL1 ABL_{P8} = VABL9 – VABL1
T13	ABL gain	C	B	B	A	A	A	A	A	A	(1) Apply external power supply of 6.5 V to pin 53. (2) Set sub-address (1B) data to 00. (3) Set BRIGHTNESS to maximum. (4) Apply external power supply of 4.5 V to pin 53. (5) Repeat step (3) above, making the following changes: Set sub-address (1B) data to 00, 04, 08, 0C, 10, 14, 18 and 1C and measure the following voltages on pin 53: VABL11, VABL12, VABL13, VABL14, VABL15, VABL16, VABL17 and VABL18. (6) ABL_{G1} = VABL11 – VABL10 ABL_{G2} = VABL12 – VABL10 ABL_{G3} = VABL13 – VABL10 ABL_{G4} = VABL14 – VABL10 ABL_{G5} = VABL15 – VABL10 ABL_{G6} = VABL16 – VABL10 ABL_{G7} = VABL17 – VABL10 ABL_{G8} = VABL18 – VABL10

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T14	RGB output mode	C	B	B	A	A	A	A	A	A	(1) Adjust BRIGHTNESS so that pin 43 picture period voltage becomes 2.4 V. (2) Set sub-address (1B) data to 01. (3) Measure picture period voltages V_{43R}, V_{42R} and V_{41R} on pins 43, 42 and 41 respectively. (4) Repeat step (3) above, changing sub-address (1B) data to 02, and measure picture period voltages V_{43G}, V_{42G} and V_{41G} on pins 43, 42 and 41 respectively. (5) Repeat step (3), changing sub-address (1B) data to 03, and measure picture period voltages V_{43B}, V_{42B} and V_{41B} on pins 43, 42 and 41 respectively.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T15	Y-OUT γ characteristic	A	B	B	A	A	A	A	A	A	(1) Input ramp waveform to pin 3 and adjust input amplitude so that pin 43 picture period amplitude becomes 2.3 V_{P-P}. (2) Set sub-address (1C) data to 01. (3) Adjust input amplitude so that pin 43 picture period amplitude becomes 2.3 V_{P-P}. (4) According to the figure below, determine in decibels Y-OUT γ correction start points γ1 and γ2 and gradient ratios Δ1, Δ2 and Δ3, which are ratios of gradient at γ-on to gradient at γ-off.



Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T16	Blue stretch circuit characteristic	A	B	B	A	A	A	A	A	A	(1) Input ramp signal of 0.7 V_{P-P} to pin 3. (2) Set SUB-CONTRAST to maximum. (3) Set sub-address (1F) data to 04. (4) Set sub-address (1E) data to 00 and determine blue stretch start point BS_Pmin using pin 41 in the figure below. (5) Repeat step (4) above, changing sub-address (1E) data to 04 and 07. Determine blue stretch start points BS_PCNT and BS_Pmax. (6) Set sub-address (1E) data to 04. (7) Determine in decibels ratio of gradient at blue stretch on to gradient at blue stretch off, using pin 41 as shown in the figure below. (8) Repeat step (7) above, changing sub-address (1F) data to 00 and 07, and determine in decibels gradient ratios BS_Gmin and BS_Gmax. Note: The blue stretch start point is determined as an IRE value by setting the amplitude from the output signal pedestal level to the positive side to be 2.3 V_{P-P} = 100 IRE. 

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T17	ACB pulse phase and amplitude	A or C	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3. Adjust DRIVE GAIN 1/2 so that pin 41/42 picture period amplitude is equal to that of pin 43. (2) Measure voltage of pins 46, 47 and 48 and apply measured voltages from external power supply to pins. (3) Set sub-address (02) data to 40. (4) Determine ACB pulse phase by referencing signal waveform output from pins 43, 42 and 41 as shown in Figure 1 below. Note: The first picture period after V-BLK ends and FBP input falls is 1H. After each H-BLK, the phase is 2H, 3H and so on.  Figure 1 RGB output Figure 2 FBP input (pin 24) (5) Determine ACB pulse amplitudes VACB1R, VACB1G and VACB1B by referencing signal waveform output from pins 43, 42 and 41. (Amplitude is based on picture period level at no input.) (6) Repeat step (5) above, setting sub-address (02) data to 80, and measure VACB2R, VACB2G and VACB2B. (7) Repeat step (5) above, setting sub-address (02) data to C0, and measure VACB3R, VACB3G and VACB3B.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T18	IK input amplitude	A or C	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3. Adjust DRIVE GAIN 1/2 so that pin 41/42 picture period amplitude is equal to that of pin 43. (2) Set sub-address (02) data to 40. (3) Determine voltage amplitudes while ACB pulse is being applied to pin 45 input signal as shown in Figure 1 of T19 above. At 1H = IK_R, at 2H = IK_G and at 3H = IK_B
T19	IK input cover range	C	B	B	A	A	A	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3 and adjust DRIVE GAIN 1/2 so that pin 41/42 picture period amplitude is equal to that of pin 43. (2) Set sub-address (02) data to 40. (3) Determine DC voltage of pin 45 during V-BLK (#45VBLK). (4) Apply external voltage via 10 kΩ and gradually increase the voltage from 0 V. (5) Determine DC voltage of pin 45 during V-BLK when picture period amplitude of pin 43 has just started decreasing (#45VBLK+). (6) Reset the external voltage to 0 V and gradually decrease from 0 V. (7) Determine DC voltage of pin 45 during V-BLK when picture period amplitude of pin 43 has just started increasing (#45VBLK–). (8) DIK_{in+} = (#45VBLK+) – (#45VBLK) DIK_{in-} = (#45VBLK–) + (#45VBLK)
T20	Analog RGB gain	A	B	B	A or B	A or B	A or B	A	A	A	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3 and adjust DRIVE GAIN 1/2 so that pin 41/42 picture period amplitude is equal to that of pin 43. (2) Apply 5 V from external power supply to pin 49. (3) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 35. (4) Measure picture period amplitude v43R on pin 43. (5) Repeat steps (3) and (4), making the following changes. Input signal 1 to pin 34 and measure pin 42 output (v42G). Input signal 1 to pin 33 and measure pin 41 output (v41B). (6) Calculate using the following formulae. GTXR = v43R/0.2 GTXG = v42G/0.2 GTXB = v41B/0.2

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T21	Analog RGB white peak slice level	A	B	B	A	A	A	A	A	A	(1) Apply 5 V from external power supply to pin 49. (2) Set RGB CONTRAST to maximum (7F). (3) Apply external power supply to pin 35. Gradually increase voltage from 3.0 V DC. When pin 43 output is clipped, measure picture period amplitude. (4) Repeat step (3), making the following changes: Input to pin 34 and measure pin 42 output; input to pin 33 and measure pin 41 output.
T22	Analog RGB black peak limit level	A	B	B	A	A	A	A	A	A	(1) Apply 5 V from external power supply to pin 49. (2) Set RGB CONTRAST to maximum (7F). (3) Apply external power supply to pin 35. Gradually increase voltage from 4.5 V DC. When pin 43 output is clipped, measure picture period amplitude. (4) Repeat step (3), making the following changes: Input to pin 34 and measure pin 42 output; input to pin 33 and measure pin 41 output.
T23	RGB contrast adjustment characteristic	A	B	B	A or B	A or B	A or B	A	A	A	(1) Apply 5 V from external power supply to pin 49. (2) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 35. (3) Change RGB CONTRAST to maximum (7F), center (40) and minimum (00), and measure picture period amplitude output V_{uTXR} (max, CNT and min) on pin 43. (4) Determine in decibels amplitude ratios of maximum and minimum to center. (5) Repeat steps (3) and (4), making the following changes: Input to pin 34 and measure picture period amplitude output on pin 42. Input to pin 33 and measure picture period amplitude output on pin 41.
T24	Analog RGB brightness adjustment characteristic	A	B	B	A or B	A or B	A or B	A	A	A	(1) Input signal 2 to pins 33, 34 and 35. (2) Apply 5 V from external power supply to pin 49. (3) Adjust signal 2 amplitude (A) so that pin 43 picture period amplitude becomes 0.5 V_{P-P}. (4) Change RGB BRIGHTNESS to maximum (FE), center (80) and minimum (00), and measure picture period voltage output V_{brTX} (max, CNT and min) on pins 43, 42 and 41 respectively.
T25	Analog RGB mode switching transfer characteristic	C	B	B	A	A	A	A	A	A	(1) Set RGB BRIGHTNESS to maximum (FE). (2) Input signal 4 (signal amplitude = 1.5 V_{P-P}) to pin 49. (3) Measure input/output transfer characteristic using pin 43 in Figure T-2. (4) Repeat steps (2) and (3) above, making the following changes: Input to pin 34 and measure pin 42; input to pin 33 and measure pin 41. (5) Determine maximum inter-axial rise/fall transfer delay time, using the data measured above.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T26	Text ACL characteristic	A	B	B	A	A	B	A	A	A	(1) Apply 5 V from external power supply to pin 49. (2) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 35. (3) Measure pin 43 picture period amplitude vTXACL1. (4) Apply external power supply (pin 53 DC voltage – 0.5 V) to pin 53 and measure picture period amplitude output vTXACL2 on pin 43. (5) Apply external power supply (pin 53 DC voltage – 1.0 V) to pin 53 and measure picture period amplitude output vTXACL3 on pin 43. (6) $TXACL_1 = -20 \times \ell og$ (vTXACL2/vTXACL1) $TXACL_2 = -20 \times \ell og$ (vTXACL3/vTXACL1) (7) Repeat steps (5) and (6), setting sub-address (10) data to 01 to ascertain $TXACL_3$ and $TXACL_4$.
T27	Analog OSD gain	A	B	B	A	A	A	A or B	A or B	A or B	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3 and adjust DRIVE GAIN 1/2 so that pin 41/42 picture period amplitude is equal to that of pin 43. (2) Apply 5 V from external power supply to pins 50 and 51. (3) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 39. (4) Adjust output picture period amplitude v43R on pin 43. (5) Repeat steps (3) and (4), making the following changes: Input to pin 38 and measure picture period amplitude output on pin 42 (v42G). Input to pin 37 and measure picture period amplitude output on pin 41 (v41B). (6) Calculate using the following formulae. G_{OSDR} = v43R/0.2 G_{OSDG} = v42G/0.2 G_{OSDB} = v41B/0.2
T28	Analog OSD white peak slice level	A	B	B	A	A	A	A	A	A	(1) Apply 5 V from external power supply to pins 50 and 51. (2) Apply external power supply to pin 39 and gradually increase voltage from 4.5 V DC. When pin 43 output is clipped, measure picture period amplitude. (3) Repeat step (2), making the following changes: Input to pin 38 and measure picture period amplitude output on pin 42. Input to pin 37 and measure picture period amplitude output on pin 41.
T29	Analog OSD black peak limit level	A	B	B	A	A	A	A	A	A	(1) Apply 5 V from external power supply to pins 50 and 51. (2) Apply external power supply to pin 39 and gradually decrease voltage from 4.5 V DC. When pin 43 output is clipped, measure picture period amplitude. (3) Repeat step (2), making the following changes. Input to pin 38 and measure picture period amplitude output on pin 42. Input to pin 37 and measure picture period amplitude output on pin 41.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T30	Analog OSD contrast adjustment characteristic	A	B	B	A	A	A	A or B	A or B	A or B	(1) Apply 5 V from external power supply to pins 50 and 51. (2) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 39. (3) Change OSD-CONTRAST to (11), (10), (01) and (00) and measure picture period amplitude outputs V_{uOSDR} (11), (10), (01) and (00) on pin 43. (4) Repeat steps (2) and (3), making the following changes: Input to pin 38 and measure picture period amplitude outputs V_{uOSDG} (11), (10), (01) and (00) on pin 42. Input to pin 37 and measure picture period amplitude outputs V_{uOSDB} (11), (10), (01) and (00) on pin 41.
T31	Analog OSD brightness adjustment characteristic	C	B	B	A	A	A	A	A	A	(1) Apply 5 V from external power supply to pins 50 and 51. (2) Change OSD BRIGHT (sub-address 1D) to (38), (78), (B8) and (F8) and measure picture period voltage outputs on pins 43, 42 and 41. Data (38) – V_{brOSD0} Data (78) – V_{brOSD1} Data (B8) – V_{brOSD2} Data (F8) – V_{brOSD3}
T32	Analog OSD mode switching transfer characteristic	C	B	B	A	A	A	A	A	A	(1) Set OSD BRIGHT to maximum (11). (2) Input signal 4 (signal amplitude = 4.5 V_{P-P}) to pin 50. (3) Measure input/output transfer characteristic, using pin 43 as shown in Figure T-2. (4) Repeat steps (2) and (3) above, and measure pins 42 and 41. (5) Determine maximum inter-axial rise/fall transfer delay time, using the data measured above. (6) Repeat steps (1) to (5), inputting signal 4 (signal amplitude = 4.5 V_{P-P}) to pin 51, and measure.

Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T33	OSD ACL characteristic	A	B	B	A	A	A	A	A	B	(1) Set sub-address (07) data to 01. (2) Apply 5 V from external power supply to pins 50 and 51. (3) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 39. (4) Measure picture period amplitude vOSDACL1 on pin 43. (5) Apply external power supply (pin 53 DC voltage – 0.5 V) to pin 53 and measure picture period amplitude vOSDACL2 on pin 43. (6) Apply external power supply (pin 53 DC voltage – 1 V) to pin 53 and measure picture period amplitude vOSDACL3 on pin 43. (7) $OSDACL_1 = -20 \times \ell og$ (vOSDACL2/vOSDACL1) $OSDACL_2 = -20 \times \ell og$ (vOSDACL3/vOSDACL1) (8) Repeat steps (5) and (6) above, changing sub-address (07) data to 00, and measure OSDACL3 and OSDACL4.

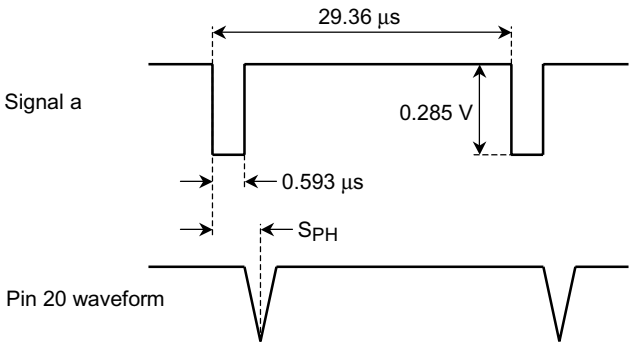
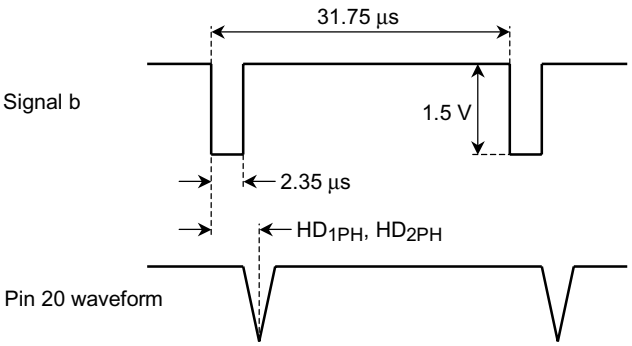
Note No.	Parameter	Test Conditions									Test Method (test conditions: V_{CC} = 9 V/2 V, Ta = 25° ± 3°C)
		SW mode									
		SW3	SW4	SW5	SW33	SW34	SW35	SW37	SW38	SW39	
T34	OSD blending characteristic	A ↓ C	B	B	A	A	A	A ↓ B	A ↓ B	B ↓ B	(1) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pin 3. (2) Measure picture period amplitudes v41a, v42a and v43a on pins 41, 42 and 43 respectively. (3) Apply 5 V from external power supply to pin 51. (4) Measure picture period amplitudes v41b, v42b and v43b on pins 41, 42 and 43 respectively. (5) Determine in decibels v41b amplitude in relation to v41a; v42b amplitude in relation to v42a; v43b amplitude in relation to v43a: α41TV1, α42TV1 and α43TV1. (6) Repeat steps (3) to (5), applying 5 V from external power supply to pin 50, and measure α41TV2, α42TV2 and α43TV2. (7) Repeat steps (3) to (5), applying 5 V from external power supply to pins 50 and 51, and measure α41TV3, α42TV3 and α43TV3. (8) Set to SW3 to C; SW37, SW38, Sw39 to B. (9) Input signal 1 (f_0 = 100 kHz, picture period amplitude = 0.2 V_{P-P}) to pins 37, 38 and 39. (10) Apply 5 V from external power supply to pins 50 and 51. (11) Measure picture period amplitudes v41c, v42c and v43c on pins 41, 42 and 43 respectively. (12) Apply 5 V from external power supply to pin 50. (13) Measure picture period amplitudes v41d, v42d and v43d on pins 41, 42 and 43 respectively. (14) Determine in decibels v41d amplitude in relation to v41c; v42d amplitude in relation to v42c; v43d amplitude in relation to v43c: α41OSD1, α42OSD1 and α43OSD1. (15) Repeat steps (12) to (14), applying 5 V from external power supply to pin 51, and measure α41OSD2, α42OSD2 and α43OSD2. (16) Repeat steps (12) to (14), applying 5 V from external power supply to pins 50 and 51, and measure α41OSD3, α42OSD3 and α43OSD3.

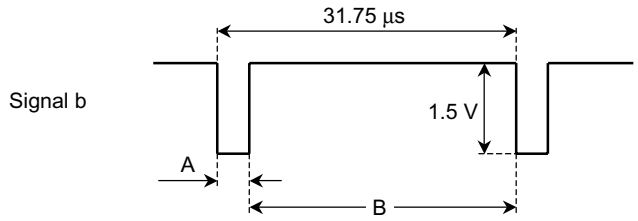
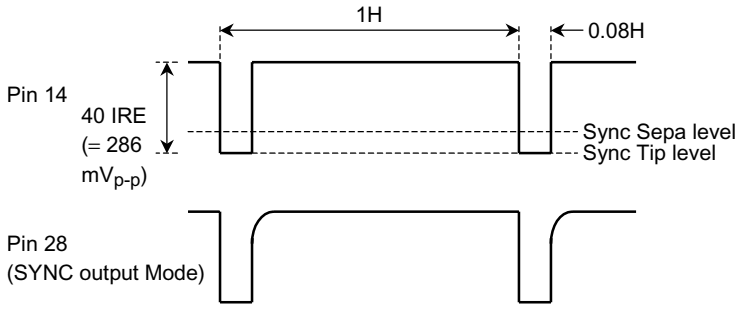
Test Conditions for Deflection

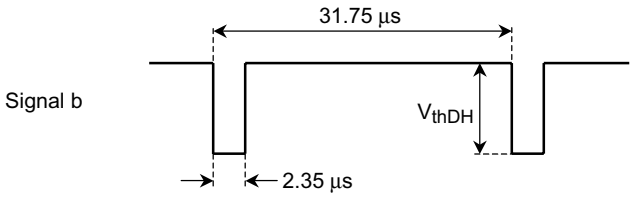
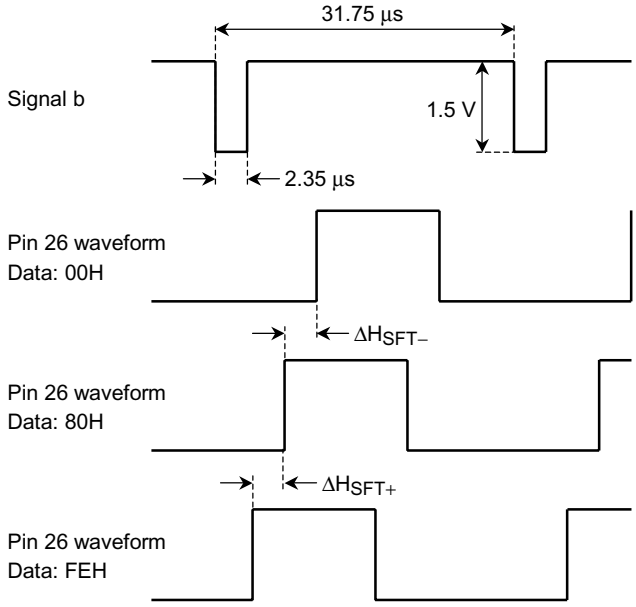
Common Test Conditions for Sync Signal

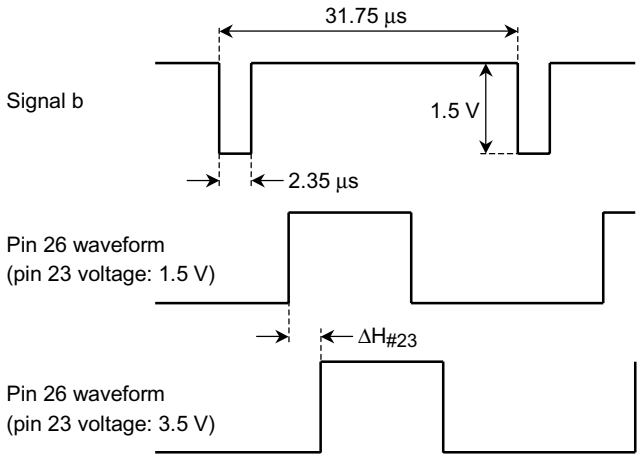
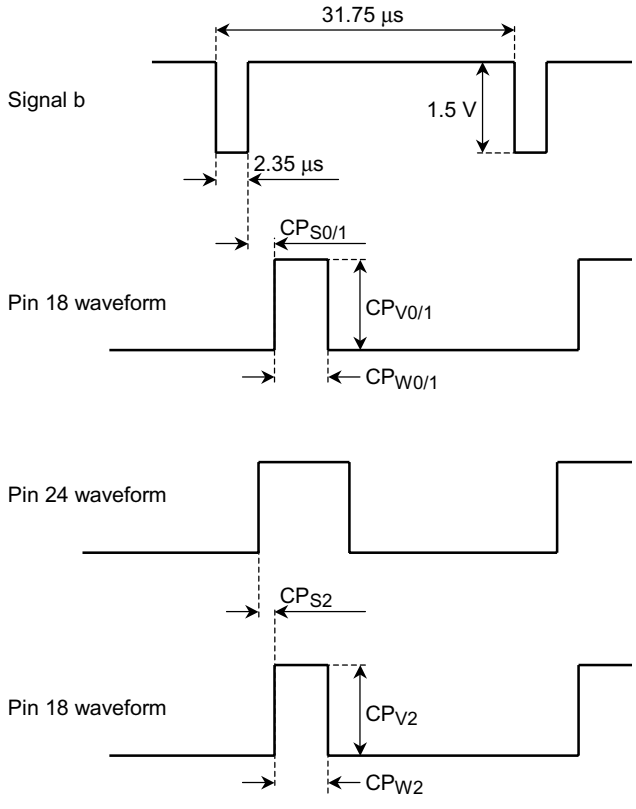
(Unless otherwise specified, V_{CC} = 9 V/2 V, Ta = 25°C, BUS data = preset values.)

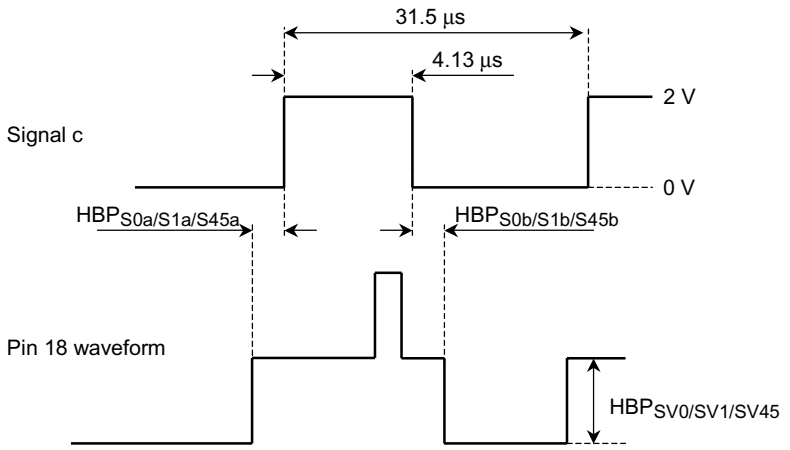
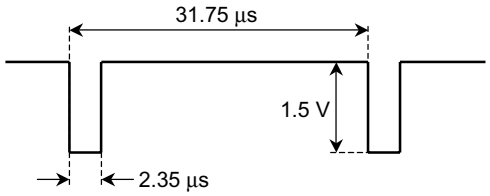
(Unless otherwise specified, SW3 = A, SW14 = A, SW20 = on, SW22 = open, SW23 = B, SW24a = B, SW24b = open and SW26 = B.)

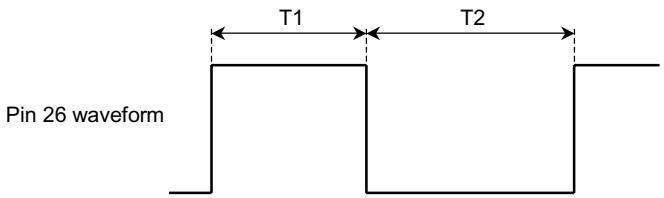
Note No.	Parameter	Test Method
HA01	Sync input horizontal sync phase	(1) Input signal a (as shown in figure below) to TPA. Set sub-address (00) data to 82H. (2) Determine phase difference S_{1PH} from pin 14 (SYNC IN) input waveform and pin 20 (AFC filter) waveform. 
HA02	HD 1/2 input horizontal sync phase	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Determine phase difference HD_{1PH} from pin 16 (HD1 IN) input waveform and pin 20 (AFC filter) waveform. (4) Input signal b to TP13 and set sub-address (00) data to 41H. (5) Determine phase difference HD_{2PH} as in step (3) above. 

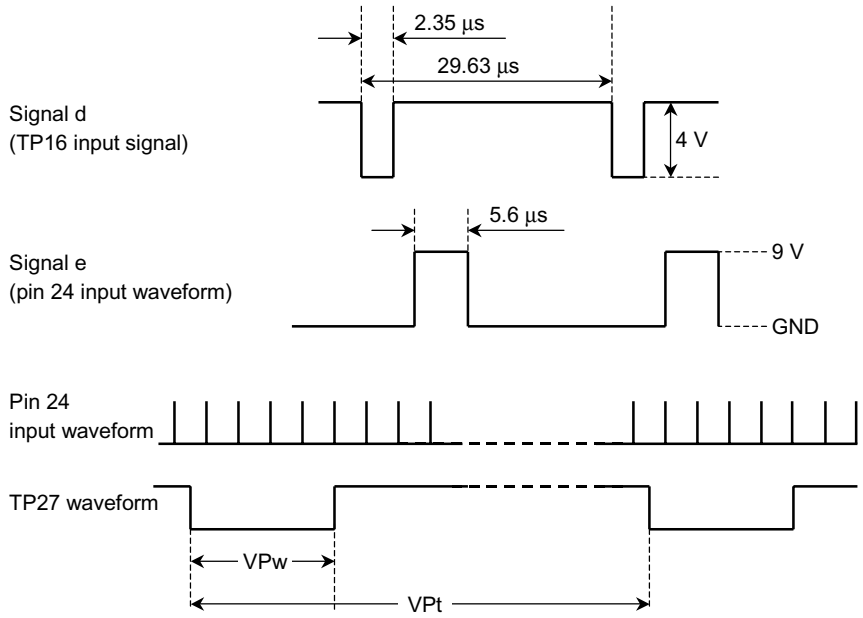
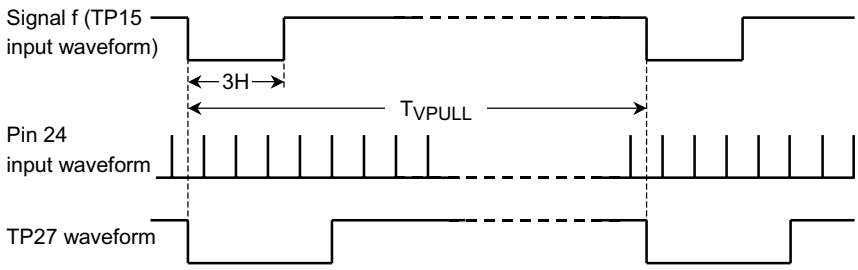
Note No.	Parameter	Test Method
HA03	Polarity detection range	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Decrease signal b duty from 10% (to shorter negative polarity period) and determine signal b duty (HD_{DUTY1}) when pin 16 input signal phase no longer locks with that of pin 26 (H-OUT). (4) Increase signal b duty from 10% (to longer negative polarity period) and determine signal b duty (HD_{DUTY2}) when pin 24 (FBP IN) phase changes in relation to signal b. (5) Further increase signal b duty (to longer negative polarity period) and determine signal b duty (HD_{DUTY3}) when pin 16 input signal phase no longer locks with that of pin 26 (H-OUT). (6) Decrease signal b duty from 90% (to shorter negative polarity period) and determine signal b duty (HD_{DUTY4}) when pin 24 (FBP IN) phase changes in relation to signal b.  Duty = A/B × 100% (0%~100%)
HA04	Sync input threshold amplitude	(1) Set sub-address (00) to 82H and TEST mode to 01. (2) Apply external voltage via 20 kΩ to pin 14. (3) Set external voltage to 0 V and monitor pin 14 pin voltage SYNC_TIP_00. Also check that pin 28 pin voltage is L. (4) By increasing external voltage SYNC_OFF_00, monitor pin 14 SYNC IN pin voltage when pin 28 DAC1 pin voltage becomes H. (5) Determine SYNC input level at SYNC separation level 00 as follows: V_{ths00} = (SYNC_OFF_00 – SYNC_TIP_00) /0.286 × 100 (6) Set SYNC separation level from 01 to 10 to 11, and determine V_{ths01}, V_{ths10} and V_{ths11}. V_{ths01} = (SYNC_OFF_01 – SYNC_TIP_01) /0.286 × 100 V_{ths10} = (SYNC_OFF_10 – SYNC_TIP_10) /0.286 × 100 V_{ths11} = (SYNC_OFF_11 – SYNC_TIP_11) /0.286 × 100 

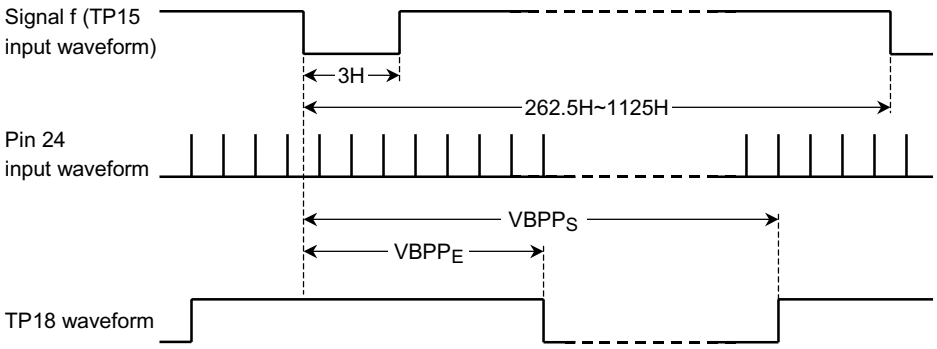
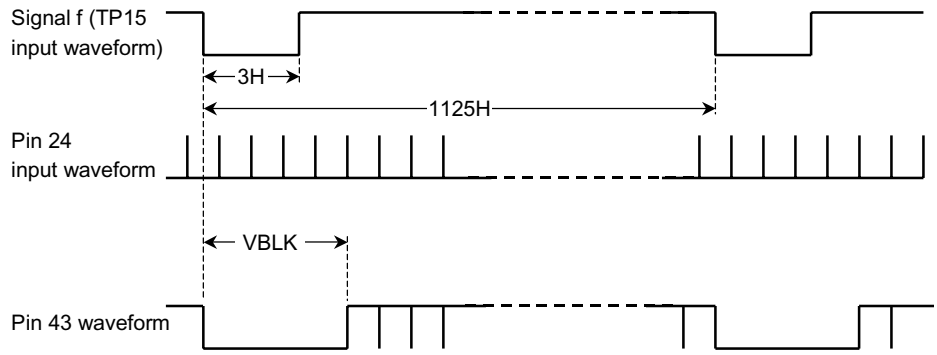
Note No.	Parameter	Test Method
HA05	HD 1/2 input threshold voltage	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Increase signal b amplitude from 0 V_{P-P}. When pin 26 (H-OUT) phase locks with that of signal b, determine signal b amplitude V_{thHD1}. (4) Input signal b (as shown in figure below) to TP13 and set sub-address (00) data to 41H. (5) Measure as in step (3) above, and determine signal amplitude V_{thHD2}. 
HA06	Horizontal picture phase adjustment variable range	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Change sub-address (01) data from 80H to 00H and measure pin 26 (H-OUT) waveform phase change ΔH_{SFT-}. (4) Change sub-address (01) data from 80H to FEH and measure pin 26 (H-OUT) waveform phase change ΔH_{SFT+}. 

Note No.	Parameter	Test Method
HA07	Curve correction	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Connect external power supply to pin 23 (H CURVE CORRECTION). Apply 1.5 V and 3.5 V to pin 23 and measure the output waveform phase change $\Delta H_{\#23}$ on pin 26 (H-OUT). 
HA08	Clamp pulse phase, width and level	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Determine clamp pulse phase CP_{S0}, width CP_{PW0} and output level CP_{V0} on pin 18 (SCP OUT) in relation to signal b. (4) Set sub-address (01) data to 81H. Determine CP_{S1}, CP_{PW1} and CP_{V1} as in step (3) above. (5) Apply no signal input to TP16. (6) Determine pin 18 clamp pulse phase CP_{S2}, width CP_{PW2} and output level CP_{V2} in relation to pin 24. 

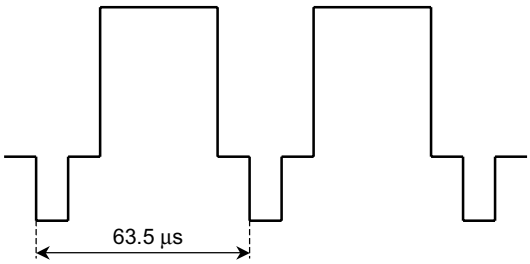
Note No.	Parameter	Test Method
HA09	Black peak detection pulse phase and level	(1) Set sub-address (00) data to 40H. (2) Set SW24A to open. (3) Input signal c (as shown in figure below) to pin 24 (FBP IN). (4) Determine pin 18 (SCP OUT) black peak detection pulse phase HBP_{S0a} and HBP_{S0b} in relation to signal c. (5) Determine output level HBP_{SV0} from pin 18 (SCP OUT) output waveform. (6) Set sub-address (02) data to 90H. (7) Measure as in steps (4) and (5), and determine phases HBP_{S1a} and HBP_{S1b}, and output level HBP_{SV1}. (8) Change sub-address (00) data to C0H and sub-address (02) data to 80H, and determine phases HBP_{S45a} and HBP_{S45b}, and output level HBP_{SV45}. 
HA10	FBP threshold	(1) Set sub-address (00) data to 40H. (2) Input signal b (as shown in figure below) to TP16. (3) Increase amplitude of FBP signal input to pin 24 (FBP IN) from 0 V_{P-P}. When signal b and pin 26 (H-OUT) phases are locked, measure pin 24 input amplitude (V_{thFBP}). 

Note No.	Parameter	Test Method
HB01	H-OUT pulse duty	(1) No signal input. (2) Measure T1 and T2 (as shown in figure below) from pin 26 (H-OUT) output waveform when sub-address (00) data is 80H and A0H. Determine duties TH_{00A} and TH_{00B} using the following formula: $TH = T1/(T1 + T2) \times 100$ % (3) Set sub-address (00) data to 81H, A1H, 82H and A2H, measure as in step (2) above, and determine duties TH_{01A}, TH_{01B}, TH_{10A} and TH_{10B}. 
HB02	Horizontal free-running frequency	(1) Set SW20 to open. (2) Set sub-address (00) data to 00H and measure horizontal free-running frequency F00 from pin 26 (H-OUT) output waveform. (3) Set sub-address (00) data to 40H, 80H and C0H, measure as in step (2) above, horizontal free-running frequencies F01, F10 and F11.
HB03	Horizontal oscillation frequency variable range	(1) Set sub-address (00) data to 00H. (2) Connect 10-kΩ resistor between pin 20 and V_{CC}. Measure horizontal frequency $F00_{MIN}$ from pin 26 (H-OUT) output waveform. (3) Connect 68-kΩ resistor between pin 20 and GND. Measure horizontal frequency $F00_{MAX}$ from pin 26 (H-OUT) output waveform. (4) Set sub-address (00) data to 40H, 80H and C0H, and measure as in steps (2) and (3) above, horizontal frequencies $F01_{MIN}$, $F01_{MAX}$, $F10_{MIN}$, $F10_{MAX}$, $F11_{MIN}$ and $F11_{MAX}$.
HB04	Horizontal oscillation control sensitivity	(1) Set SW20 to open. (2) Connect external power supply to TP20. Set sub-address (00) data to 00H. Apply $V_{20} + 0.05$ V and $V_{20} - 0.05$ V (see HB01) to TP20, and measure frequencies FA and FB from pin 26 (H-OUT) output waveform. Calculate frequency change rate (BH00) using the following formula. (3) Set sub-address (00) data to 40H, 80H and C0H, measure as in step (2) above, and calculate frequency change rates BH01, BH10 and BH11.
HB05	H-OUT output voltage	(1) Set SW20 to open. (2) Measure high ($V15_H$) and low ($V15_L$) voltages of pin 26 (H-OUT) output waveform.

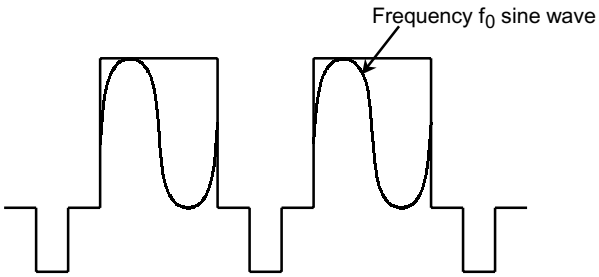
Note No.	Parameter	Test Method
V01	VP output pulse width Vertical free-running (maximum pull-in range)	(1) Input signal d (as shown in figure below) to TP16 and signal e (as shown in figure below) to pin 24 (FBP IN). (2) Measure VP output pulse width (VP_W) from TP27 output waveform. (3) Measure VP pull-in range (VP_{t0}) from TP27 output waveform. (4) Set sub-address (03) data to 01H, 02H, 03H, 04H, 05H and 06H and measure, as in step (4) above, pull-in ranges VPt1, VPt2, VPt3, VPt4, VPt5 and VPt6. 
V02	Minimum vertical pull-in range	(1) This is same as step (1) for V01. (2) Input signal f (as shown in figure below) to TP15. (3) Increase signal f cycle from 30H. Measure cycle (T_{VPULL}) when phase locks with that of TP27. 

Note No.	Parameter	Test Method
V03	Vertical black peak detection pulse	(1) This is same as step (1) for V01. (2) Input signal f (as shown in figure below) to TP15. (3) Measure phase differences $VBPP_{0E}$ and $VBPP_{0S}$ from TP18 output waveform. (4) Set sub-address (03) data to 01H, 02H, 03H, 04H, 05H and 06H, and measure as in step (3) above, phase differences $VBPP_{1E}$, $VBPP_{1S}$, $VBPP_{2E}$, $VBPP_{2S}$, $VBPP_{3E}$, $VBPP_{3S}$, $VBPP_{4E}$, $VBPP_{4S}$, $VBPP_{5E}$, $VBPP_{5S}$, $VBPP_{6E}$ and $VBPP_{6S}$. 
V04	Vertical blanking stop phase	(1) This is same as step (1) for V01. (2) Input signal f (as shown in figure below) to TP15. (3) Set sub-address (03) data to 00H and F0H, and measure blanking stop phases $VBLK_{MIN}$ and $VBLK_{MAX}$ from pin 43 output waveform. 

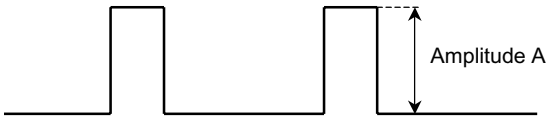
(1) Video signal



(2) Input signal 1



(3) Input signal 2



(4) Input signal 3

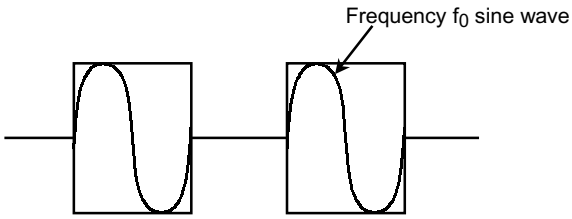


Figure T-1 Test Signals for Text/Color Difference Signal 2

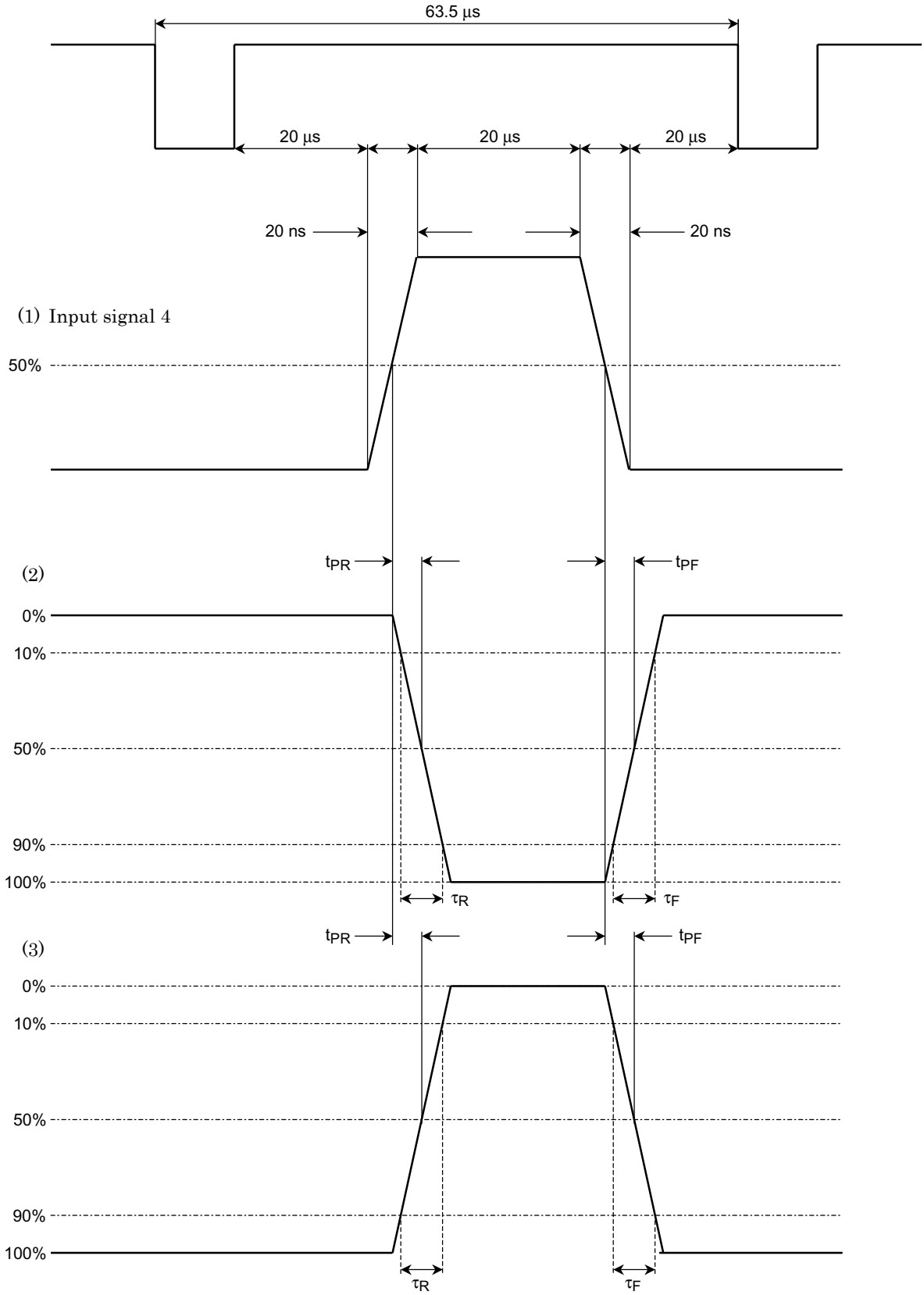
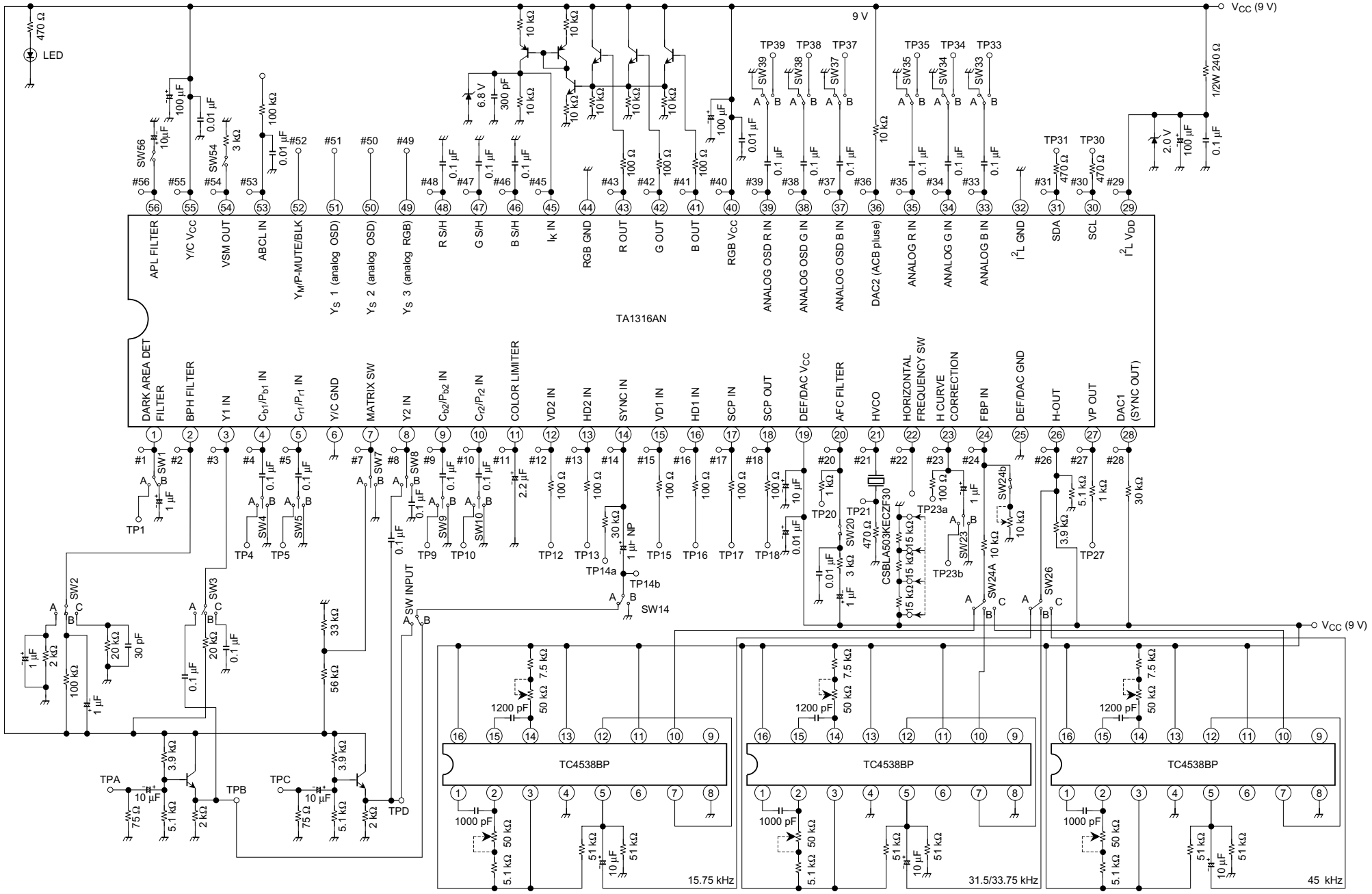
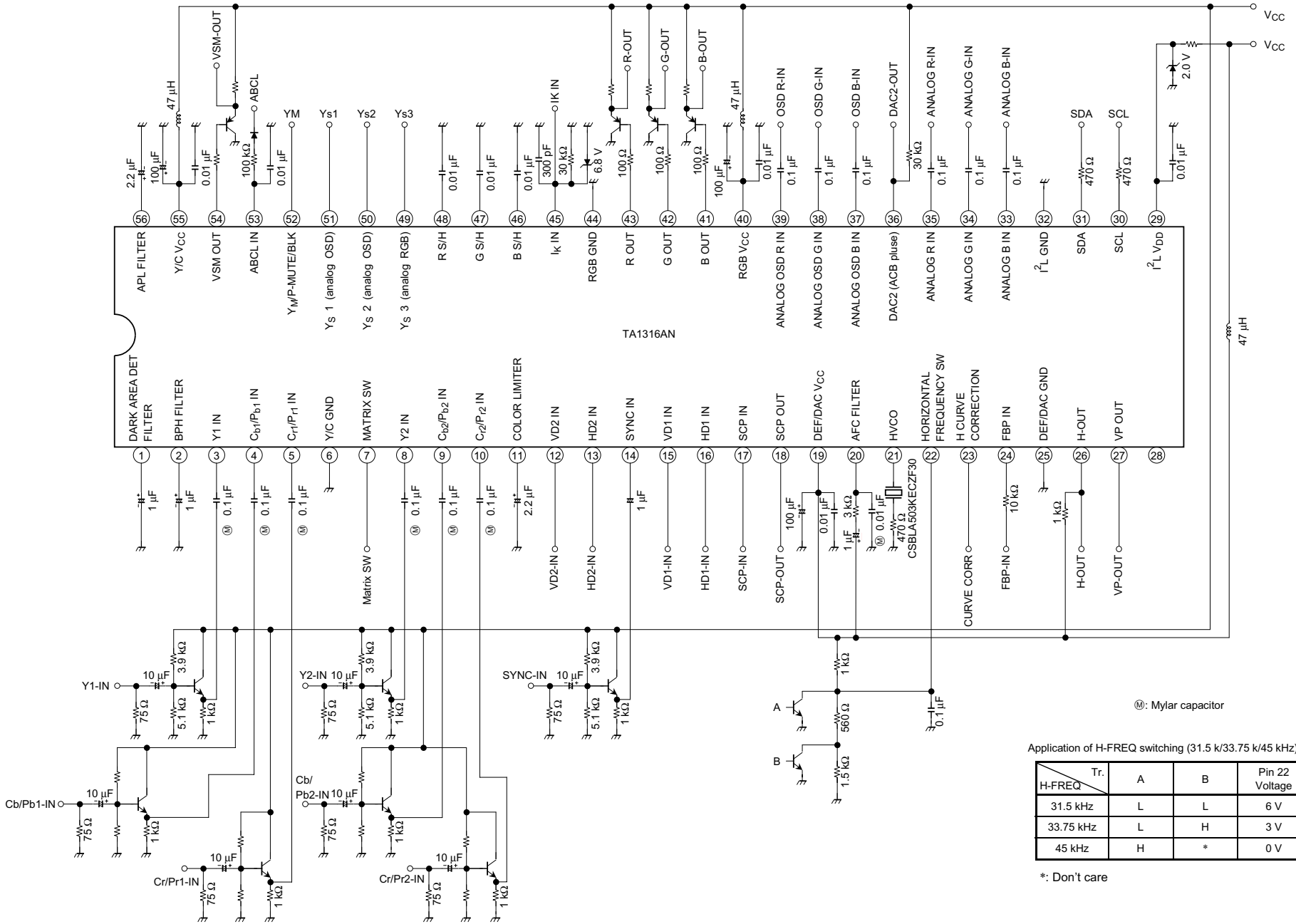


Figure T-2 Test Pulses for Text/Color Difference Signal 2

Test Circuit



Application Circuit

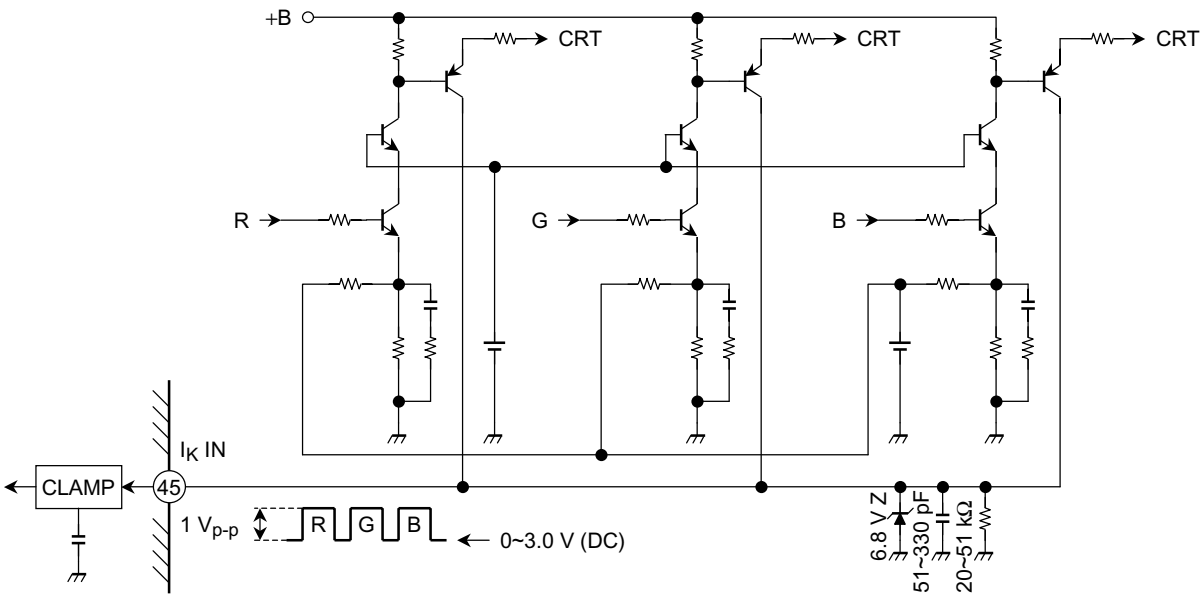


Application of H-FREQ switching (31.5 k/33.75 k/45 kHz)

H-FREQ \ Tr.	A	B	Pin 22 Voltage
31.5 kHz	L	L	6 V
33.75 kHz	L	H	3 V
45 kHz	H	*	0 V

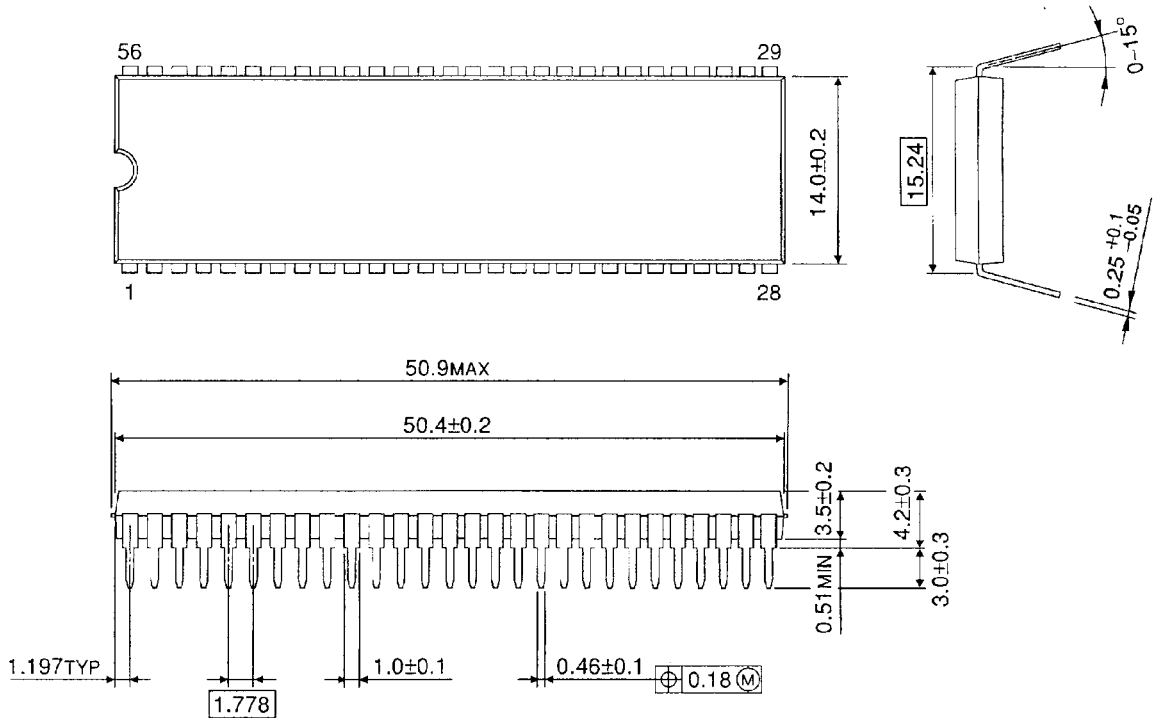
*: Don't care

ACB Application Circuit



Package Dimensions

SDIP56-P-600-1.78 Unit : mm



Weight: 5.55 g (typ.)

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