

FEATURES

- **Monolithic Design for Reliability and Low Cost**
- **High Slew Rate** 0.5V/ μ s
- **Low Droop Rate**
 $T_A = 25^\circ\text{C}$ 0.1mV/ms
 $T_A = 125^\circ\text{C}$ 10mV/ms
- **Low Zero-Scale Error** 4mV
- **Digitally Selected Hold and Reset Modes**
- **Reset to Positive or Negative Voltage Levels**
- **Logic Signals TTL and CMOS Compatible**
- **Uncommitted Comparator on Chip**
- **Available in Die Form**

ORDERING INFORMATION†

25° C V_{ZS} (mV)	PACKAGE	OPERATING TEMPERATURE RANGE
	14-PIN DUAL-IN-LINE PACKAGE	
	HERMETIC*	PLASTIC
4	PKD01AY*	—
4	PKD01EY	—
7	PKD01FY	—
4	—	PKD01EP
7	—	PKD01FP
		COM

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

GENERAL DESCRIPTION

The PKD-01 tracks an analog input signal until a maximum amplitude is reached. The maximum value is then retained as a peak voltage on a hold capacitor. Being a monolithic circuit, the PKD-01 offers significant performance and package density advantages over hybrid modules and discrete designs without sacrificing system versatility. The matching characteristics attained in a monolithic circuit provide inherent advantages when charge injection and droop rate error reduction are primary goals.

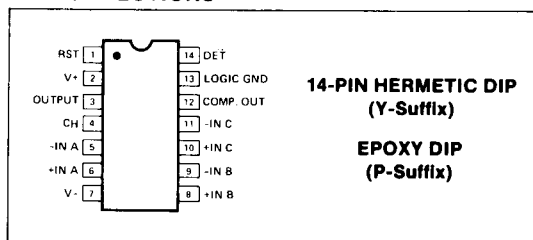
Innovative design techniques maximize the advantages of monolithic technology. Transconductance (g_m) amplifiers were chosen over conventional voltage amplifier circuit building blocks. The " g_m " amplifiers simplify internal frequency compensation, minimize acquisition time and maximize circuit accuracy. Their outputs are easily switched by low glitch current steering circuits. The steered outputs are clamped to reduce charge injection errors upon entering the hold mode or exiting the reset mode. The inherently low zero-scale error is reduced further by active "Zener-Zap" trimming to optimize overall accuracy.

The output buffer amplifier features an FET input stage to reduce droop rate error during lengthy peak hold periods. A bias current cancellation circuit minimizes droop error at high ambient temperatures.

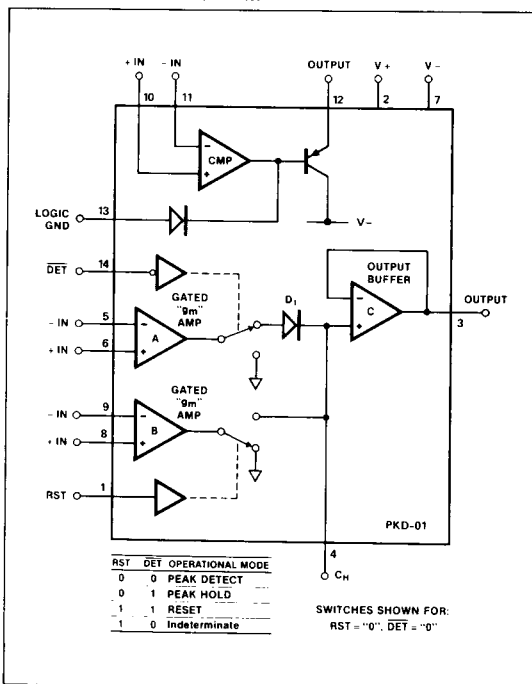
Through the $\overline{\text{DET}}$ control pin, new peaks may either be detected or ignored. Detected peaks are presented as positive output levels. Positive or negative peaks may be detected without additional active circuits since amplifier A can operate as an inverting or noninverting gain stage.

An uncommitted comparator provides many application options. Status indication and logic shaping/shifting are typical examples.

PIN CONNECTIONS



FUNCTIONAL DIAGRAM



PKD-01

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	±18V
Input Voltage	Equal to Supply Voltage
Logic and Logic Ground Voltage	Equal to Supply Voltage
Output Short-Circuit Duration	Indefinite
Amplifier A or B Differential Input Voltage	±24V
Comparator Differential Input Voltage	±24V
Comparator Output Voltage	Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration	Indefinite
Lead Temperature (Soldering, 60 sec)	300°C
Storage Temperature Range	
PKD-01AY, PKD-01EY, PKD-01FY	–65°C to +150°C
PKD-01EP, PKD-01FP	–65°C to +125°C

Operating Temperature Range

PKD-01AY	–55°C to +125°C
PKD-01EY, PKD-01FY	–25°C to +85°C
PKD-01EP, PKD-01FP	0°C to +70°C
Junction Temperature	–65°C to +150°C

PACKAGE TYPE	θ_{JA} (Note 2)	θ_{JC}	UNITS
14-Pin Hermetic DIP (Y)	99	12	°C/W
14-Pin Plastic DIP (P)	76	33	°C/W

NOTES:

1. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
2. θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for CerDIP and P-DIP packages.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g _m " AMPLIFIERS A, B									
Zero-Scale Error	V _{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V _{OS}		—	2	3	—	3	6	mV
Input Bias Current	I _B		—	80	150	—	80	250	nA
Input Offset Current	I _{OS}		—	20	40	—	20	75	nA
Voltage Gain	A _V	R _L = 10kΩ, V _O = ±10V	18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	A _V = 1	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	86	96	—	76	96	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/μs
Feedthrough Error		ΔV _{IN} = 20V, DET = 1, RST = 0, (Note 1)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	41	70	—	41	70	μs
Acquisition Time to 0.01% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	45	—	—	45	—	μs
COMPARATOR									
Input Offset Voltage	V _{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I _B		—	700	1000	—	700	1000	nA
Input Offset Current	I _{OS}		—	75	300	—	75	300	nA
Voltage Gain	A _V	2kΩ Pull-up Resistor to 5V	5	7.5	—	3.5	7.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	76	90	—	76	90	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±11.5	±12.5	—	±11.5	±12.5	—	V

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

3. DET = 1, RST = 0.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2k Ω Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	1.6	10	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_J = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	—	0.01	0.07	—	0.01	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$\overline{DET} = 1$ $R_L = 2.5k$	± 11.5	± 12.5	—	± 11	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	t_S		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PKD-01AY, $-25^\circ C \leq T_A \leq +85^\circ C$ for PKD-01EY, PKD-01FY and $0^\circ C \leq T_A \leq +70^\circ C$ for PKD-01EP, PKD-01FP.

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
"g _m " AMPLIFIERS A, B									
Zero-Scale Error	V _{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V _{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV _{OS}	(Note 1)	—	−9	−24	—	−9	−24	μV/°C
Input Bias Current	I _B		—	160	250	—	160	500	nA
Input Offset Current	I _{OS}		—	30	100	—	30	150	nA
Voltage Gain	A _V	R _L = 10kΩ, V _O = ±10V	7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	−10V ≤ V _{CM} ≤ +10V	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	80	90	—	70	90	—	dB
Input Voltage Range	V _{CM}	(Note 1)	±10	±11	—	±10	±11	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/μs
Acquisition Time to 0.1% Accuracy	t _{aq}	20V Step, A _{VCL} = +1, (Note 1)	—	60	—	—	60	—	μs
COMPARATOR									
Input Offset Voltage	V _{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV _{OS}	(Note 1)	—	−4	−6	—	−4	−6	μV/°C
Input Bias Current	I _B		—	1000	2000	—	1100	2000	nA

PKD-01

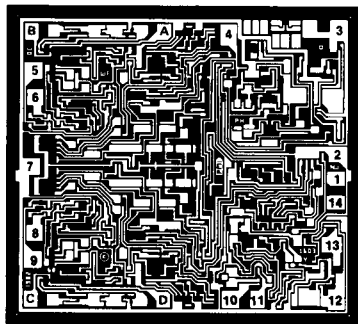
ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55^\circ C \leq T_A \leq +125^\circ C$ for PKD-01AY, $-25^\circ C \leq T_A \leq +85^\circ C$ for PKD-01EY, PKD-01FY and $0^\circ C \leq T_A \leq +70^\circ C$ for PKD-01EP, PKD-01FP. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PKD-01A/E			PKD-01F			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2k Ω Pull-up Resistor to 5V	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \leq V_{CM} \leq +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \leq V_S \leq \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	± 11	—	—	± 11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \leq 5mA$, Logic GND = 0V	-0.2	0.15	0.4	-0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	100	180	μA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_S	5mV Overdrive, 2k Ω Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-RST, DET (See Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	μA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	μA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_J = Max. Operating Temp T_A = Max. Operating Temp. DET = 1, (Note 2)	—	1.2	10	—	3	15	mV/ms
			—	2.4	20	—	6	20	
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	± 12	—	± 10.5	± 12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/ μs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.
3. DET = 1, RST = 0.

DICE CHARACTERISTICS



1. RST (RESET CONTROL)
2. V+
3. OUTPUT
4. C_H (HOLD CAPACITOR)
5. INVERTING INPUT (A)
6. NONINVERTING INPUT (A)
7. V-
8. NONINVERTING INPUT (B)
9. INVERTING INPUT (B)
10. COMPARATOR NONINVERTING INPUT
11. COMPARATOR INVERTING INPUT
12. COMPARATOR OUTPUT
13. LOGIC GROUND
14. DET (PEAK DETECT CONTROL)
A,B (A) NULL
C,D (B) NULL

DIE SIZE 0.101 × 0.091 inch, 9191 sq. mils
(2.565 × 2.311mm, 5.93 sq mm)

WAFER TEST LIMITS at V_S = ±15V, C_H = 1000pF, T_A = 25° C.

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V _{ZS}		7	mV MAX
Input Offset Voltage	V _{OS}		6	mV MAX
Input Bias Current	I _B		250	nA MAX
Input Offset Current	I _{OS}		75	nA MAX
Voltage Gain	A _V	R _L = 10kΩ, V _O = ±10V	10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	-10V ≤ V _{CM} ≤ +10V	74	dB MIN
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	76	dB MIN
Input Voltage Range	V _{CM}	(Note 1)	±11.5	V MIN
Feedthrough Error		ΔV _{IN} = 20V, DET = 1, RST = 0, (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V _{OS}		3	mV MAX
Input Bias Current	I _B		1000	nA MAX
Input Offset Current	I _{OS}		300	nA MAX
Voltage Gain	A _V	2kΩ Pull-up Resistor to 5V, (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	-10V ≤ V _{CM} ≤ +10V	82	dB MIN
Power Supply Rejection Ratio	PSRR	±9V ≤ V _S ≤ ±18V	76	dB MIN
Input Voltage Range	V _{CM}	(Note 1)	±11.5	V MIN
Low Output Voltage	V _{OL}	I _{SINK} ≤ 5mA, Logic GND = 5V	0.4 -0.2	V MAX V MIN
"OFF" Output Leakage Current	I _L	V _{OUT} = 5V	80	μA MAX
Output Short- Circuit Current	I _{SC}	V _{OUT} = 5V	45 7	mA MAX mA MIN

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The

warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperature. Ambient (T_A) temperature specifications are not subject to production testing.

3. DET = 1, RST = 0.

PKD-01

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25^\circ C$. (Continued)

PARAMETER	SYMBOL	CONDITIONS	PKD-01N LIMIT	UNITS
DIGITAL INPUTS-RST, DET (See Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	μA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	μA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_J = 25^\circ C$, $T_A = 25^\circ C$ (See Note 2)	0.1	mV/ms MAX
			0.20	mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40	mA MAX
			7	mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:

1. Guaranteed by design.
2. Due to limited production test times, the droop current corresponds to junction temperature (T_J). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_J) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures. Ambient (T_A) temperature specifications are not subject to production testing.
3. DET = 1, RST = 0.

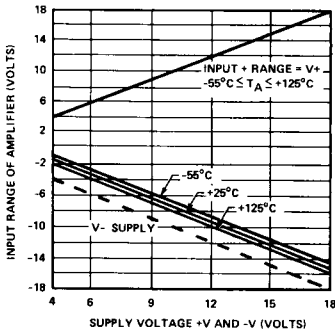
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, and $T_A = 25^\circ C$, unless otherwise noted.

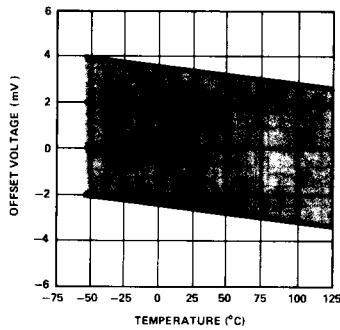
PARAMETER	SYMBOL	CONDITIONS	PKD-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/ μs
Acquisition Time	t_a	0.1% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	41	μs
Acquisition Time	t_a	0.01% Accuracy, 20V step, $A_{VCL} = 1$, (Note 1)	45	μs
COMPARATOR				
Response Time		5mV Overdrive, 2k Ω Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperature Time	t_{ap}		75	ns
Switching Time	t_s		50	ns
Buffer Slew Rate	SR	$R_L = 2.5k\Omega$	2.5	V/ μs

TYPICAL PERFORMANCE CHARACTERISTICS

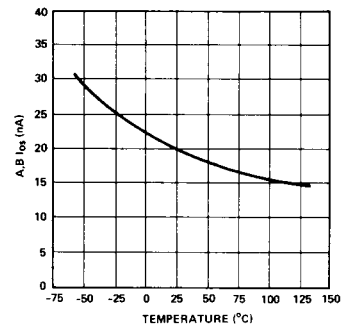
A AND B INPUT RANGE vs SUPPLY VOLTAGE



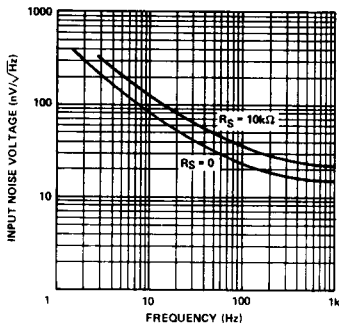
A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE



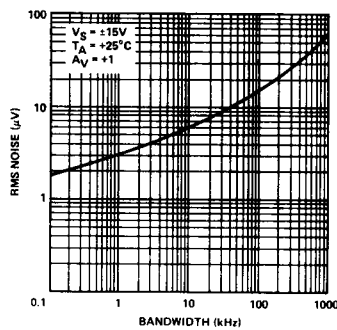
A, B I_{OS} vs TEMPERATURE



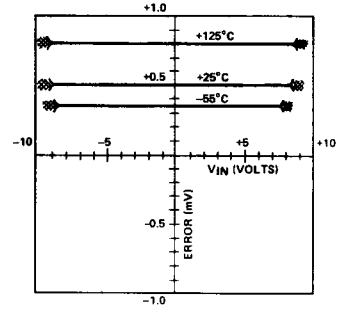
INPUT SPOT NOISE vs FREQUENCY



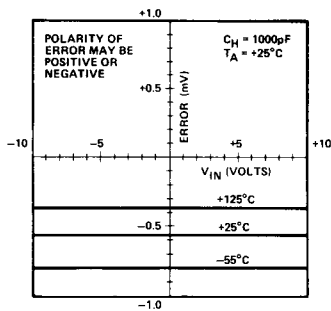
WIDEBAND NOISE vs BANDWIDTH



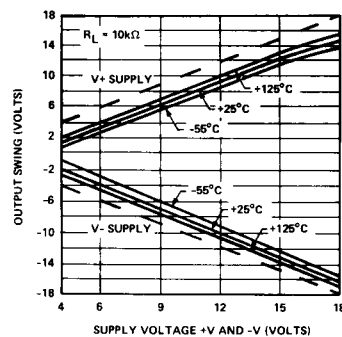
AMPLIFIER B CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



AMPLIFIER A CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE

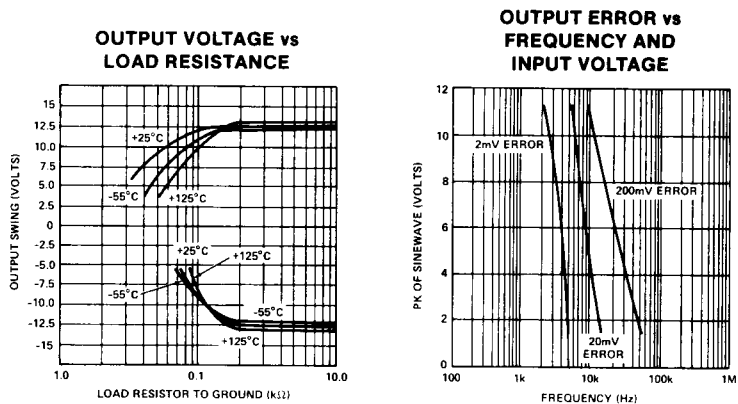


OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)

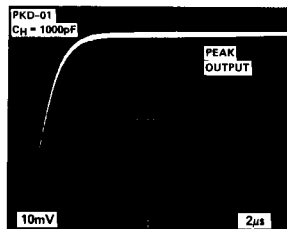


PKD-01

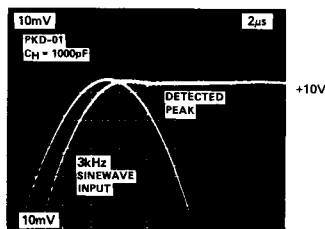
TYPICAL PERFORMANCE CHARACTERISTICS



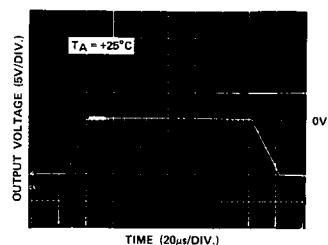
PKD-01 SETTLING RESPONSE



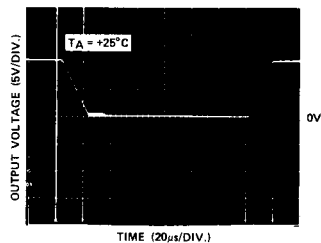
PKD-01 SETTLING RESPONSE



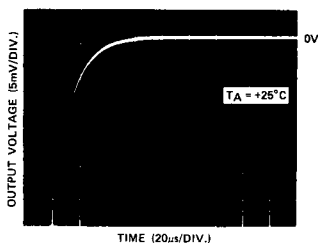
**LARGE-SIGNAL
INVERTING RESPONSE**



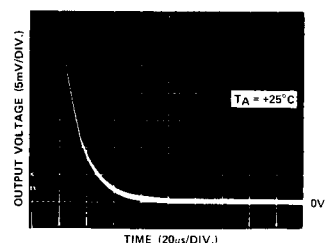
**LARGE-SIGNAL
NONINVERTING RESPONSE**



**SETTLING TIME FOR -10V
TO 0V STEP INPUT**

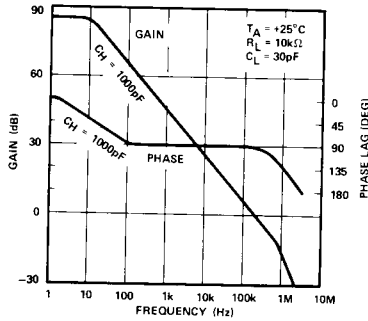


**SETTLING TIME FOR +10V
TO 0V STEP INPUT**

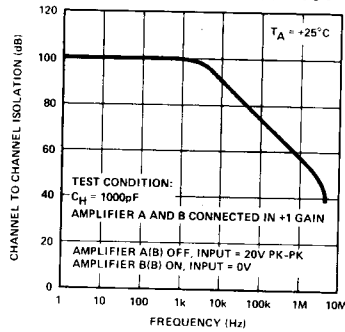


TYPICAL PERFORMANCE CHARACTERISTICS

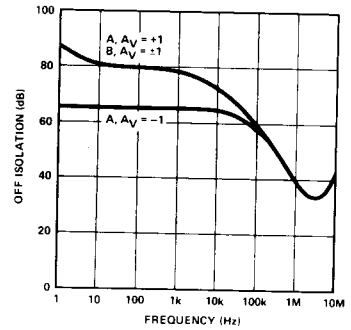
SMALL-SIGNAL OPEN LOOP GAIN/PHASE vs FREQUENCY



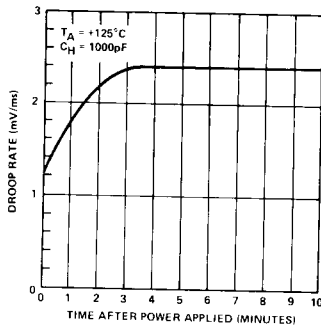
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



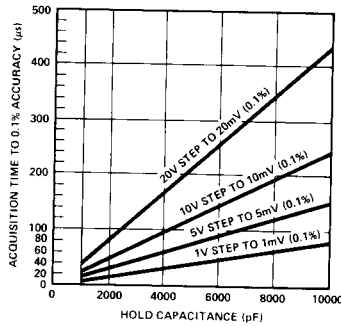
OFF ISOLATION vs FREQUENCY



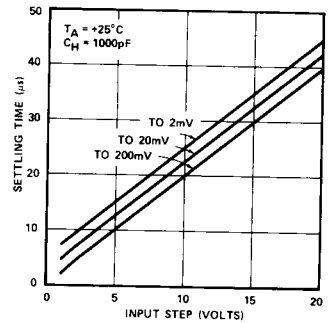
DROOP RATE vs TIME AFTER POWER ON



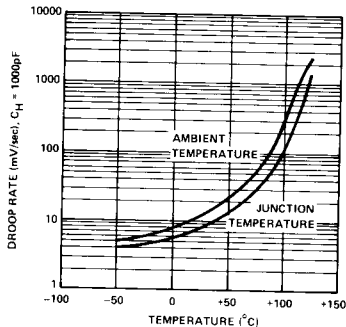
ACQUISITION TIME vs EXTERNAL HOLD CAPACITOR AND ACQUISITION STEP



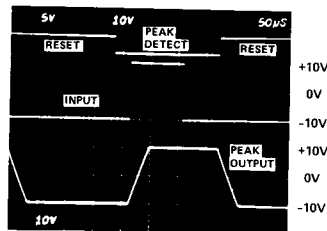
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



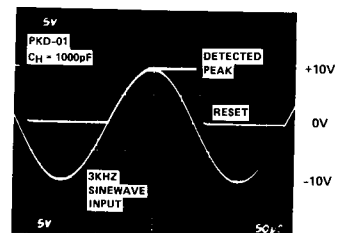
DROOP RATE vs TEMPERATURE



ACQUISITION OF STEP INPUT

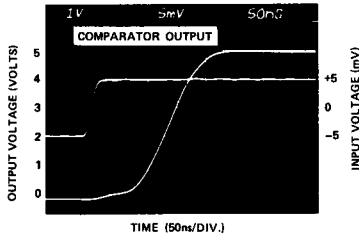


ACQUISITION OF SINEWAVE PEAK

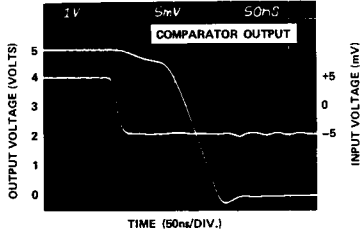


TYPICAL PERFORMANCE CHARACTERISTICS

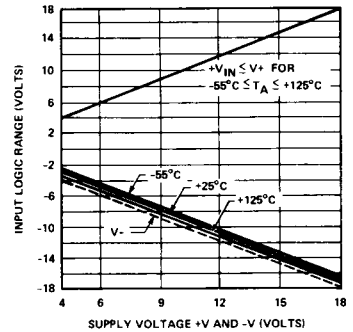
**COMPARATOR OUTPUT
RESPONSE TIME**
(2k Ω PULL-UP RESISTOR, $T_A = +25^\circ\text{C}$)



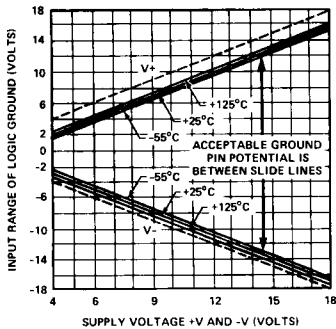
**COMPARATOR OUTPUT
RESPONSE TIME**
(2k Ω PULL-UP RESISTOR, $T_A = +25^\circ\text{C}$)



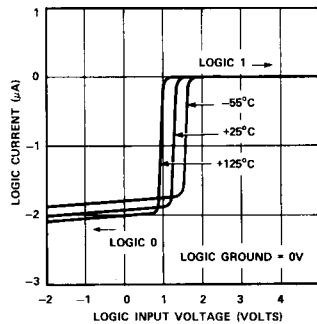
**INPUT LOGIC RANGE vs
SUPPLY VOLTAGE**



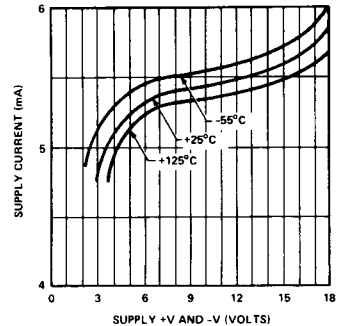
**INPUT RANGE OF LOGIC
GROUND vs SUPPLY VOLTAGE**



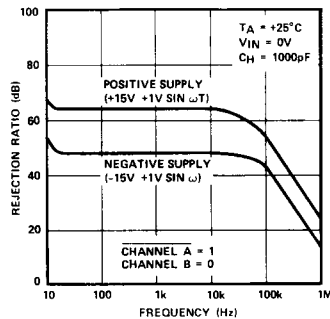
**LOGIC INPUT CURRENT vs
LOGIC INPUT VOLTAGE**



**SUPPLY CURRENT vs
SUPPLY VOLTAGE**

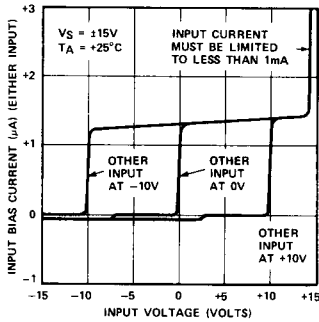


**HOLD MODE POWER SUPPLY
REJECTION vs FREQUENCY**

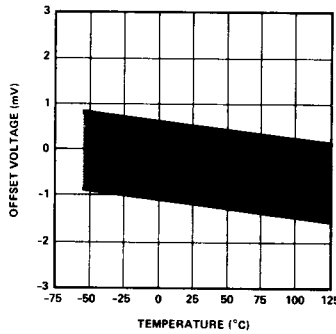


TYPICAL PERFORMANCE CHARACTERISTICS

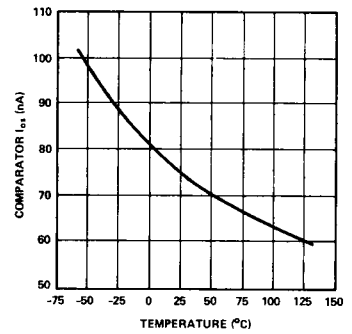
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



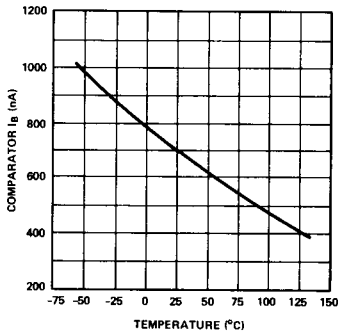
COMPARATOR OFFSET VOLTAGE vs TEMPERATURE



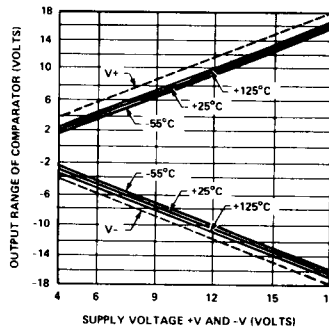
COMPARATOR I_{OS} vs TEMPERATURE



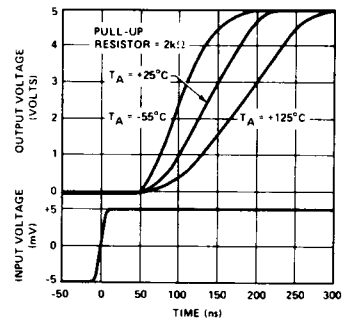
COMPARATOR I_B vs TEMPERATURE



OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE

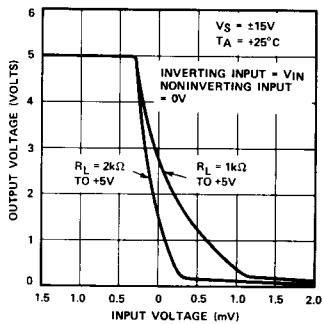


COMPARATOR RESPONSE TIME vs TEMPERATURE

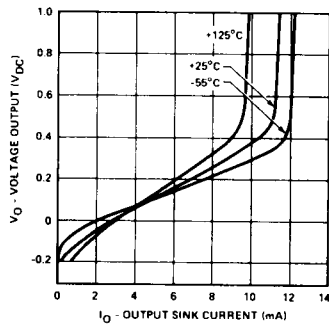


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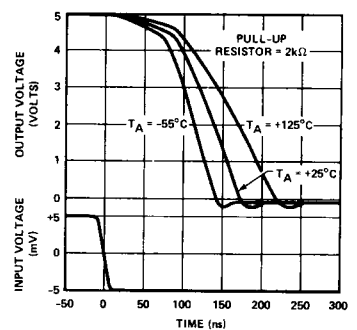
COMPARATOR TRANSFER CHARACTERISTIC



COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



COMPARATOR RESPONSE TIME vs TEMPERATURE



THEORY OF OPERATION

The typical peak detector uses voltage amplifiers and a diode or an emitter follower to charge the hold capacitor, C_H , unidirectionally (Figure 1). The output impedance of A plus D_1 's dynamic impedance, r_d , make up the resistance which determines the feedback loop pole. The dynamic impedance is $r_d = \frac{kT}{qI_d}$. I_d is the capacitor charging current.

The pole moves toward the origin of the S plane as I_d goes to zero. The pole movement in itself will not significantly lengthen the acquisition time since the pole is enclosed in the system feedback loop.

When the moving pole is considered with the typical frequency compensation of voltage amplifiers there is however, a loop stability problem. The necessary compensation can increase the required acquisition time. PMI's approach replaces the input voltage amplifier with a transconductance amplifier; Figure 2.

The PKD-01 transfer function can be reduced to:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 + \frac{sC_H}{g_m} + \frac{1}{g_m R_{OUT}}} \approx \frac{1}{1 + \frac{sC_H}{g_m}}$$

Where: $g_m \approx 1 \mu A/mV$, $R_{OUT} \approx 20 M\Omega$.

The diode in series with A's output (Figure 2) has no effect because it is a resistance in series with a current source. In addition to simplifying the system compensation, the input transconductance amplifier output current is switched by current steering. The steered output is clamped to reduce and match any charge injection.

Fig. 3 shows a simplified schematic of the reset "g_m" amplifier, B. In the track mode, Q₁ & Q₄ are ON and Q₂ & Q₃ are OFF. A current of 2I passes through D₁, I is summed at "B" and passes through Q₁, and is summed with g_mV_{IN}. The current sink can absorb only 3I, thus, the current passing through D₂ can only be: 2K - g_mV_{IN}. The net current into the hold capacitor node then is, g_mV_{IN} (C_H = 2I - (2I - g_mV_{IN})). The hold mode, Q₂ & Q₃ are ON while Q₁ & Q₄ are OFF. The net current into the top of D₁ is -I until D₃ turns ON. With Q₁ OFF, the bottom of D₂ is pulled up with a current I until D₄ turns ON, thus D₁ & D₂ are reverse biased by ≈0.6V and charge injection is independent of input level.

The monolithic layout results in points A and B having equal nodal capacitance. In addition, matched diodes D_1 and D_2 have equal diffusion capacitance. When the transconductance amplifier outputs are switched open, points A and B are ramped equally but in opposite phase. Diode clamps D_3 and D_4 cause the swings to have equal amplitudes. The net charge injection (voltage change) at node C is therefore zero.

The peak transconductance amplifier, A, is shown in Figure 4. Unidirectional hold capacitor charging requires diode D_1 to be connected in series with the output. Upon entering the peak hold mode D_1 is reverse biased. The voltage clamp limits charge injection to approximately 1pC and the hold step to 0.6mV.

Minimizing acquisition time dictated a small C_H capacitance. A 1000 pF value was selected. Droop rate was also minimized

by providing the output buffer with an FET input stage. A current cancellation circuit further reduces droop current and minimizes the gate current's tendency to double for every 10°C temperature change.

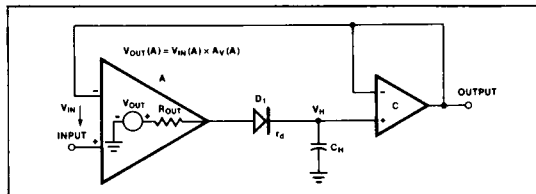


Figure 1. Conventional Voltage Amplifier Peak Detector

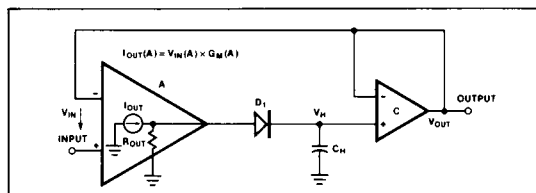


Figure 2. Transconductance Amplifier Peak Detector

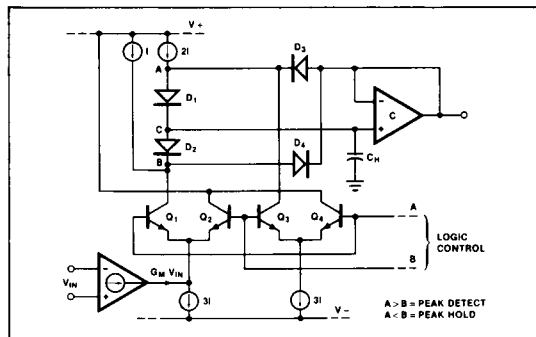


Figure 3. Transconductance Amplifier with Low Glitch Current Switch

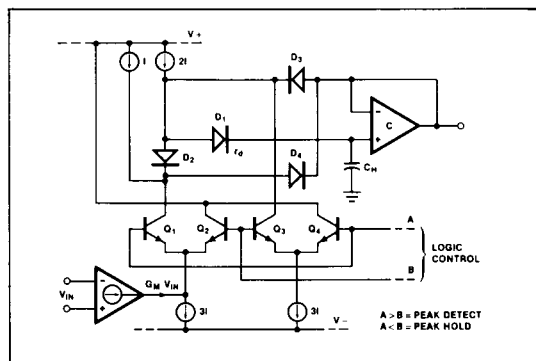


Figure 4. Peak Detecting Transconductance Amplifier with Switched Output

APPLICATIONS INFORMATION

OPTIONAL OFFSET VOLTAGE ADJUSTMENT

Offset voltage is the primary zero scale error component since a variable voltage clamp limits voltage excursions at D_1 's anode and reduces charge injection. The PKD-01 circuit gain and operational mode (positive or negative peak detection) determine the applicable null circuit. Figures A through D are suggested circuits. Each circuit corrects amplifier C offset voltage error also.

A. NULLING GATED OUTPUT g_m AMPLIFIER A. Diode D_1 must be conducting to close the feedback circuit during

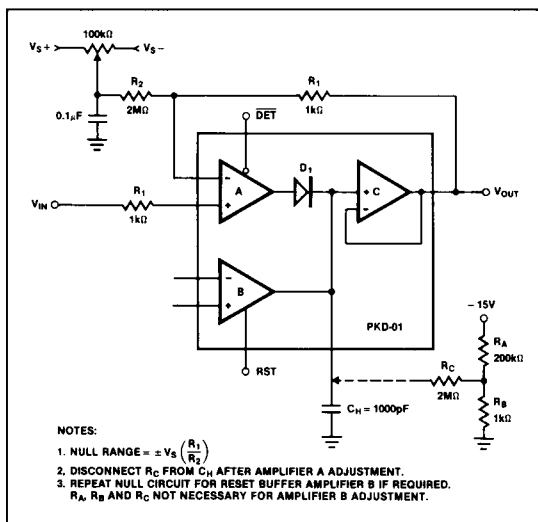


Figure A. V_{OS} Null Circuit for Unity Gain Positive Peak Detector

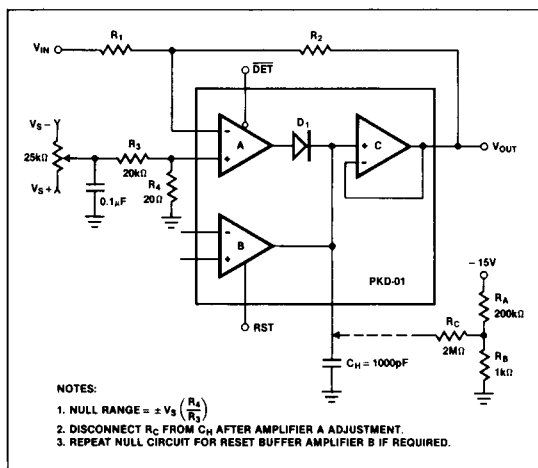


Figure C. V_{OS} Null Circuit for Negative Peak Detector

amplifier A V_{OS} adjustment. Resistor network $R_A - R_C$ cause D_1 to conduct slightly. With $DET = 0$ and $V_{IN} = 0V$ monitor the PKD-01 output. Adjust the null potentiometer until $V_{OUT} = 0V$. After adjustment, disconnect R_C from C_H .

B. NULLING GATED g_m AMPLIFIER B. Set amplifier B signal input to $V_{IN} = 0V$ and monitor the PKD-01 output. Set $DET = 1$, $RST = 1$ and adjust the null potentiometer for $V_{OUT} = 0V$. The circuit gain — inverting or noninverting — will determine which null circuit illustrated in Figures A through D is applicable.

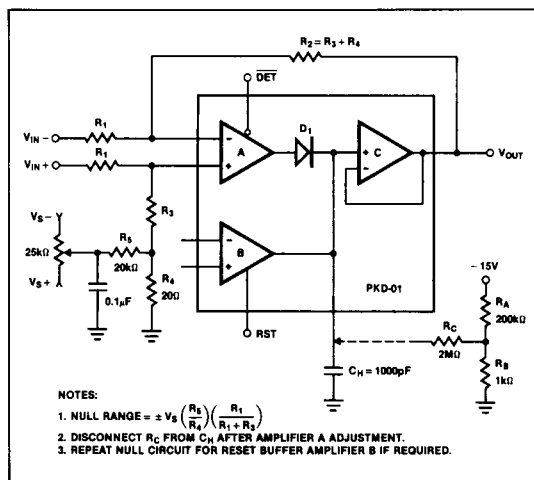


Figure B. V_{OS} Null Circuit for Differential Peak Detector

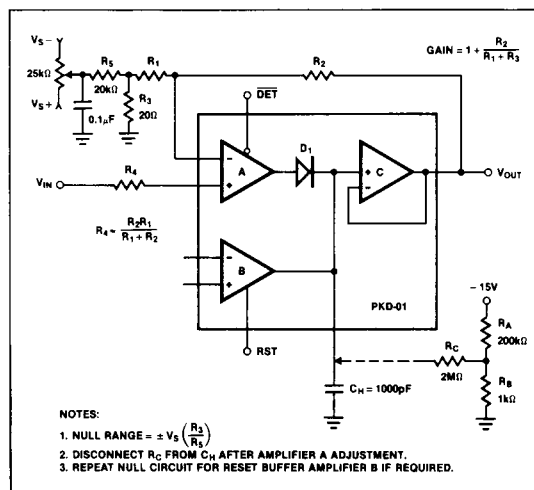


Figure D. V_{OS} Null Circuit for Positive Peak Detector With Gain

PKD-01

PEAK HOLD CAPACITOR RECOMMENDATIONS

The hold capacitor (C_H) serves as the peak memory element and compensating capacitor. Stable operation requires a minimum value of 1000pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase.

Zero scale error is internally trimmed for $C_H = 1000\text{pF}$. Other C_H values will cause a zero scale shift which can be approximated with the following equation.

$$\Delta V_{ZS}(\text{mV}) = \frac{1 \times 10^3(\text{pC})}{C_H(\text{nF})} - 0.6\text{mV}$$

The peak hold capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85°C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the PKD-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

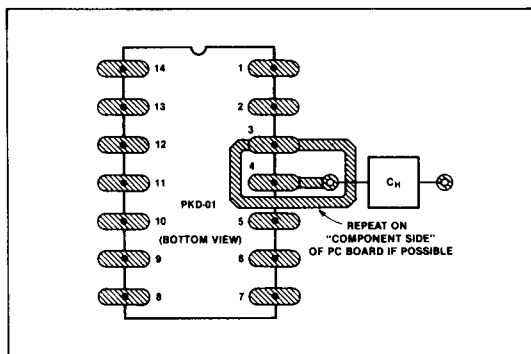


Figure 2. C_H terminal (Pin 4) guarding. See text.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

The maximum comparator high output voltage (V_{OH}) should be limited to:

$$V_{OH}(\text{maximum}) < V^+ - 2.0\text{V}$$

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1 .

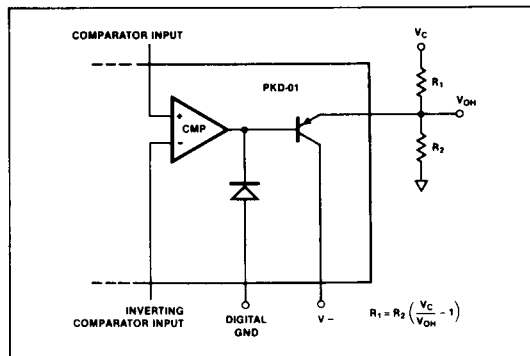


Figure 1

Table I.

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{SINK}}$$

$$R_2 \approx \left(\frac{1}{\frac{V_C}{V_{OH}} - 1} \right)$$

PEAK DETECTOR LOGIC CONTROL (RST, DET)

The transconductance amplifier outputs are controlled by the digital logic signals RST and DET. The PKD-01 operational mode is selected by steering the current (I_1) through Q_1 and Q_2 , thus providing high-speed switching and a predictable logic threshold. The logic threshold voltage is 1.4 volts when digital ground is at zero volts.

Other threshold voltages (V_{TH}) may be selected by applying the formula:

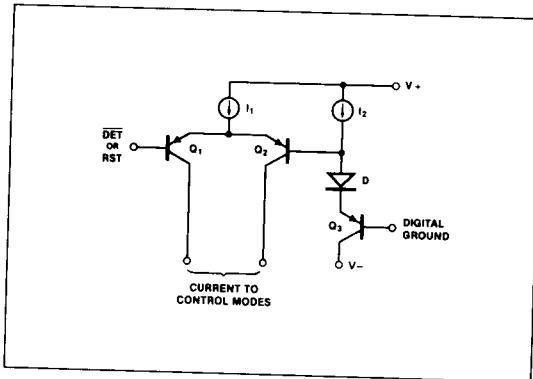
$$V_{TH} \approx 1.4\text{V} + \text{Digital Ground Potential.}$$

For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The RST or DET signal must always be at least 2.8V above the negative supply.

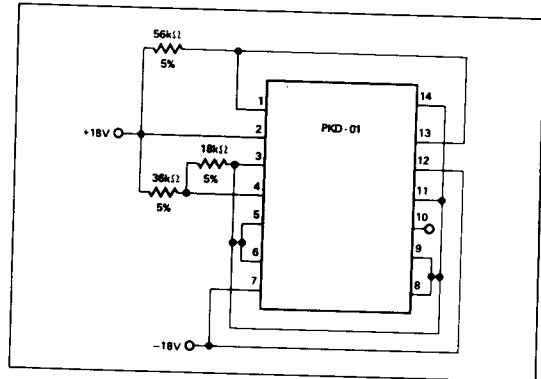
Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$$V_{OL} \approx 0.2\text{V} + \text{Digital Ground Potential.}$$

PKD-01 LOGIC CONTROL

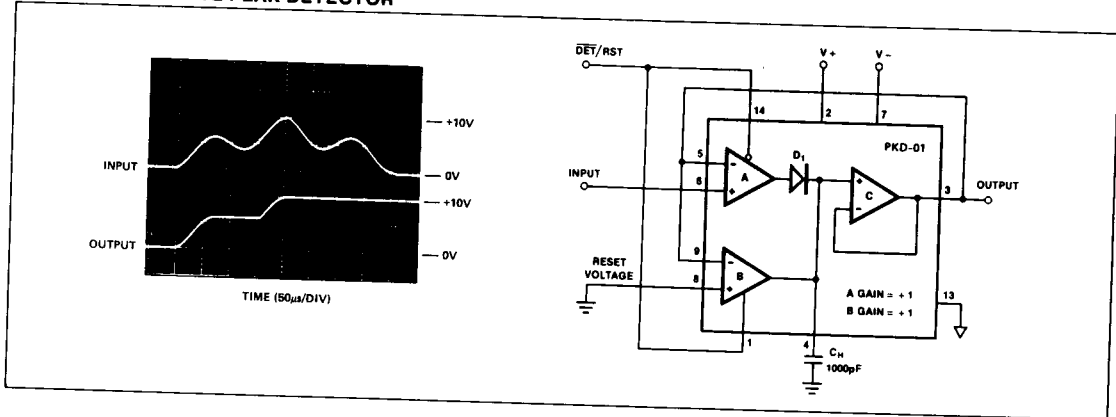


BURN-IN CIRCUIT



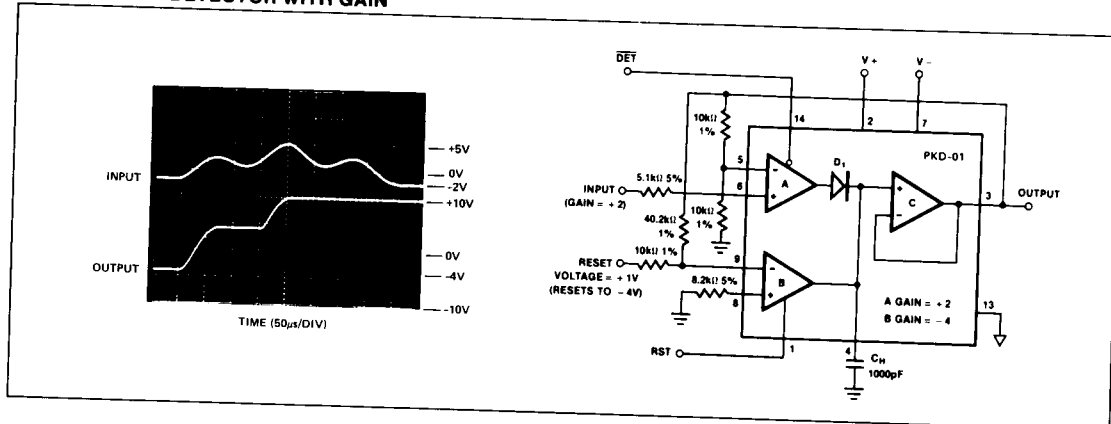
TYPICAL CIRCUIT CONFIGURATIONS

UNITY GAIN POSITIVE PEAK DETECTOR



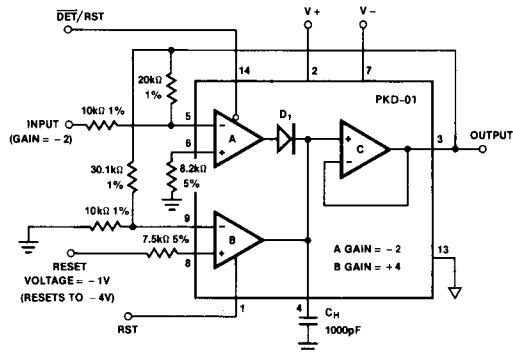
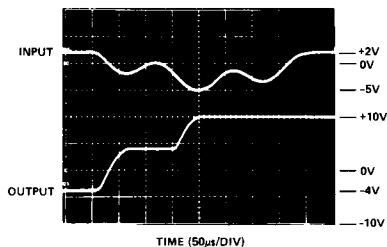
7

POSITIVE PEAK DETECTOR WITH GAIN

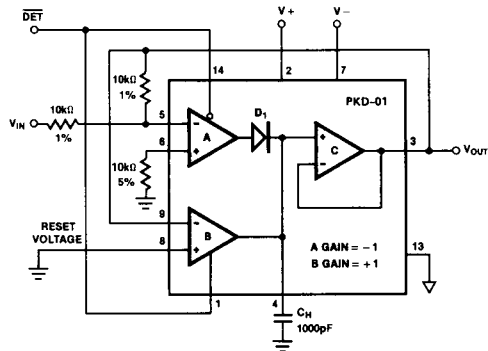
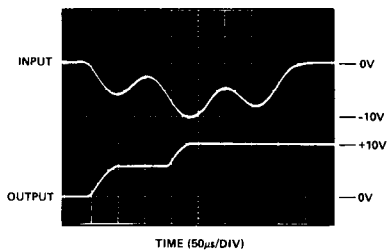


PKD-01

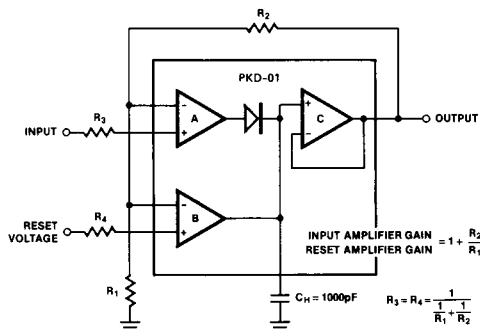
NEGATIVE PEAK DETECTOR WITH GAIN



UNITY GAIN NEGATIVE PEAK DETECTOR



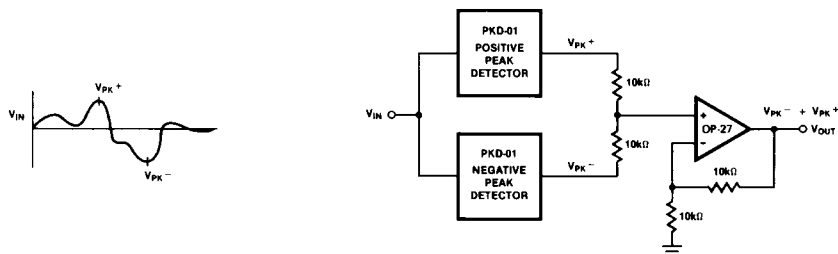
ALTERNATE GAIN CONFIGURATION



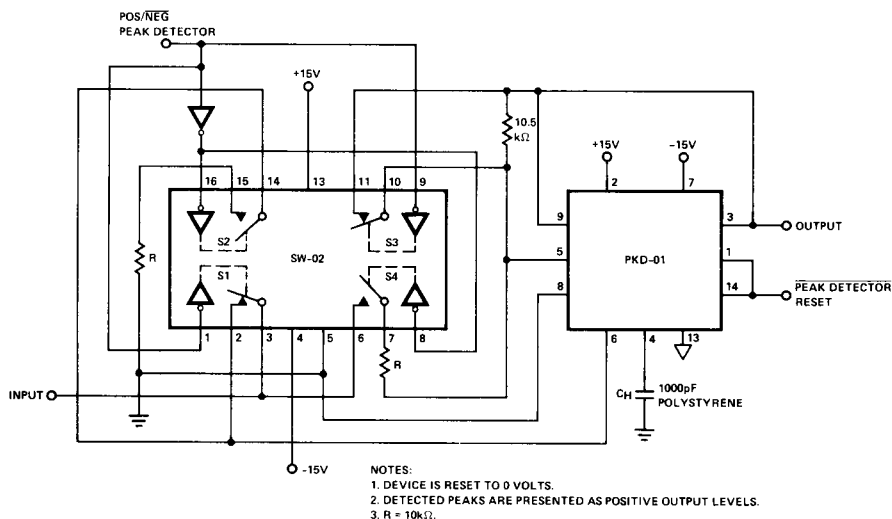
IF BOTH INPUT SIGNAL (AMPLIFIER A INPUT) AND THE RESET VOLTAGE (AMPLIFIER B INPUT) HAVE THE SAME POSITIVE VOLTAGE GAIN THE GAIN CAN BE SET BY A SINGLE VOLTAGE DIVIDER FOR BOTH INPUT AMPLIFIERS.

NOTE:
R1, R2, R3 AND R4 > 5kΩ

PEAK-TO-PEAK DETECTOR

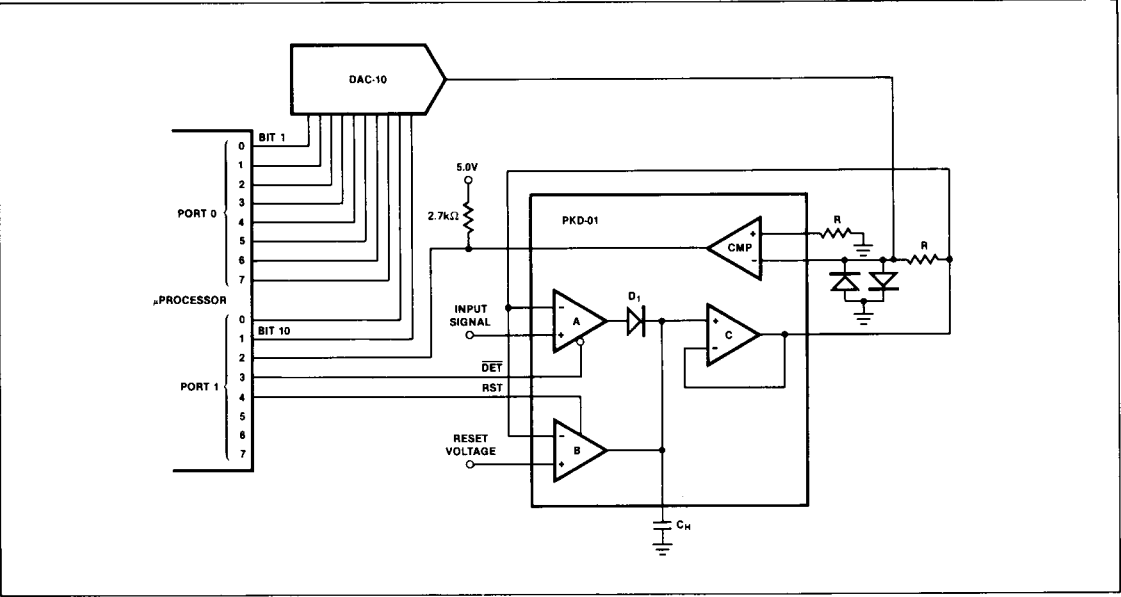


LOGIC SELECTABLE POSITIVE OR NEGATIVE PEAK DETECTOR

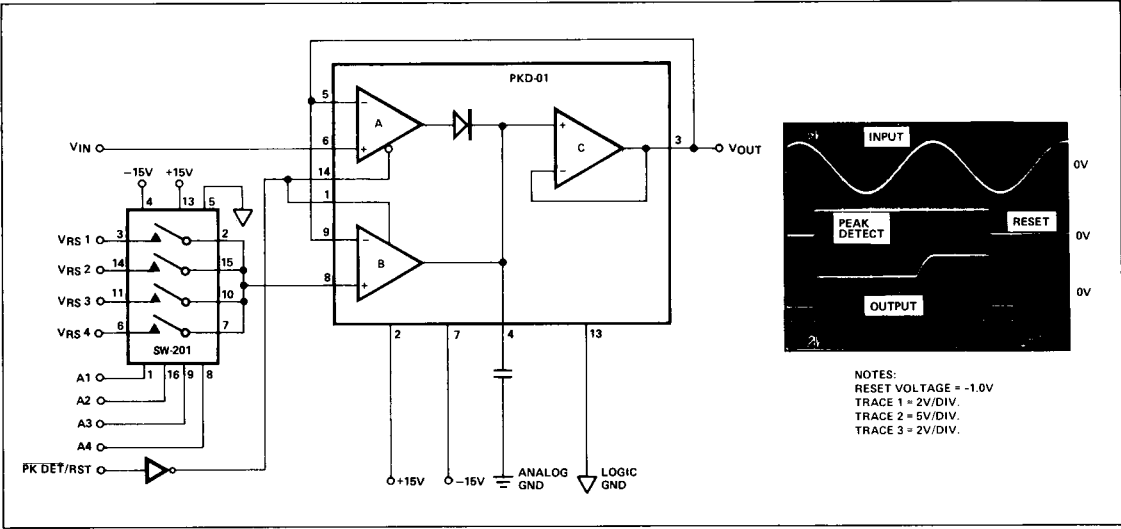


PKD-01

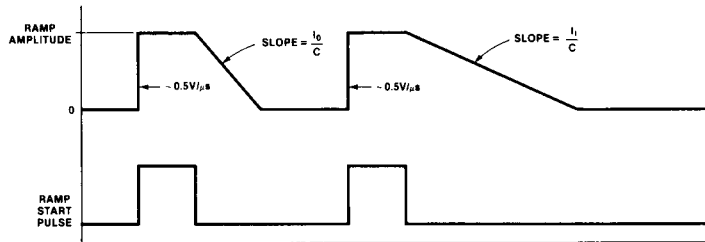
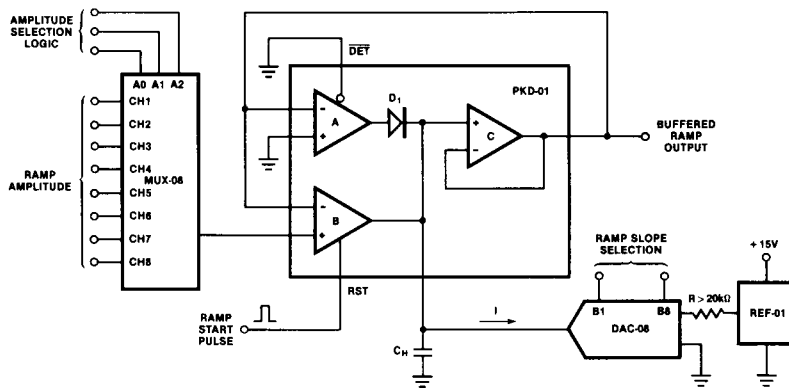
PEAK READING A/D CONVERTER



POSITIVE PEAK DETECTOR WITH SELECTABLE RESET VOLTAGE



PROGRAMMABLE LOW FREQUENCY RAMP GENERATOR



- NOTES:
1. NEGATIVE SLOPE OF RAMP IS SET BY DAC-08 OUTPUT CURRENT.
 2. DAC-08 IS DIGITALLY CONTROLLED CURRENT GENERATOR.
- THE MAXIMUM FULL SCALE CURRENT MUST BE LESS THAN 0.5mA.