Signetics

8X310

Interrupt Control Coprocessor

Product Specification

Military
Customer Specific Products

FEATURES

- **Three prioritized interrupts**
- **Subroutine handling capabilities**
- **4-level LIFO stack for return address storage**
- **Interrupt masking by software and hardware**
- **Stack full flag**
- **Directly compatible with 8X305 Microcontroller**
- **Bipolar ISL (Integrated Schottky Logic) and low-power Schottky technology**
- **Single +5V power supply**
- **0.6", 40-pin DIP**

PRODUCT DESCRIPTION

The Signetics 8X310 Interrupt Control Coprocessor (ICC) supports the 8X305 Microcontroller in systems that are interrupt driven and those that require subroutine handling capabilities.

As shown in Figure 1, the ICC provides three prioritized interrupt request lines, INT 0 (highest priority), INT 1 and INT 2. A Low-to-High transition applied to any of these input lines latches in an interrupt request which may be serviced when sampled by the ICC once each instruction cycle of the Microcontroller. When an interrupt request is serviced, the ICC forces the Microcontroller to jump to one of three fixed locations in program memory; instruction addresses 4, 5, and 6 correspond to INT 0, INT 1, and INT 2. At each of these addresses, the user programs a JMP instruction to another address where the user's interrupt service routine begins.

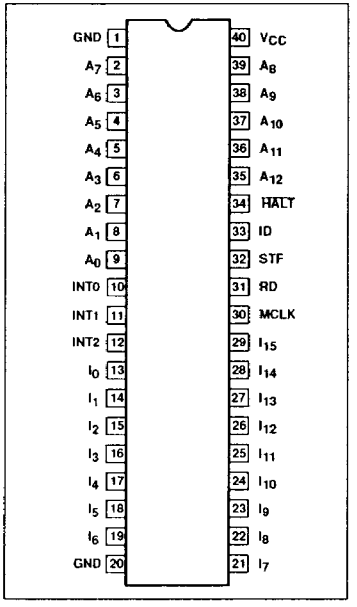
During interrupt servicing, the ICC also stores the proper return address into a four deep, Last-In-First-Out (LIFO) stack. At the conclusion of the interrupt service routine, the user program instructs the ICC to return to the main program at the location previously stored in the stack. The return operation is implemented by coding a special RETURN instruction which is decoded directly off the instruction bus by the ICC. There are five such special instructions relating to interrupt and subroutine handling functions performed by the ICC. These instruction codes are all treated as non- operational instructions (NOPs) by the Microcontroller.

An internal one-bit mask is used to inhibit interrupt servicing. Whenever the mask is set, the ICC does not respond to any pending interrupt requests, however, any requests remain latched for future servicing. The mask can be set and cleared either by the user program or automatically during certain ICC functions. The special instructions SET MASK and CLEAR MASK are provided for user control. The Interrupt Disable input also inhibits interrupt request servicing.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
40–Pin DIP	8X310/BQA

PIN CONFIGURATION



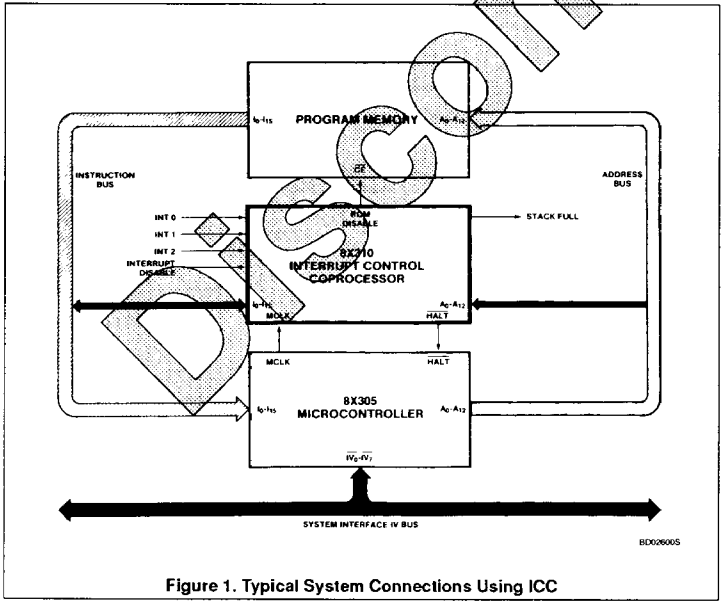


Figure 1. Typical System Connections Using ICC

Packaging Information

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SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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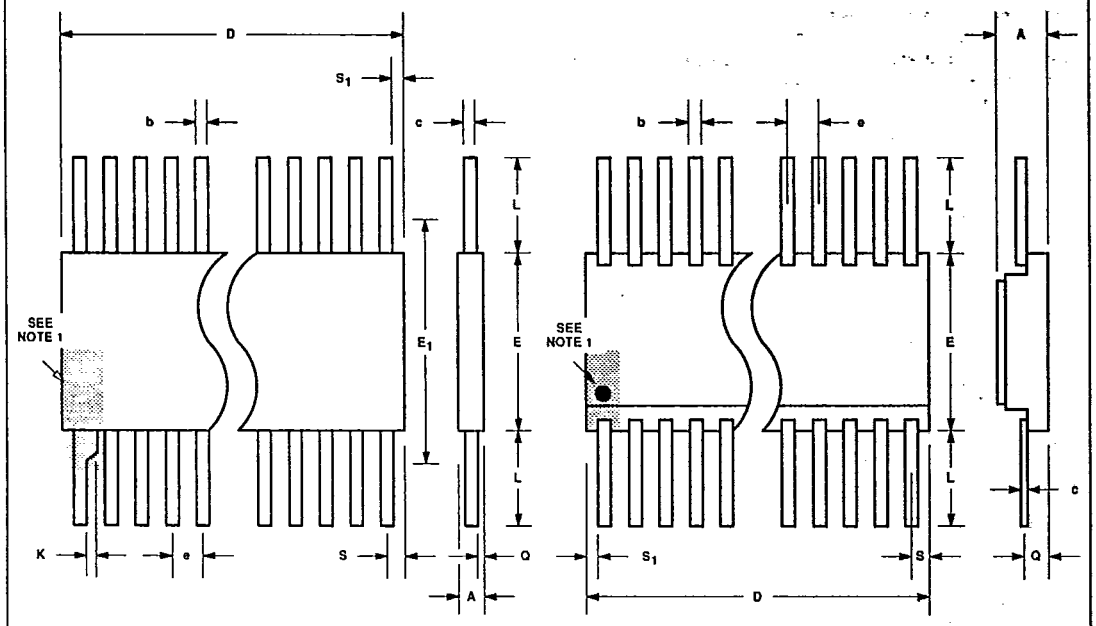
CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1

Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counter-clockwise (as viewed from the top of the device.
2. This dimension allows for off-center lid, meniscus and glass overrun.
3. The reference pin spacing is 0.050 between center-lines. Each pin centerline is located within ±0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	–	1.330	2
E	0.620	0.660	
e	0.050BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	–	0.045	5
S1	0.005	–	5

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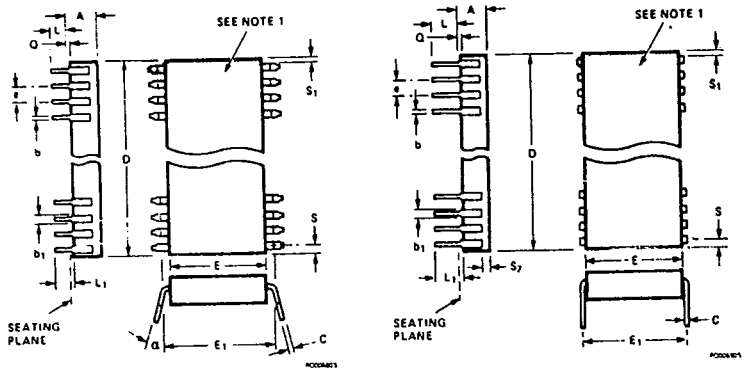
CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1

Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

Packaging Information

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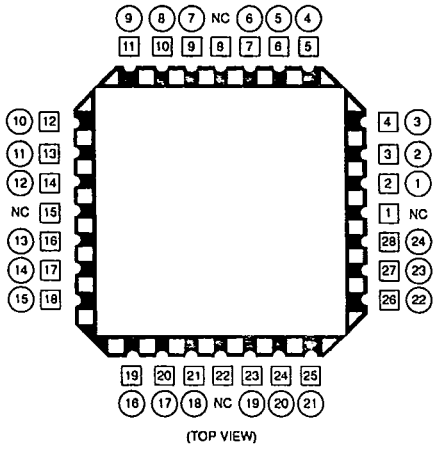
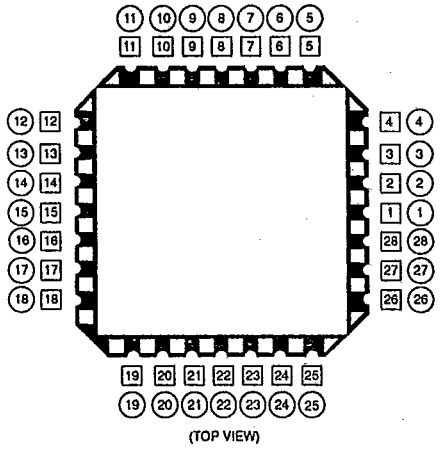
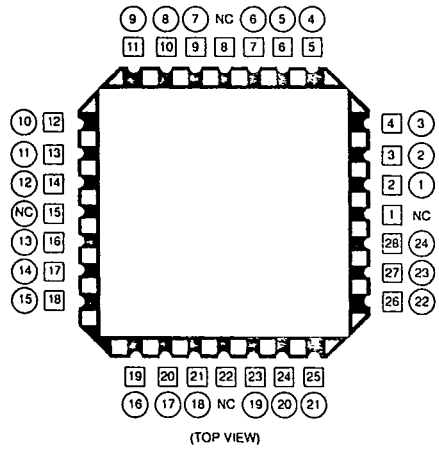
LEADLESS CHIP CARRIER (LLCC) PINOUTS



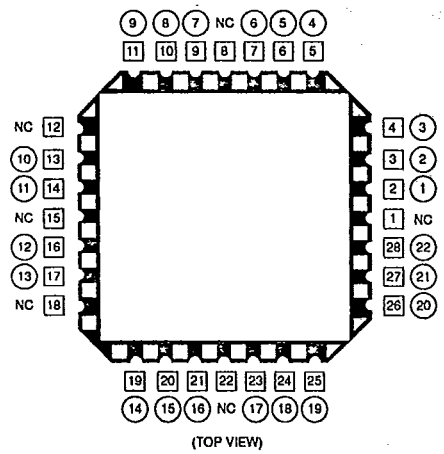
24-Lead Logic Pinout for 28 Terminal Chip Carrier



28-Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24-Lead Memory Pinout for 28 Terminal Chip Carrier



22-Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect

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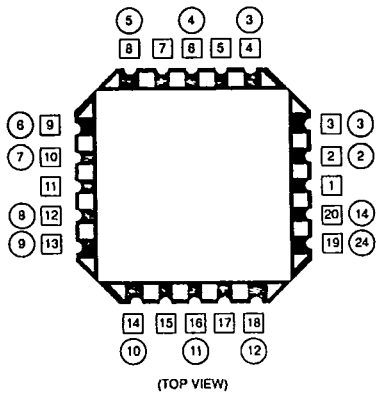
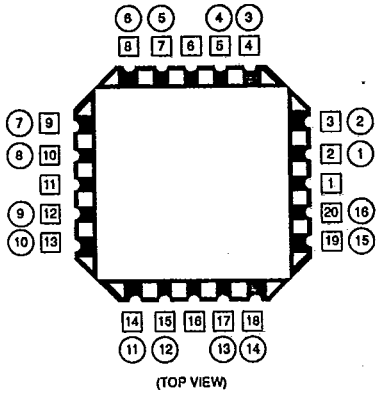
LEADLESS CHIP CARRIER (LLCC) PINOUTS



14-Pin Logic Pinout for 20 Terminal Chip Carrier



16-Pin Logic Pinout for 20 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number