

FEATURES

- **Guaranteed Low Offset Voltage**

LT1001AM	15 μ V max
LT1001C	60 μ V max
- **Guaranteed Low Drift**

LT1001AM	0.6 μ V/ $^{\circ}$ C max
LT1001C	1.0 μ V/ $^{\circ}$ C max
- **Guaranteed Low Bias Current**

LT1001AM	2nA max
LT1001C	4nA max
- **Guaranteed CMRR**

LT1001AM	114dB min
LT1001C	110dB min
- **Guaranteed PSRR**

LT1001AM	110dB min
LT1001C	106dB min
- **Low Power Dissipation**

LT1001AM	75mW max
LT1001C	80mW max
- **Low Noise 0.3 μ V_{P-P}**

APPLICATIONS

- Thermocouple amplifiers
- Strain gauge amplifiers
- Low level signal processing
- High accuracy data acquisition

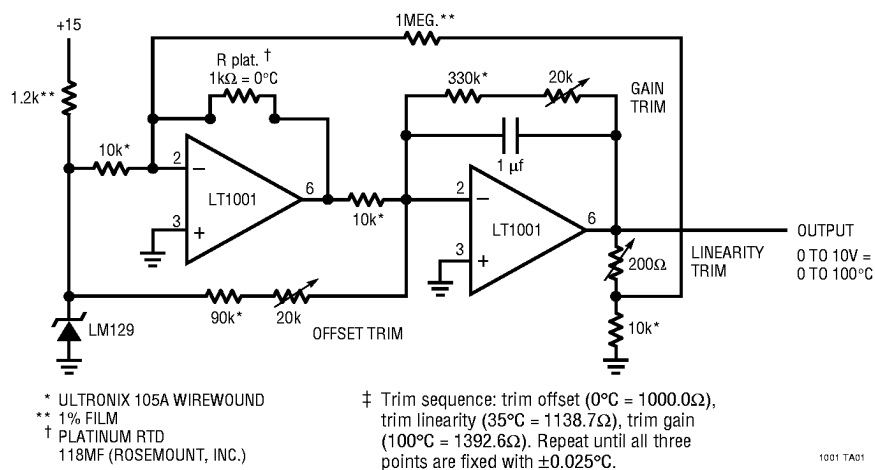
DESCRIPTION

The LT[®]1001 significantly advances the state-of-the-art of precision operational amplifiers. In the design, processing, and testing of the device, particular attention has been paid to the optimization of the entire distribution of several key parameters. Consequently, the specifications of the lowest cost, commercial temperature device, the LT1001C, have been dramatically improved when compared to equivalent grades of competing precision amplifiers.

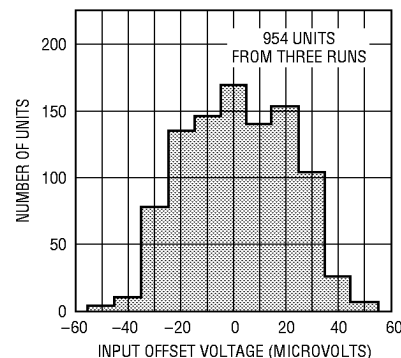
Essentially, the input offset voltage of all units is less than 50 μ V (see distribution plot below). This allows the LT1001AM/883 to be specified at 15 μ V. Input bias and offset currents, common-mode and power supply rejection of the LT1001C offer guaranteed performance which were previously attainable only with expensive, selected grades of other devices. Power dissipation is nearly halved compared to the most popular precision op amps, without adversely affecting noise or speed performance. A beneficial by-product of lower dissipation is decreased warm-up drift. Output drive capability of the LT1001 is also enhanced with voltage gain guaranteed at 10 mA of load current. For similar performance in a dual precision op amp, with guaranteed matching specifications, see the LT1002. Shown below is a platinum resistance thermometer application.

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**Linearized Platinum Resistance Thermometer
with $\pm 0.025^{\circ}$ C Accuracy Over 0 to 100° C**



**Typical Distribution
of Offset Voltage
 $V_S = \pm 15V$, $T_A = 25^{\circ}$ C**



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	$\pm 22\text{V}$
Differential Input Voltage	$\pm 30\text{V}$
Input Voltage	$\pm 22\text{V}$
Output Short Circuit Duration	Indefinite
Operating Temperature Range	
LT1001AM/LT1001M	-55°C to 150°C
LT1001AC/LT1001C	0°C to 125°C
Storage: All Devices	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW OFFSET ADJUST V- (CASE) H PACKAGE METAL CAN	ORDER PART NUMBER		
	LT1001AMH/883 LT1001MH LT1001ACH LT1001CH		
TOP VIEW VOS TRIM 1 8 VOS TRIM -IN 2 7 V+ +IN 3 6 OUT V- 4 5 NC J8 PACKAGE N8 PACKAGE 8 PIN HERMETIC DIP 8 PIN PLASTIC DIP S8 PACKAGE 8 PIN PLASTIC SO	LT1001AMJ8/883 LT1001MJ8 LT1001ACJ8 LT1001CJ8 LT1001ACN8 LT1001CN8 LT1001CS8		
	S8 PART MARKING		
	1001		

ELECTRICAL CHARACTERISTICS $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	LT1001AM/883 LT1001AC			LT1001M/LT1001C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	Note 1 LT1001AM/883 LT1001AC		7	15		18	60	μV
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long Term Input Offset Voltage Stability	Notes 2 and 3		0.2	1.0		0.3	1.5	$\mu\text{V}/\text{month}$
I_{OS}	Input Offset Current			0.3	2.0		0.4	3.8	nA
I_b	Input Bias Current			± 0.5	± 2.0		± 0.7	± 4.0	nA
e_n	Input Noise Voltage	0.1Hz to 10Hz (Note 2)		0.3	0.6		0.3	0.6	μV_{p-p}
e_n	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 5) $f_0 = 1000\text{Hz}$ (Note 2)		10.3 9.6	18.0 11.0		10.5 9.8	18.0 11.0	$\text{nV}/\sqrt{\text{Hz}}$
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2\text{k}\Omega$, $V_O = \pm 12\text{V}$ $R_L \geq 1\text{k}\Omega$, $V_O = \pm 10\text{V}$	450 300	800 500		400 250	800 500		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13\text{V}$	114	126		110	126		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3\text{V}$ to $\pm 18\text{V}$	110	123		106	123		dB
R_{in}	Input Resistance Differential Mode		30	100		15	80		$\text{M}\Omega$
	Input Voltage Range		± 13	± 14		± 13	± 14		V
V_{OUT}	Maximum Output Voltage Swing	$R_L \geq 2\text{k}\Omega$ $R_L \geq 1\text{k}\Omega$	± 13 ± 12	± 14 ± 13.5		± 13 ± 12	± 14 ± 13.5		V V
S_R	Slew Rate	$R_L \geq 2\text{k}\Omega$ (Note 4)	0.1	0.25		0.1	0.25		V/ μs
GBW	Gain-Bandwidth Product	(Note 4)	0.4	0.8		0.4	0.8		MHz
P_d	Power Dissipation	No load No load, $V_S = \pm 3\text{V}$	46 4	75 6		48 4	80 8		mW

See Notes on page 3.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V, -55^\circ C \leq T_A \leq 125^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AM/883			LT1001M			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	30	60		45	160		μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	0.2	0.6		0.3	1.0		$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.8	4.0		1.2	7.6		nA
I_B	Input Bias Current		●	± 1.0	± 4.0		± 1.5	± 8.0		nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$	●	300	700		200	700		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	122		106	120		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3$ to $\pm 18V$	●	104	117		100	117		dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.5		± 12.0	± 13.5		V
P_d	Power Dissipation	No load	●	55	90		60	100		mW

$V_S = \pm 15V, 0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		LT1001AC			LT1001C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage		●	20	60		30	110		μV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Offset Voltage Drift		●	0.2	0.6		0.3	1.0		$\mu V/^\circ C$
I_{OS}	Input Offset Current		●	0.5	3.5		0.6	5.3		nA
I_B	Input Bias Current		●	± 0.7	± 3.5		± 1.0	± 5.5		nA
A_{VOL}	Large Signal Voltage Gain	$R_L \geq 2k\Omega, V_O = \pm 10V$	●	350	750		250	750		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 13V$	●	110	124		106	123		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 3V$ to $\pm 18V$	●	106	120		103	120		dB
	Input Voltage Range		●	± 13	± 14		± 13	± 14		V
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$	●	± 12.5	± 13.8		± 12.5	± 13.8		V
P_d	Power Dissipation	No load	●	50	85		55	90		mW

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Offset voltage for the LT1001AM/883 and LT1001AC are measured after power is applied and the device is fully warmed up. All other grades are measured with high speed test equipment, approximately 1 second after power is applied. The LT1001AM/883 receives 168 hr. burn-in at $125^\circ C$. or equivalent.

Note 2: This parameter is tested on a sample basis only.

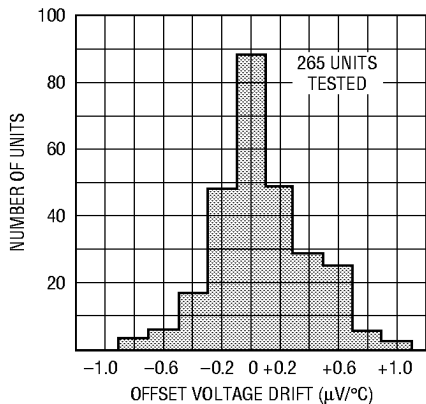
Note 3: Long Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} versus Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically $2.5\mu V$.

Note 4: Parameter is guaranteed by design.

Note 5: 10Hz noise voltage density is sample tested on every lot. Devices 100% tested at 10Hz are available on request.

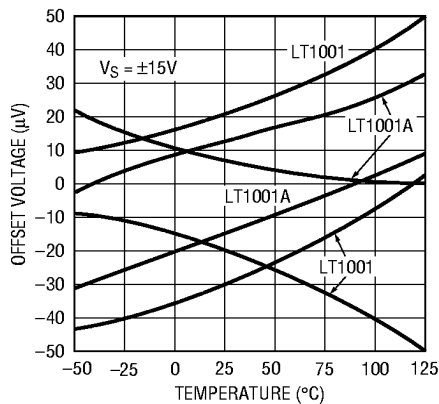
TYPICAL PERFORMANCE CHARACTERISTICS

Typical Distribution of Offset Voltage Drift with Temperature



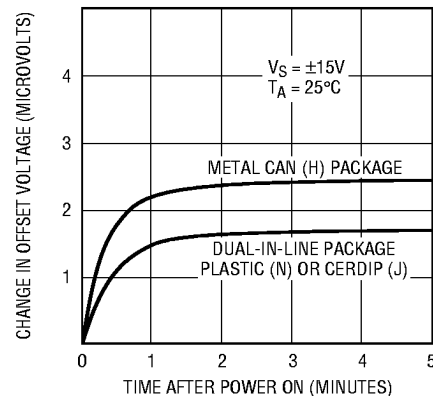
1001 G01

Offset Voltage Drift with Temperature of Representative Units



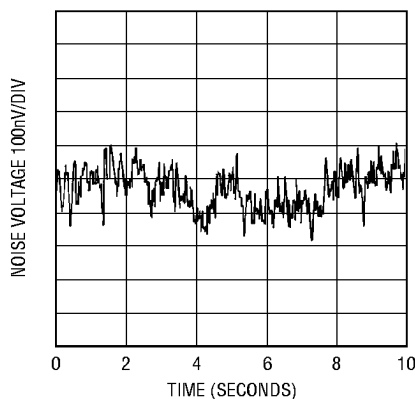
1001 G02

Warm-Up Drift



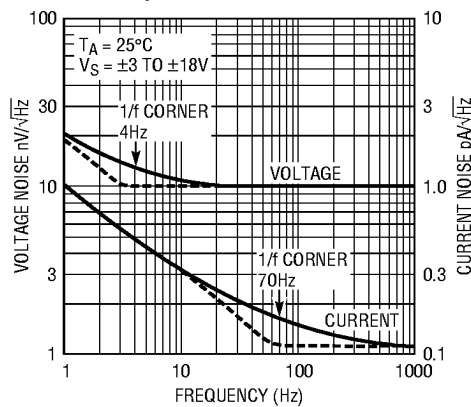
1001 G03

0.1Hz to 10Hz Noise



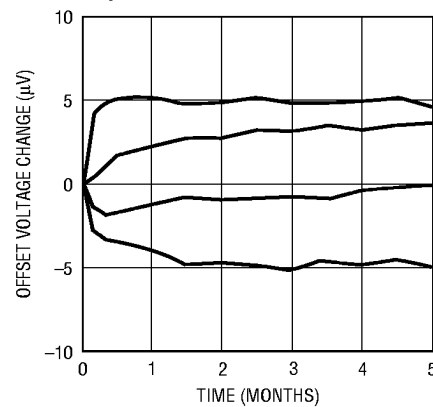
1001 G04

Noise Spectrum



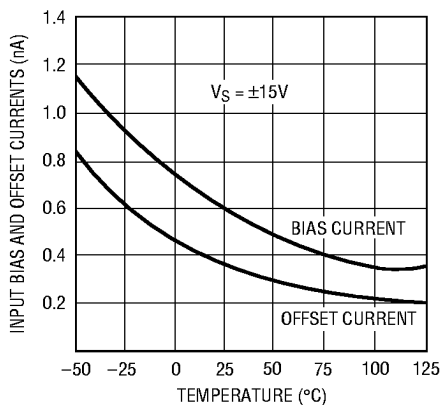
1001 G05

Long Term Stability of Four Representative Units



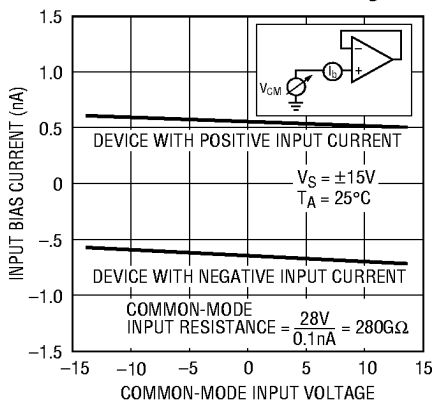
1001 G06

Input Bias and Offset Current vs Temperature



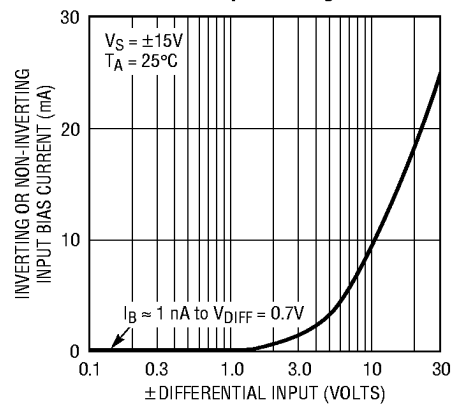
1001 G07

Input Bias Current Over the Common Mode Range



1001 G08

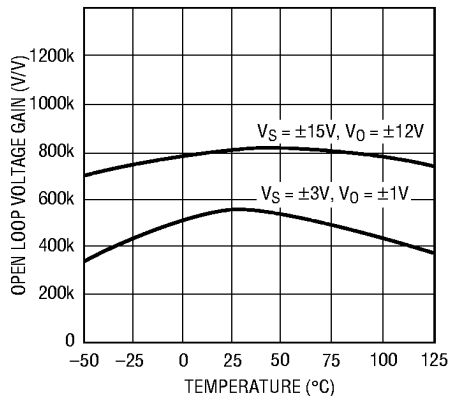
Input Bias Current vs Differential Input Voltage



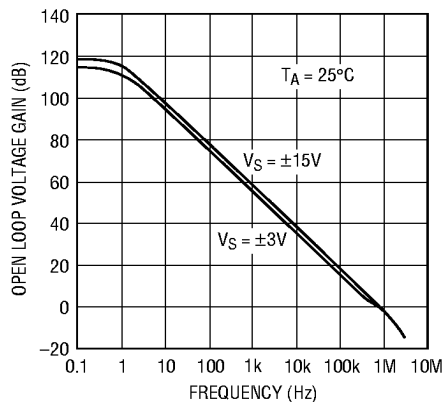
1001 G09

TYPICAL PERFORMANCE CHARACTERISTICS

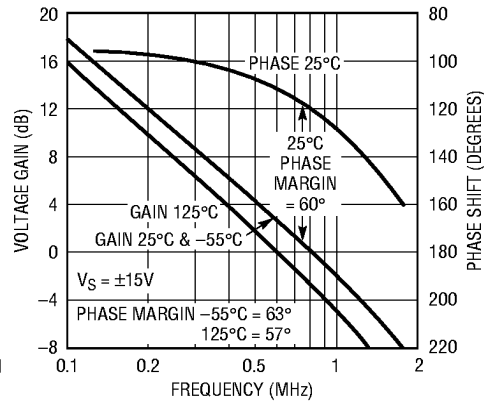
Open Loop Voltage Gain vs Temperature



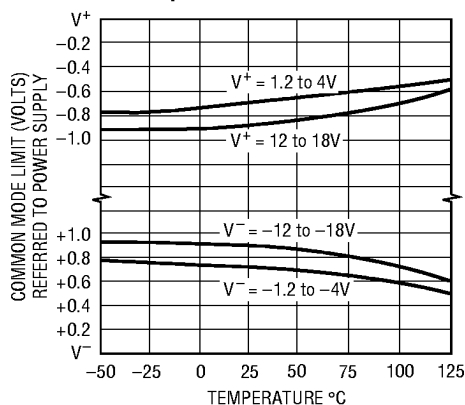
Open Loop Voltage Gain Frequency Response



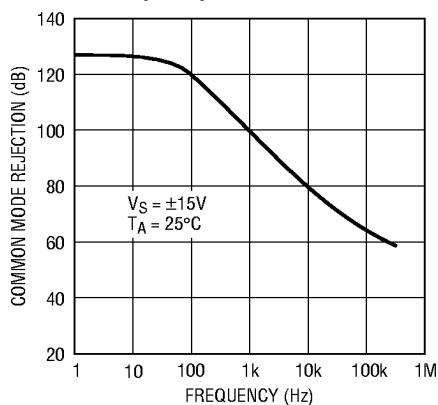
Gain, Phase Shift vs Frequency



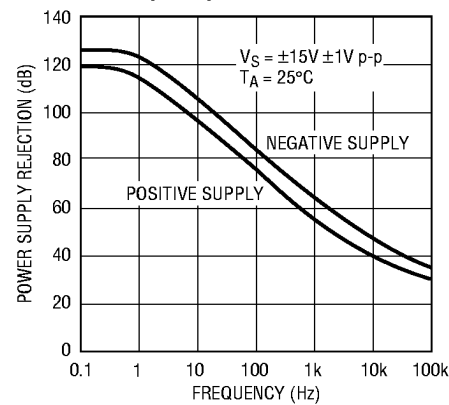
Common Mode Limit vs Temperature



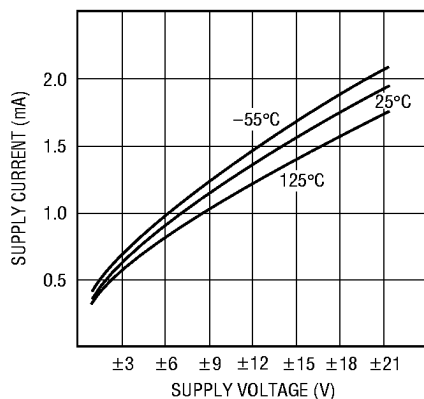
Common Mode Rejection Ratio vs Frequency



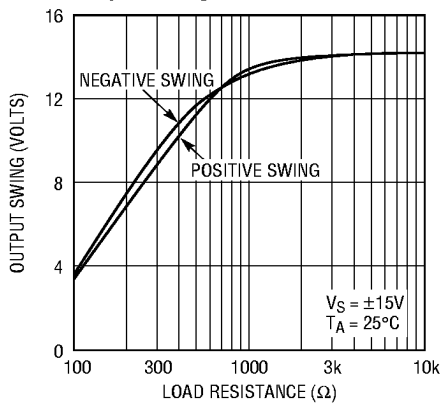
Power Supply Rejection Ratio vs Frequency



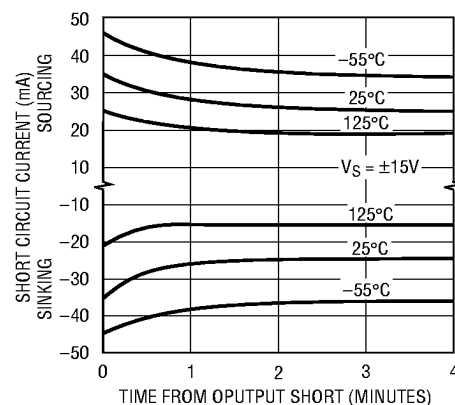
Supply Current vs Supply Voltage



Output Swing vs Load Resistance

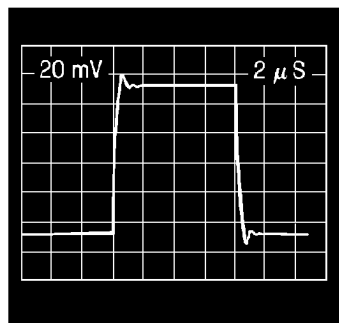


Output Short-Circuit Current vs Time



TYPICAL PERFORMANCE CHARACTERISTICS

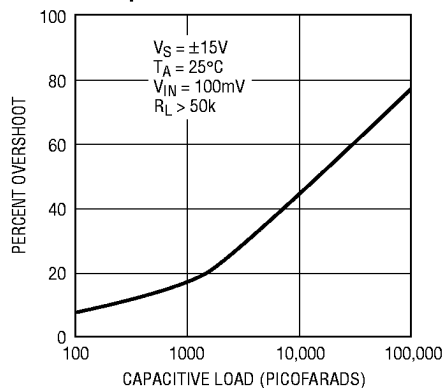
Small Signal Transient Response



$A_V = +1$, $C_L = 50\text{pF}$

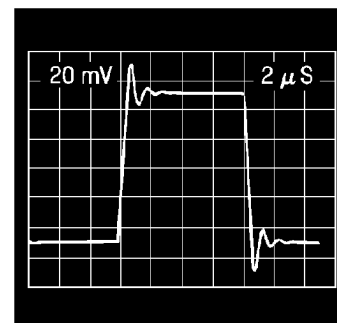
1001 G19

Voltage Follower Overshoot vs Capacitive Load



1001 G20

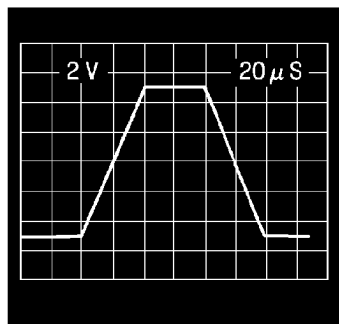
Small Signal Transient Response



$A_V = +1$, $C_L = 1000\text{pF}$

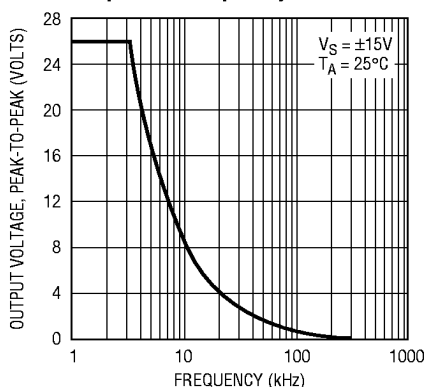
1001 G21

Large Signal Transient Response



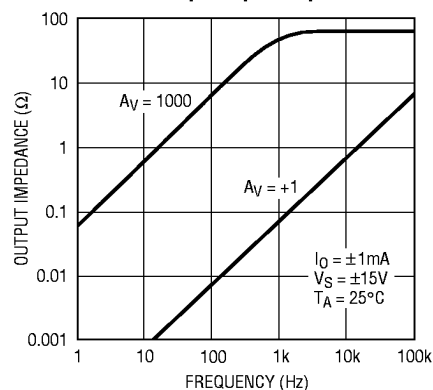
1001 G22

Maximum Undistorted Output vs. Frequency



1001 G23

Closed Loop Output Impedance



1001 G24

APPLICATIONS INFORMATION

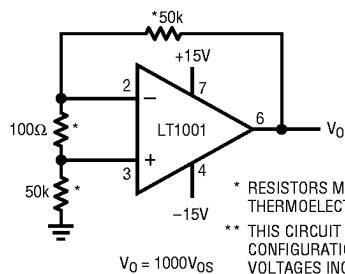
Application Notes and Test Circuits

The LT1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT1001 can also be used in 741, LF156 or OP-15 applications provided that the nulling circuitry is removed.

The LT1001 is specified over a wide range of power supply voltages from $\pm 3\text{V}$ to $\pm 18\text{V}$. Operation with lower supplies is possible down to $\pm 1.2\text{V}$ (two Ni-Cad batteries). However, with $\pm 1.2\text{V}$ supplies, the device is stable only in closed loop gains of +2 or higher (or inverting gain of one or higher).

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Test Circuit for Offset Voltage and its Drift with Temperature



* RESISTORS MUST HAVE LOW THERMOELECTRIC POTENTIAL.

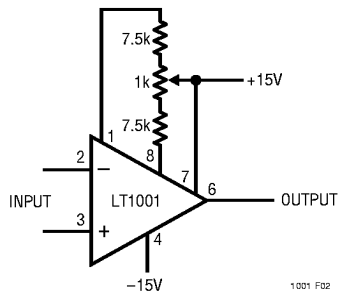
** THIS CIRCUIT IS ALSO USED AS THE BURN-IN CONFIGURATION FOR THE LT1001, WITH SUPPLY VOLTAGES INCREASED TO $\pm 20\text{V}$.

1001 F01

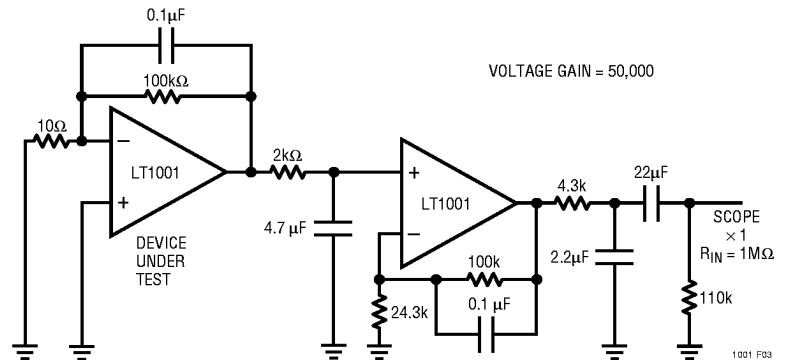
Offset Voltage Adjustment

The input offset voltage of the LT1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{os} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of $(V_{os}/300)\mu V/^{\circ}C$, e.g., if V_{os} is adjusted to $300\mu V$, the change in drift will be $1\mu V/^{\circ}C$. The adjustment range with a 10k or 20k pot is approximately $\pm 2.5mV$. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of $\pm 100\mu V$.

Improved Sensitivity Adjustment



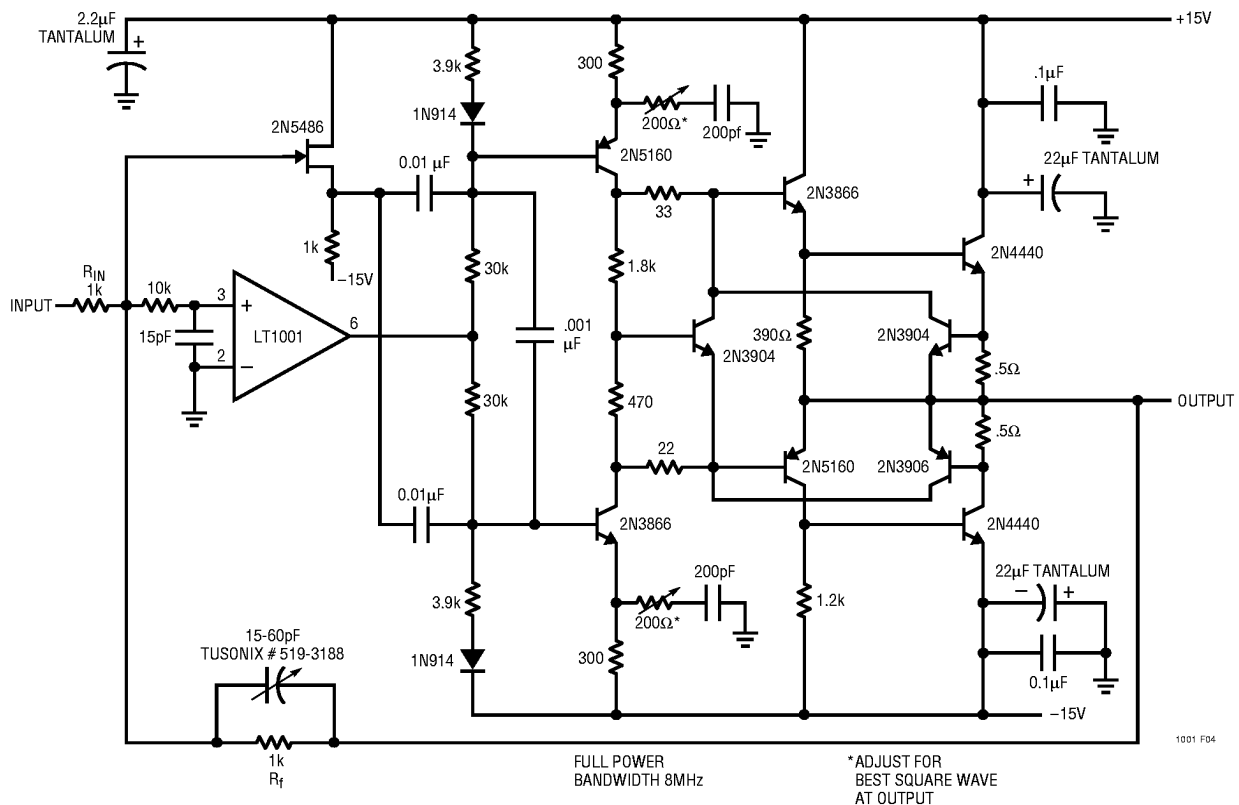
0.1Hz to 10Hz Noise Test Circuit



(Peak-to-Peak noise measured in 10 sec interval)

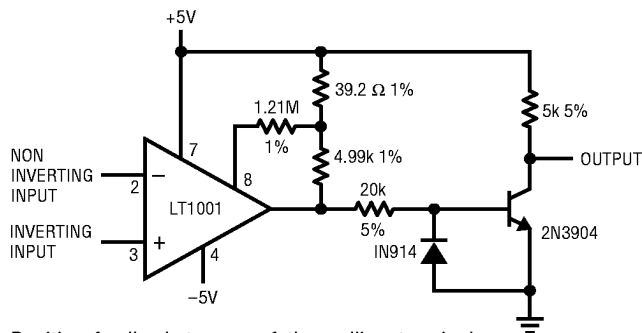
The device under test should be warmed up for three minutes and shielded from air currents.

DC Stabilized 1000v/μsec Op Amp



TYPICAL APPLICATIONS

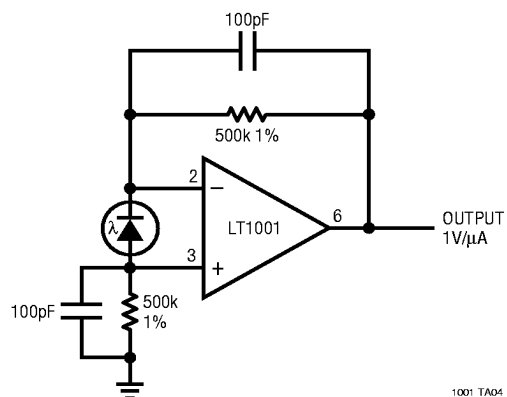
Microvolt Comparator with TTL Output



Positive feedback to one of the nulling terminals creates 5 μ to 20 μ V of hysteresis. Input offset voltage is typically changed by less than 5 μ V due to the feedback.

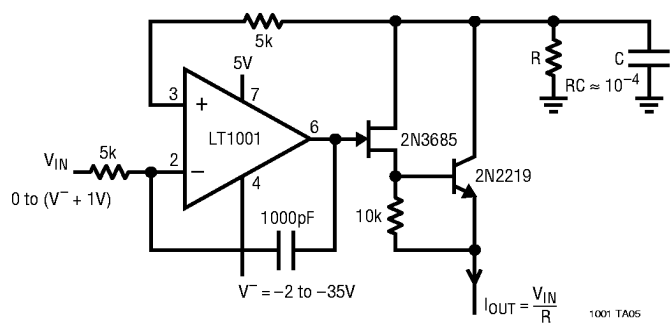
1001 TA03

Photodiode Amplifier



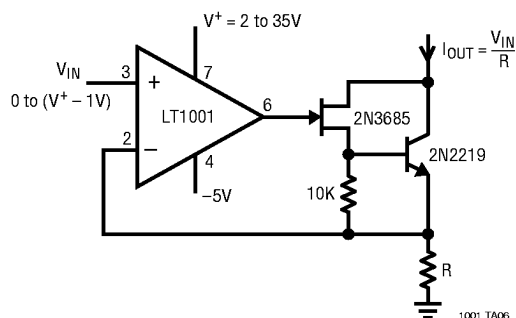
1001 TA04

Precision Current Source



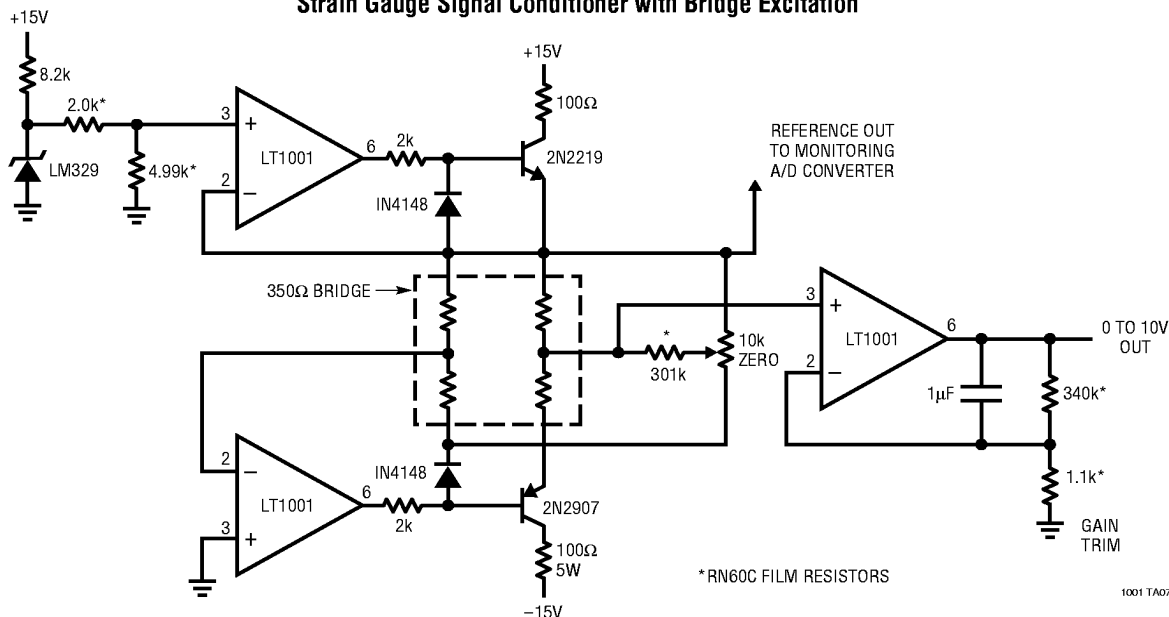
1001 TA05

Precision Current Sink



1001 TA06

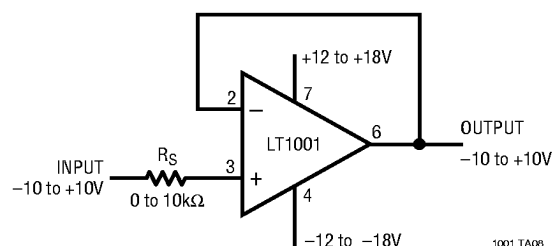
Strain Gauge Signal Conditioner with Bridge Excitation



* RN60C FILM RESISTORS

1001 TA07

Large Signal Voltage Follower With 0.001% Worst-Case Accuracy

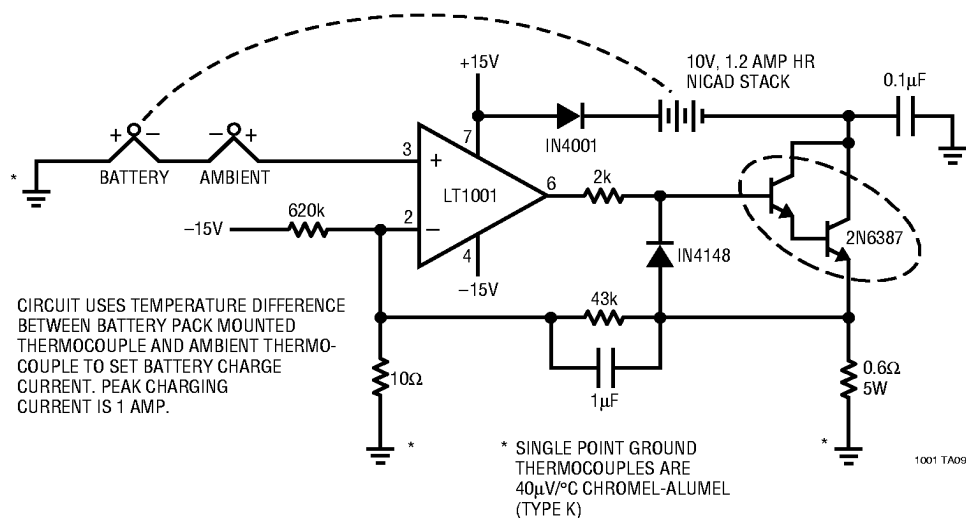


The voltage follower is an ideal example illustrating the overall excellence of the LT1001. The contributing error terms are due to offset voltage, input bias current, voltage gain, common-mode and power-supply

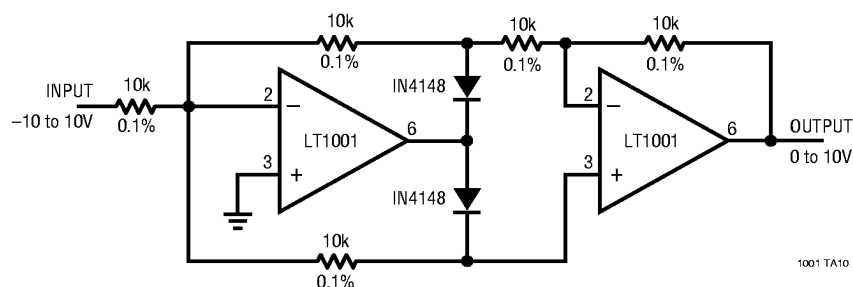
rejections. Worst-case summation of guaranteed specifications is tabulated below.

Error	OUTPUT ACCURACY			
	LT1001AM /883 25°C Max.	LT1001C 25°C Max.	LT1001AM /883 -55 to 125°C Max.	LT1001C 0 to 70°C Max.
Offset Voltage	15μV	60μV	60μV	110μV
Bias Current	20μV	40μV	40μV	55μV
Common-Mode Rejection	20μV	30μV	30μV	50μV
Power Supply Rejection	18μV	30μV	36μV	42μV
Voltage Gain	22μV	25μV	33μV	40μV
Worst-case Sum	95μV	185μV	199μV	297μV
Percent of Full Scale (=20V)	0.0005%	0.0009%	0.0010%	0.0015%

Thermally Controlled NiCad Charger



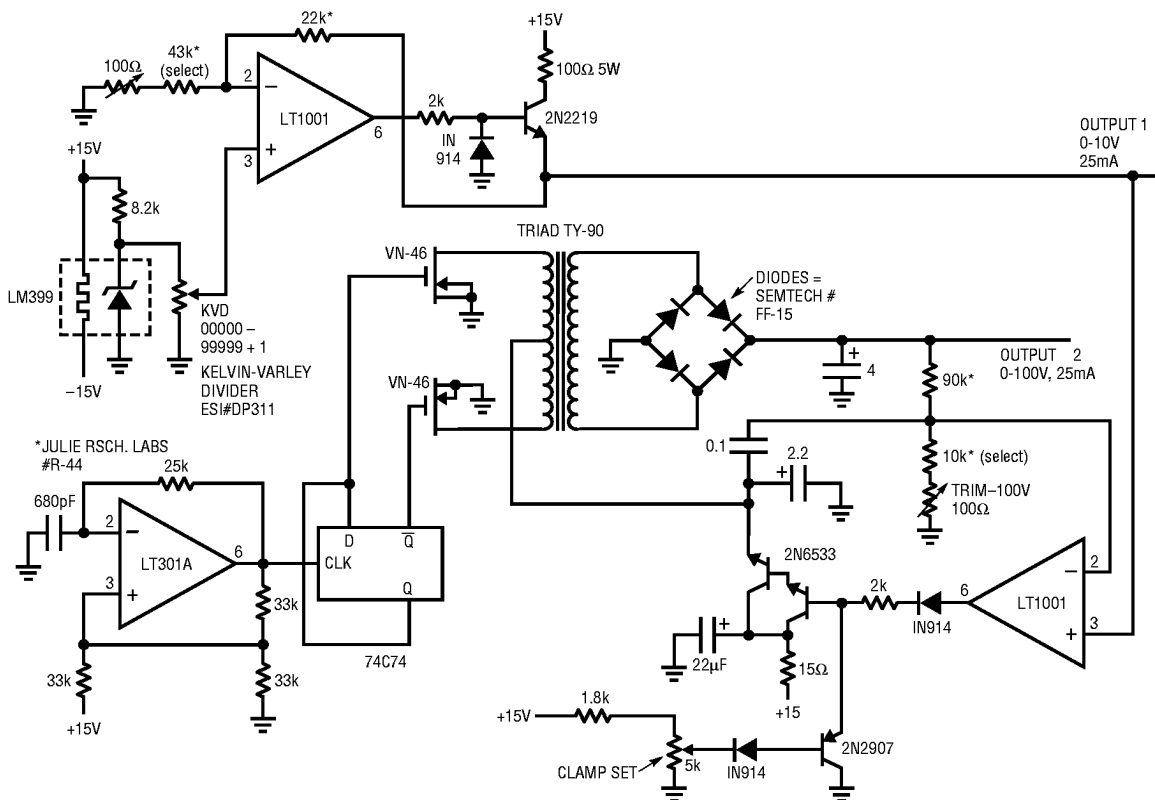
Precision Absolute Value Circuit



Precision Power Supply with Two Outputs

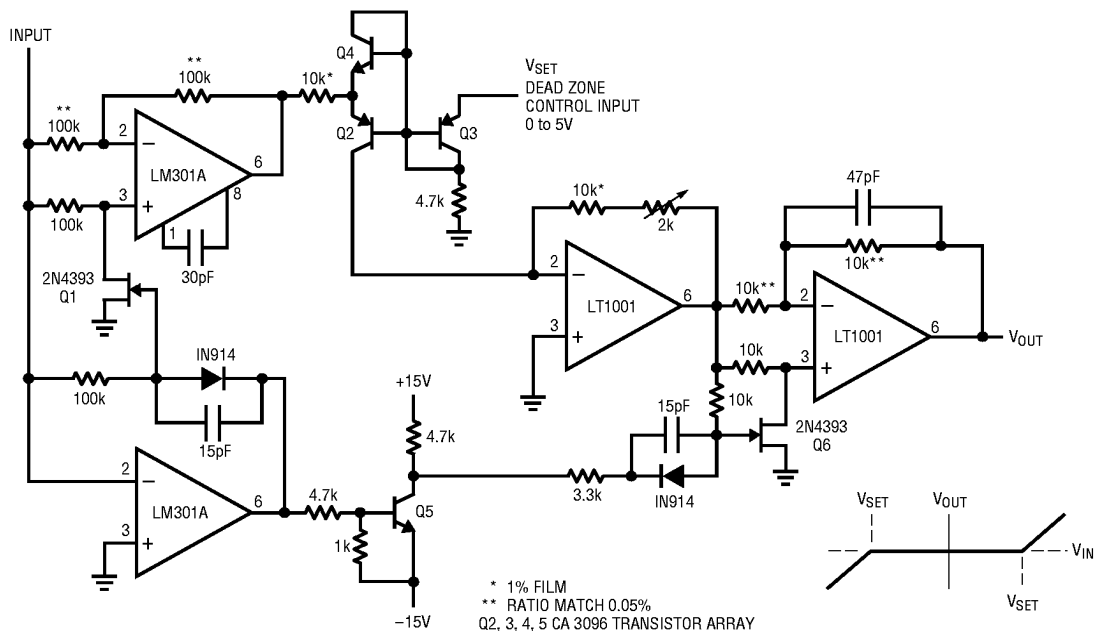
(1) 0V to 10V in 100 μ V STEPS

(2) 0V to 100V in 1mV STEPS



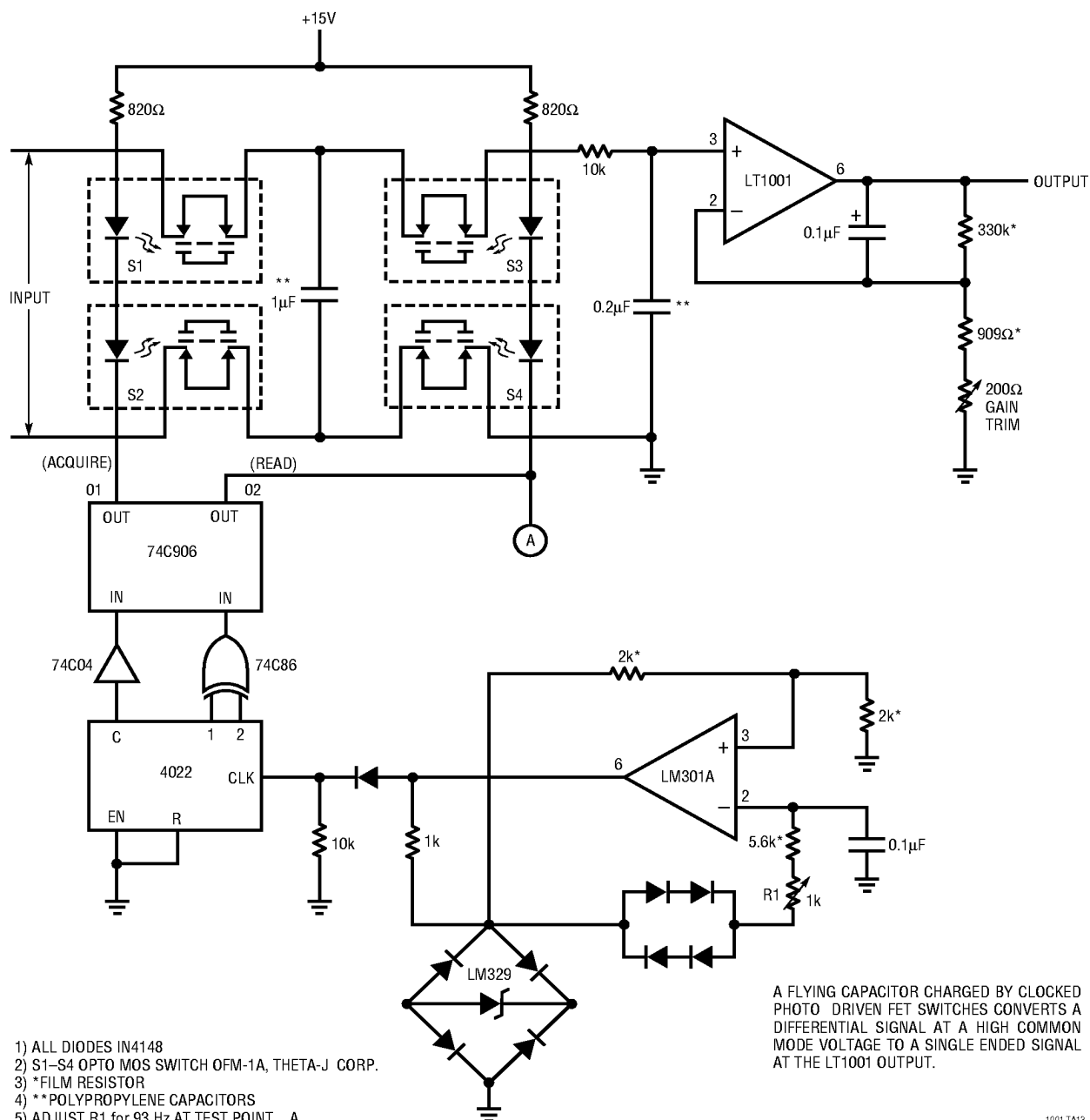
Dead Zone Generator

BIPOLAR SYMMETRY IS EXCELLENT BECAUSE ONE DEVICE, Q2, SETS BOTH LIMITS



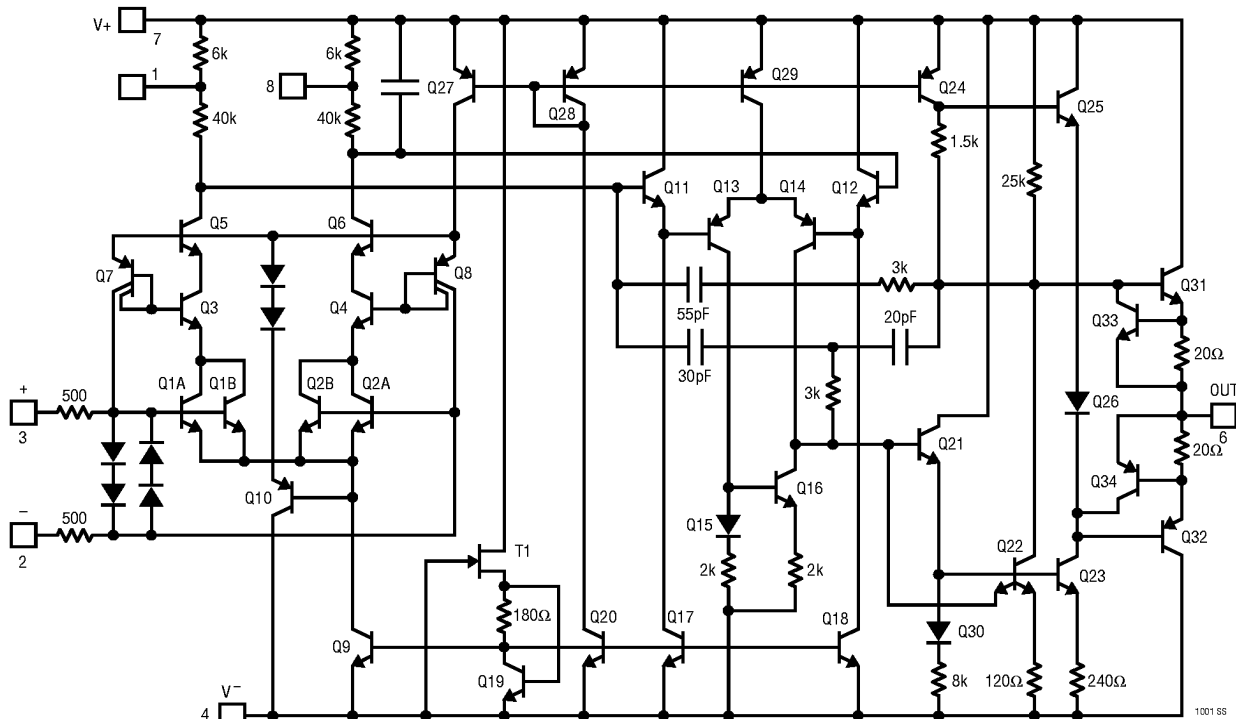
* 1% FILM
** RATIO MATCH 0.05%
Q2, 3, 4, 5 CA 3096 TRANSISTOR ARRAY

**Instrumentation Amplifier with $\pm 300V$
Common Mode Range and CMRR > 150dB**



1001 TA13

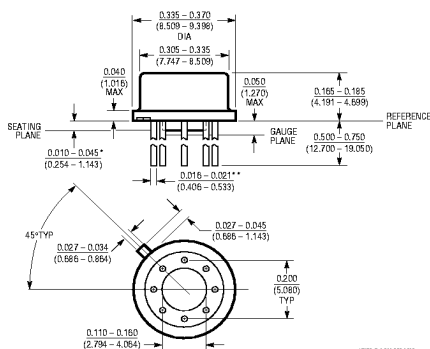
SCHEMATIC DIAGRAM



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

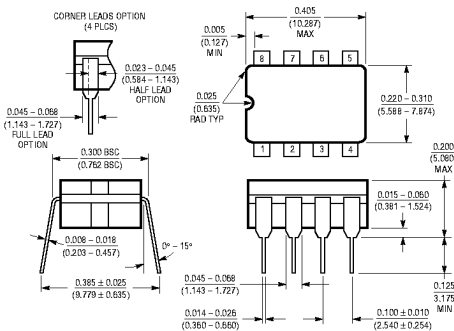
H Package
8-Lead TO-5 Metal Can (0.200 PCD)
 (LTC DWG # 05-08-1320)



**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

T_{jmax}	θ_{ja}	θ_{jc}
150°C	150°C/W	45°C/W

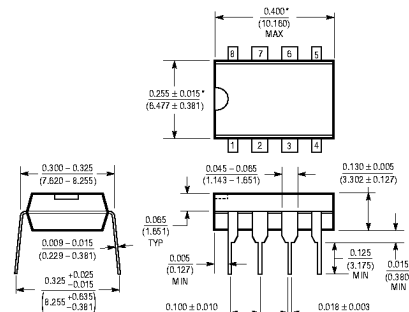
J8 Package
8-Lead Cerdip (Narrow 0.300, Hermetic)
 (LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

T_{jmax}	θ_{ja}
150°C	100°C/W

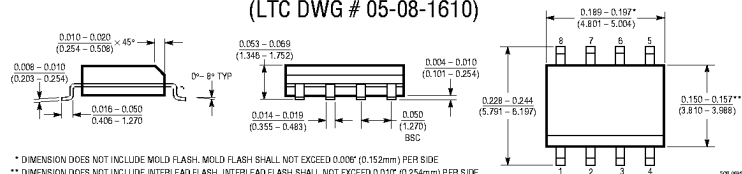
N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

T_{jmax}	θ_{ja}
150°C	130°C/W

S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

T_{jmax}	θ_{ja}
150°C	150°C/W