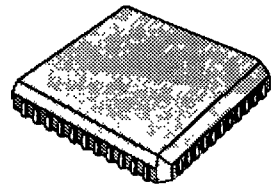
SGS-THOMSON MICROELECTRONICS

IMSA113

PROGRAMMABLE LENGTH DIGITAL DELAY LINE

PRELIMINARY DATA

- VARIABLE LENGTH 5-1317 CYCLES (LATENCIES OF 6-1318)
- FULLY CASCADABLE IN WIDTH AND LENGTH
- AUTO-ZEROING OF DATA ON LENGTH CHANGE
- UP TO 20MHz DATA RATE
- FULLY STATIC HIGH SPEED CMOS IMPLEMENTATION
- TTL COMPATIBLE
- SINGLE +5V ± 10% SUPPLY
- POWER DISSIPATION < 250 MWATTS
- 44 PIN PLCC PACKAGE



PLCC44
(Plastic Chip Carrier)

APPLICATIONS

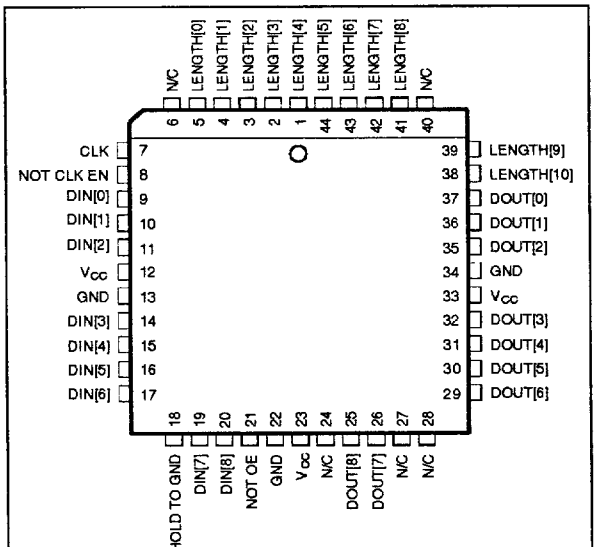
- IMAGE PROCESSING
- AUDIO PROCESSING
- ENHANCMENT OF A100/A110/A121 APPLICATIONS
- GHOST/ECHO CANCELLATION
- RADAR/SONAR BEAMFORMING
- DIGITAL TV LINE BUFFER
- LATENCY EQUALISER

ORDERING INFORMATION

Designation	Package	Clock speed
IMSA113-J20S	PLCC44	20MHz

A113-01.TBL

PIN CONNECTIONS



Notes : 1. All V_{CC} pins **must** be connected to the 5 Volt power supply.
2. All **GND** pins **must** be connected to ground.
3. **N/C** indicates pin not connected

A113-01.EPS

DESCRIPTION

The IMSA113 is a digital Delay line of programmable length. The device can be set up to delay input data from 5 clock cycles up to 1317 clock cycles. The delay line can be viewed as a data queue of prespecified length. On the rising edge of each clock pulse the data word on the **Din[8-0]** bus is placed onto the back of the queue and the data word at the front of the queue is placed onto the **Dout[8-0]** bus. Data is thus delayed by a number of clock cycles equal to the value present on the pins **Length[10-0]**.

1. PIN DESCRIPTIONS

System services

Pin	In/out	Function
V_{CC}, GND		Power supply and return
CLK	In	Input clock

Synchronous input/output

Pin	In/out	Function
Din[8-0]	In	Data input port
Dout[8-0]	Out	Data output port
notClkEn	In	Enable internal clock
Length[10-0]	In	Delay line length input port

Asynchronous input

Pin	In/out	Function
notOE	In	Output port tristate control

1.1 System services

Power

Power is supplied to the device via the V_{CC} and **GND** pins. All supply pins must be connected. The supply must be decoupled close to the chip by at least one 100nF low inductance (e.g. ceramic) capacitor between V_{CC} and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling. Input voltages must not exceed specification with respect to V_{CC} and **GND**.

CLK

The clock input signal **CLK** controls the timing of input and the output on the three dedicated interfaces, and controls the progress of data through the line delay. Since the IMS A113 is fully static, the clock can be stopped in either phase without corrupting data.

Resetting the device

The IMS A113 does not have a reset pin. A reset is initiated automatically when power is first applied to the device. This reset will be completed once four cycles of **CLK** have occurred after V_{CC} is valid.

1.2 Synchronous input/output

Din[8-0]

The data input port is sampled on every clock cycle. Data must be valid on the rising edge of **CLK**.

Dout[8-0]

The data output port is driven on the rising edge of **CLK**.

notClkEn

The **notClkEn** pin is sampled on the rising edge of **CLK**. The signal is active low. When it is inactive the device's internal clock is stopped, thus stopping the progress of data through the line delay.

Length[10-0]

The length of the delay line is specified by the binary number present on **Length[10-0]**. **Length[0]** is the least signifigant bit. The length set will give a latency of Length + 1 after the output data has been clocked on the following rising clock edge. For example to achieve a latency of 6 cycles **Length[10-0]** must be set to 5. Since **Din[8-0]** is latched on the rising clock edge when cascading devices for increased length the overall latency is the sum of the individual latencies.
For a fixed delay **Length[10-0]** are simply wired to V_{DD} or **Gnd** as appropriate. In order to accomodate variable delay lengths the **Length[10-0]** bus is sampled on the rising edge of **CLK**. When a delay length change is detected the line delay is reset. The value on the **Din[8-0]** bus at the time of the delay length change will appear at the **Dout[8-0]** bus after a period equal to the new delay length.
When the delay length on **Length[10-0]** is changed the contents of the delay line are zeroed, excepting the three data samples at the front of the queue. At power on the delay length on **Length[10-0]** is treated as a new length.
The exception to this is changing to the minimum delay length of five cycles, when no zeroing takes place.
When an illegal delay length (less than 5 or greater than 1317) is programmed no data is taken from the **Din[8-0]** bus (see Figure 1). So effectively the **Dout[8-0]** bus will continue to be zero. The delay lengths from 1984 to 2015 are used for testing purposes and therefore should not be set.

Example of a length Change

If the delay length is changed for example to an x cycles delay, the status of the delay line immediately after the change is shown in Figure 2.

Thus the order of data pushed from the front of the queue immediately following the length change will be: –

- 3 cycles of original data (including data output as new length latched)
- x - 3 cycles of zeroed data
- Valid data, beginning with that sampled at the time of the length change

Refer to the timing diagram, Figure 3, for an example of changing the length to 6.

1.3 Asynchronous input/output

notOE

This pin is asynchronous to **CLK**. The signal is active low. When it is inactive the **Dout[8-0]** pins are high impedance.

Figure 1

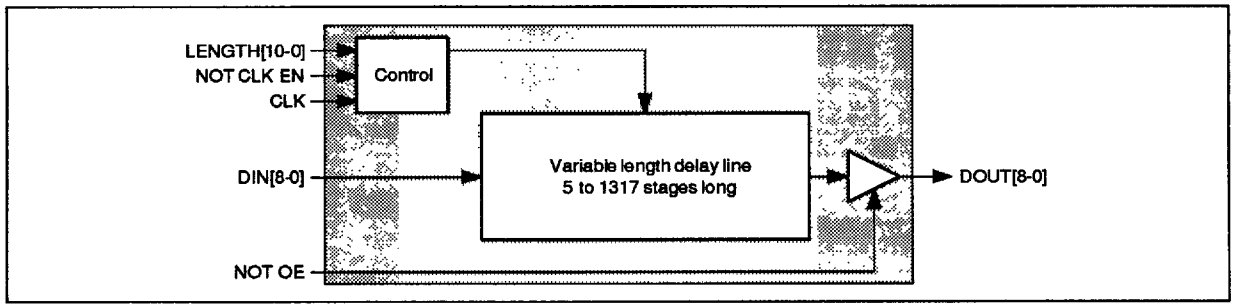


Figure 2

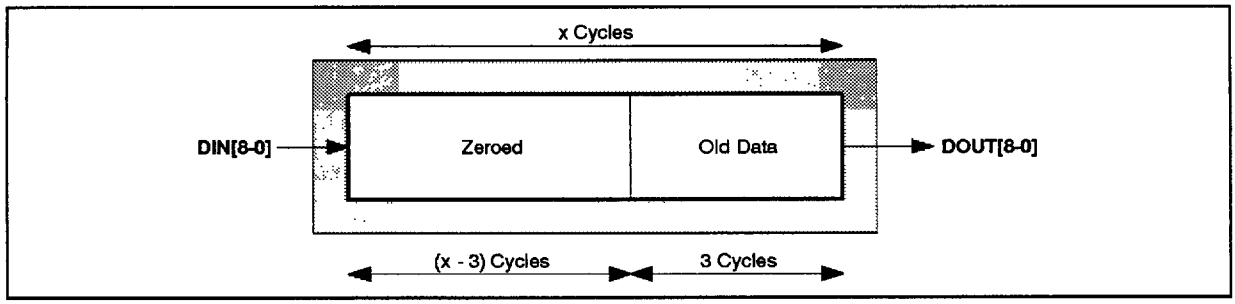
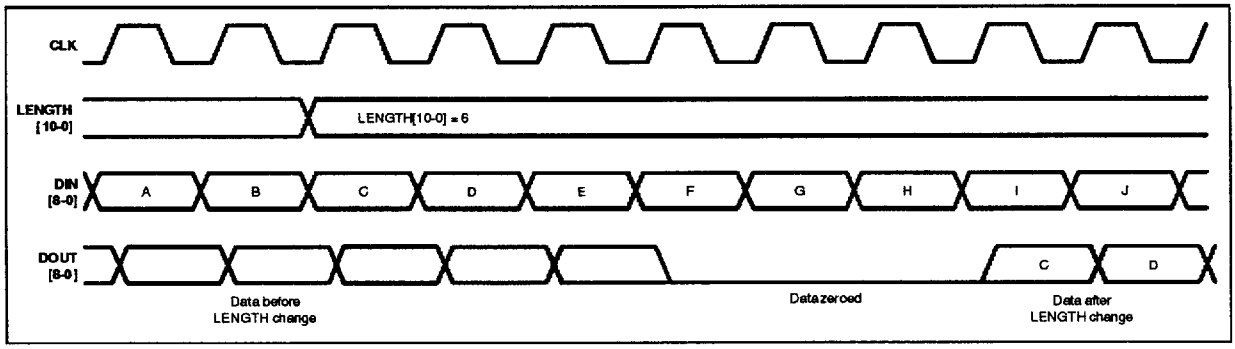


Figure 3



2. ELECTRICAL SPECIFICATION

2.1 DC Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
V_{CC}	DC supply voltage	0		7.0	V	2
V_I, V_O	Voltage on input and output pins	-1.0		V_{CC}+0.5	V	2
T_A	Temperature under bias	-40		85	°C	2
T_S	Storage temperature	-65		150	°C	2
P_{Dmax}	Power dissipation			250	mW	

Notes : 1. All voltages are with respect to GND.
2. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
V_{CC}	DC supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input Logic '1' Voltage	2.0		V_{CC}+0.5	V	2
V_{IL}	Input Logic '0' Voltage	-0.5		0.8	V	2
T_A	Ambient Operating Temperature	0		70	°C	3

Notes: 1. All voltages are with respect to GND. All **GND** pins must be connected to GND.
2. Input signal transients 10ns wide, are permitted in the voltage ranges GND - 0.5V to GND - 1.0V and V_{CC} + 0.5V to V_{CC} + 1.0V.
3. 400 linear ft/min transverse air flow.

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2)
V_{OH}	Output Logic '1' Voltage	2.4		V_{CC}	V	$I_O \leq$ -4.4 mA
V_{OL}	Output Logic '0' Voltage	0		0.4	V	$I_O \leq$ 4.4 mA
I_{IN}	Input leakage current (any input)			±10	µA	3
I_{CC}	Average power supply current			55	mA	4

Notes: 1. All voltages are with respect to GND. All **GND** pins must be connected to GND.
2. Under the conditions specified by the DC operating conditions.
3. $V_{CC} = V_{CC}$ (max), GND $\leq V_{IN} \leq V_{CC}$
4. This applies with no DC loading on the output pins at 20MHz and it will be less at slower clock rates

2.2 Package specifications

THERMAL CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
θ JA	Junction to ambient thermal resistance				°C/W	1,2

Notes: 1. Measured at 400 linear ft/min transverse air flow.
2. This parameter is sampled and not 100% tested.

2.3 A.C. timing characteristics

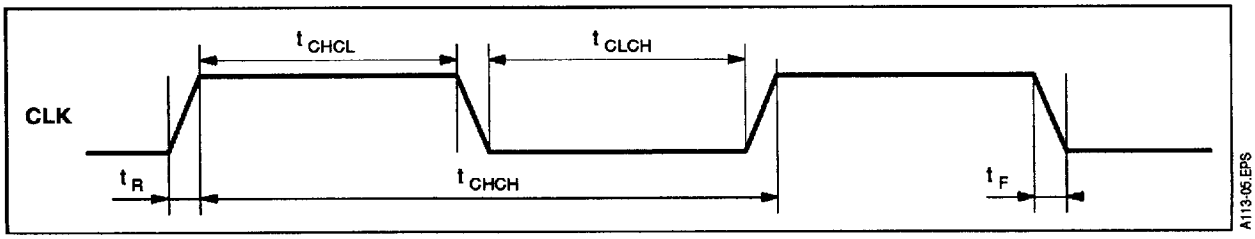
All timings are given for a load of 30pF unless otherwise stated.

CLOCK REQUIREMENTS

Symbol	Parameter	Min	Typ.	Max	Units	Notes
t_{CHCL}	Clock Pulse High Width	20			ns	
t_{CLCH}	Clock Pulse Low Width	20			ns	
t_{CHCH}	Clock Period	50			ns	
t_R	Clock rise time	0		50	ns	1
t_F	Clock fall time	0		50	ns	1

Note: 1. The clock edges should be monotonic between V_{IL} and V_{IH}.

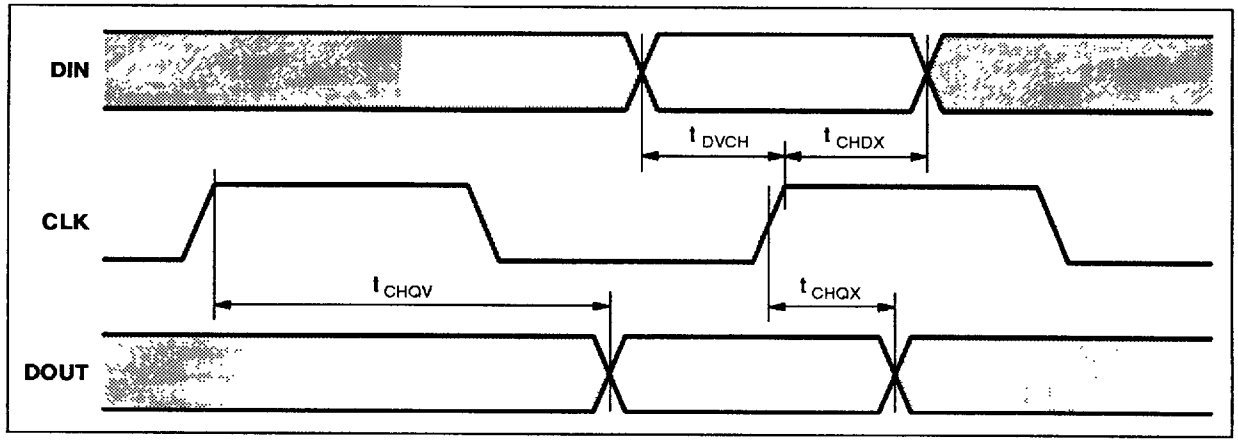
Figure 4



SYNCHRONOUS INPUT AND OUTPUT (Din, Dout)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
t_{CHQV}	CLK high to Dout Valid			38	ns	
t_{CHQX}	Dout hold time after CLK	2			ns	
t_{DVCH}	Din setup time to CLK high	10			ns	
t_{CHDX}	Din hold time to CLK high	0			ns	

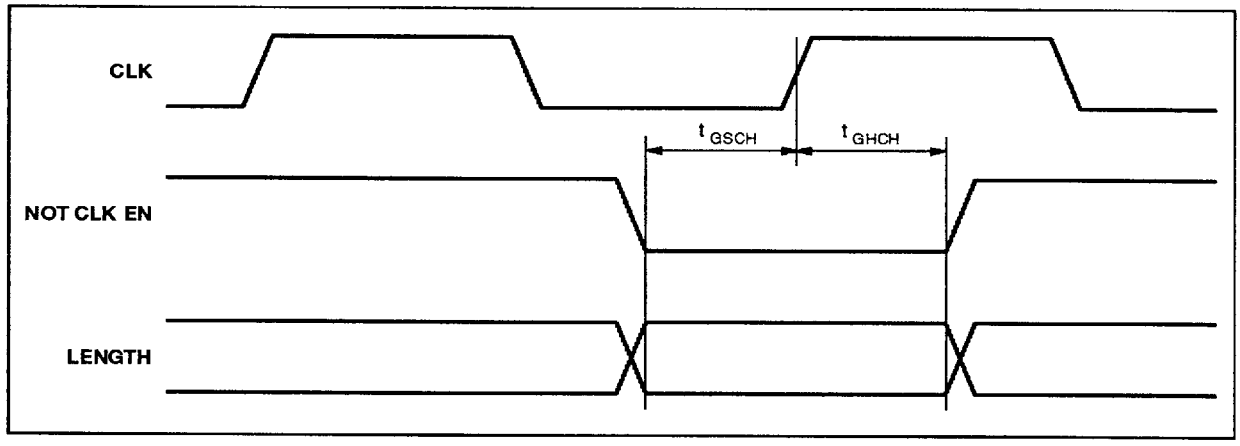
Figure 5



SYNCHRONOUS CONTROL (notClkEn, Length[10-0])

Symbol	Parameter	Min	Typ.	Max	Units	Notes
t_{GHCH}	notClkEn/Length hold to clock high	0			ns	
t_{GSCH}	notClkEn/Length setup to clock high	10			ns	

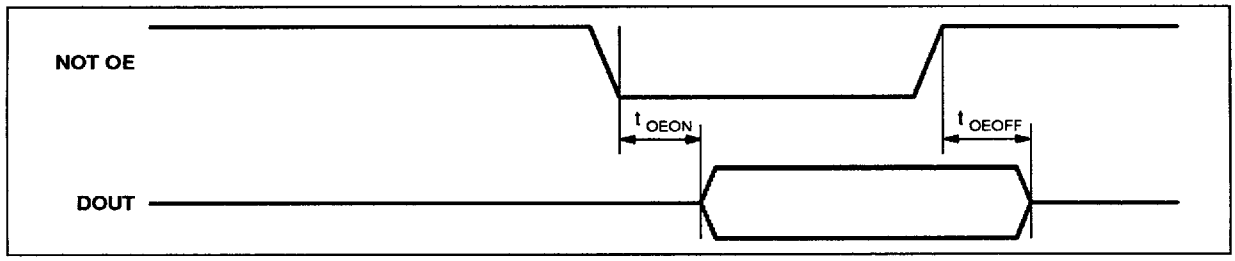
Figure 6



ASYNCHRONOUS CONTROL (notOE)

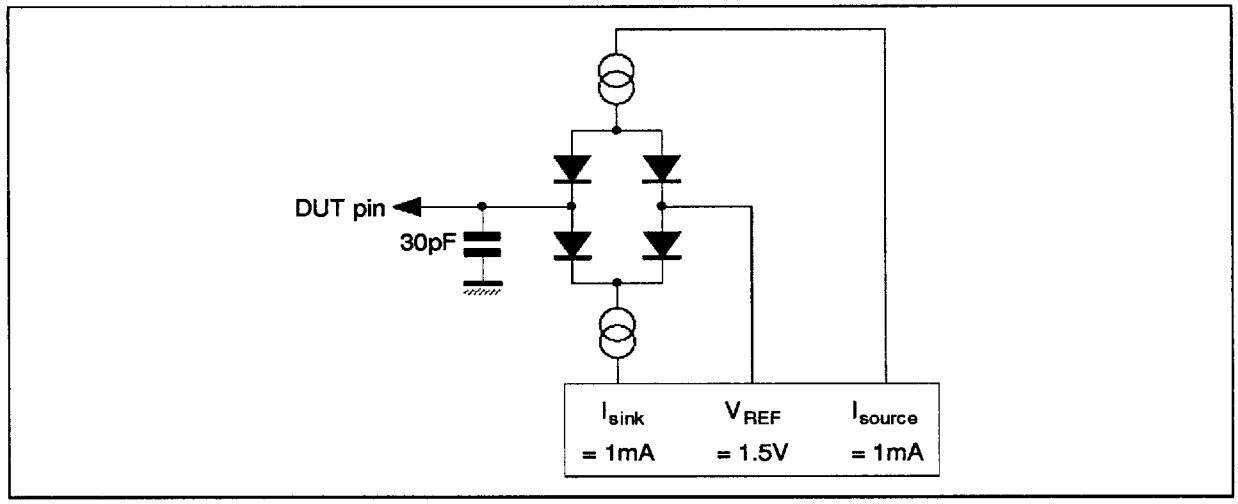
Symbol	Parameter	Min	Typ.	Max	Units	Notes
t_{OEON}	notOE to Dout enabled			15	ns	
t_{OEOFF}	notOE to Dout high impedance			15	ns	

Figure 7

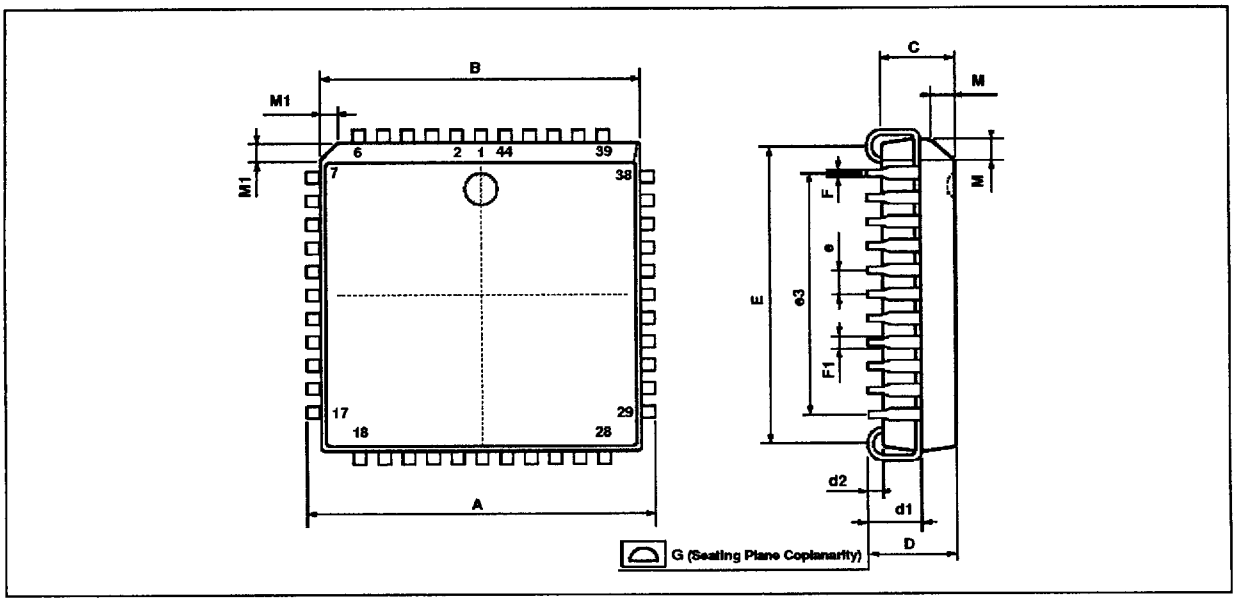


OUTPUT LOAD (output turn-off tests)

Figure 8



PACKAGE MECHANICAL DATA
44 PINS - PLASTIC CHIP CARRIER



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		17.577			0.692	
B		16.612			0.654	
C		3.861			0.152	
D		4.369			0.172	
d1						
d2						
E						
e		1.270			0.050	
e3		12.70			0.500	
F						
F1		0.457			0.018	
G						
M						
M1		1.143			0.045	

PLCC44B.TBL