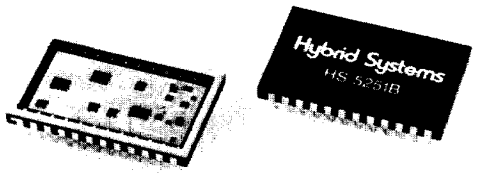
12-BIT LOW POWER CMOS ADC

FEATURES

- Low power: 80mW
- Low standby power: 10nW
- Adjustment-free, ±0.0125% linearity
- Small size: 24-pin DIP
  Full Mil operation −55°C to +125°C
- Full MIL-STD-883, Class B or commercial processing
- Improved replacement for MN5251
- No missing codes: 0°C to +70°C



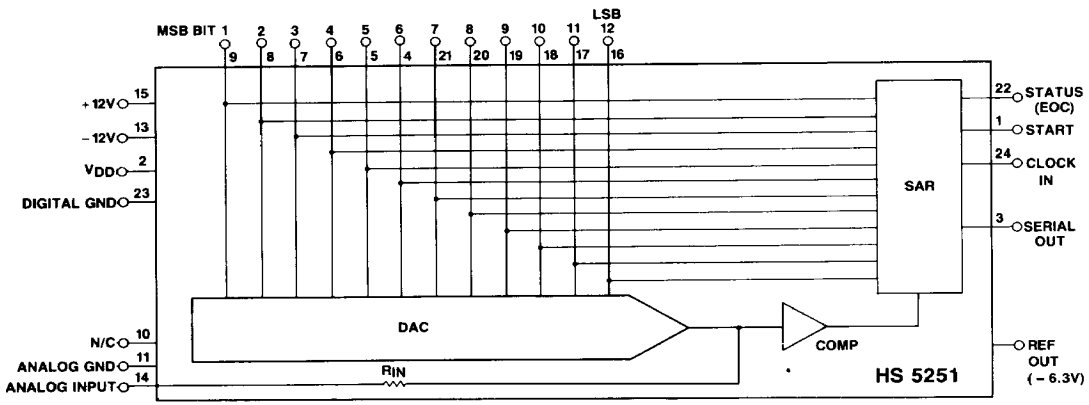
DESCRIPTION

The HS5251 Series is a complete adjustment free successive approximation type ADC requiring a low 80mW of power. The ADC provides digital output in both parallel or serial form. The HS5251 is packaged in a hermetically-sealed dual-in-line package and has the pinout of the popular HS5200 family of ADC's.

Miniature size, ultra low power consumption and adjustment free operation are product features. The HS5251 provides the user with the best possible performance in systems requiring maximum reliability in the smallest space. All converters are completely laser-trimmed, adjustment free, and incorporate highly stable thin-film resistor networks which provide long term maintenance free operation. Linearity of ±½ LSB is guaranteed over the entire operating temperature range.

All models of the HS5251 may be procured for operation over the −55°C to +125°C military temperature range ("B" models) with the same operating characteristics as the commercial 0°C to +70°C range. In addition, full military temperature range models are available screened to MIL-STD-883 Rev. C, Level B and are processed in accordance with the Method 5008.1.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

(Typical @ +25°C with ±12V, and V_{DD} = +5V, unless otherwise specified)

SERIES	**HS 5251**
TYPE	Successive Approximation
RESOLUTION	12 Bits
ANALOG INPUTS	
Bipolar Range	±5V
Impedance	50kΩ
DIGITAL INPUTS (CMOS Compatible)	
Logic Level	
Logic 1	3.5V min, V_{DD} = +5V 8.4V min, V_{DD} = +12V
Logic 0	1.5 max, V_{DD} = +5V 3.5 max, V_{DD} = +12V
Loading	
Input Current	10pA
Input Capacitance	5pF
Pulse Width (Start)	750ns min, V_{DD} = +5V 250ns min, V_{DD} = +12V
Clock Input	
Frequency	71kHz max
Pulse Width	600ns min, V_{DD} = +5V 300ns min, V_{DD} = +12V
Rise/Fall Time	15µs max, V_{DD} = +5V 4µs max, V_{DD} = +12V
DIGITAL OUTPUTS	
Parallel Data	
Output Codes	
Unipolar	Complementary Binary
Bipolar	Complementary Offset Binary
Logic Levels	
Logic 1	4.95V min, V_{DD} = +5V 11.95V min, V_{DD} = +12V
Logic 0	0.01V max, V_{DD} = +5V 0.05V max, V_{DD} = +12V
Output Drive	
Logic 1	0.2mA min, V_{DD} = +5V, V_{OH} = 2.5V 0.3mA min, V_{DD} = +12V, V_{OH} = 11V
Logic 0	0.1mA min, V_{DD} = +5V, V_{OH} = 0.4V 1.0mA min, V_{DD} = +12V, V_{OH} = 1.5V
Serial Output	NRZ (see coding)

REFERENCE, INTERNAL	
Voltage	−6.3V ±5%
Drift	±15ppm/°C
Output Current	10µA max
CONVERSION TIME/ THROUGHPUT RATE	175µs max/5.7kHz
ACCURACY	
Linearity, +25°C	±0.012% max
Over Temperature (Tmin to Tmax)	
C-Model	±0.012% max
B-Model	±0.024% max
Differential Linearity	½ LSB
Monotonicity[5]	No Missing Codes
Absolute Accuracy[2] +25°C	±0.05% FSR, ±0.1% FSR max
Over Temperature (Tmin to Tmax)	
C-Model	±0.2% FSR, ±0.5% FSR max
B-Model	±0.3% FSR, ±0.6% FSR max
Zero Error, +25°C	±0.01% FSR, .1% max
Over Temperature (Tmin to Tmax)	
C-Model	±0.04% FSR, ±0.1% FSR max
B-Model	±0.05% FSR, ±0.1% FSR max
Gain Error	±0.05% FSR, .1% max
Gain TC	±20% ppm/°C
POWER SUPPLY	
Requirements	
+12V, rated	+11.64V to +12.36V, @ 3.5mA max
−12V, rated	−11.64V to −12.36V, @ −2.7mA max
V_{DD}[1] (+5V nominal)	+4.75 to +12.36, @ 1.0mA
Rejection Ratio	
+12V	±0.003% FSR/%
−12V	±0.03% FSR/%
V_{DD} (+5V nominal)	±0.0003% FSR/%
Power	56mW, 80mW max
TEMPERATURE	
Operating	
C-Model	0° to +70°C
B-Model	−55°C to +125°C
Storage	−65°C to +150°C

NOTES:
1. V_{DD} logic is CMOS compatible. It can vary between +5V and +12V as indicated.
2. Absolute accuracy includes all errors, gain, zero, and linearity.
3. For proper operation ±12V power supplies tolerance should not be greater than ±3%
4. FSR is the abbreviation for "Full Scale Range" and is equal to the peak to peak output voltage, i.e. 10V for ±5V range.
5. No missing codes 0°C to +70°C

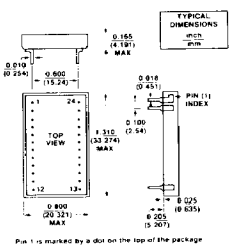
PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	START	24	CLOCK INPUT
2	V_{DD} (+5V)	23	DIGITAL GND
3	SERIAL OUT	22	STATUS (EOC)
4	BIT 6	21	BIT 7
5	BIT 5	20	BIT 8
6	BIT 4	19	BIT 9
7	BIT 3	18	BIT 10
8	BIT 2	17	BIT 11
9	BIT 1, MSB	16	BIT 12, LSB
10	N/C	15	+12V
11	ANALOG GROUND	14	ANALOG INPUT
12	REF OUT	13	−12V

ABSOLUTE MAXIMUM RATINGS

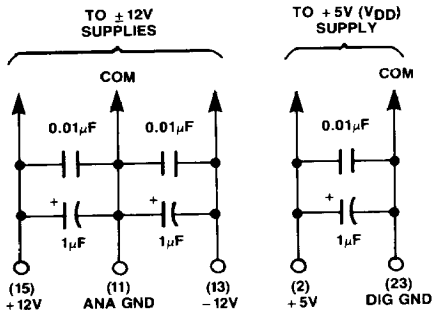
+12V Supply to Digital Common	+18V
−12V Supply to Digital Common	−18V
V_{DD} to Digital Common	−0.5V to +16V
Analog Input to Analog Common	±25V
Digital Inputs to Digital Common	−0.5V to +V_{DD}

PACKAGE OUTLINE



APPLICATIONS INFORMATION

RECOMMENDED POWER SUPPLY BYPASS CIRCUIT

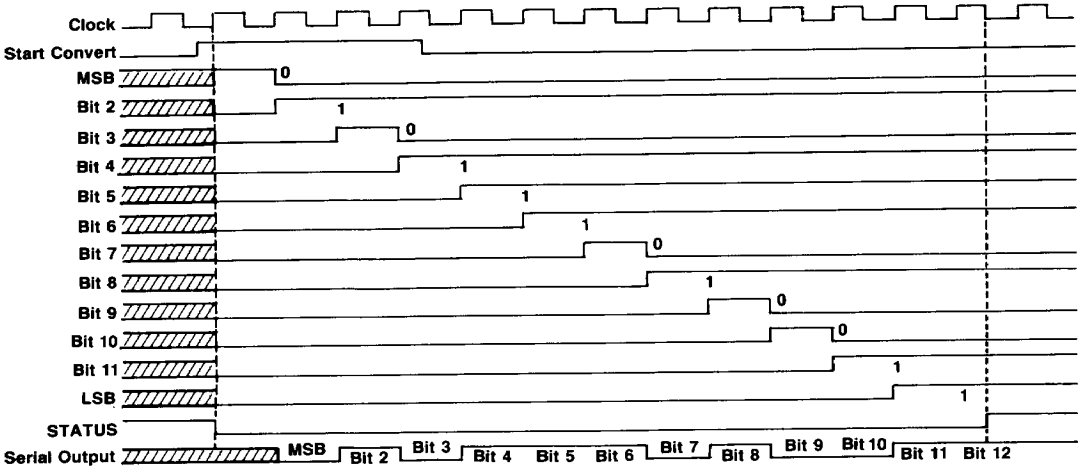


TRANSFER CHARACTERISTICS

DIGITAL OUTPUT CODE MSB LSB	BIPOLAR INPUT VOLTAGE RANGE
000000000000	+4.9976
100000000000	0.0000V
111111111110*	−4.9976V

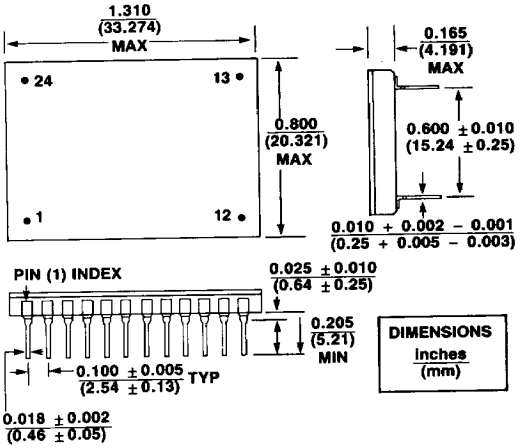
* The voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting the output bits indicated as 0 will change from "1" to "0" or from "0" to "1" as the input voltage passes through the level indicated.

TIMING DIAGRAM



NOTES:
1. Shaded areas shown for parallel data outputs denote bit states determined by successive approximation of analog input.
2. For continuous operation connect START (Pin 1) to STATUS (Pin 22)
3. Reset the converter by holding the start high during a low to high transition of the clock. The start must be high for a minimum of 300 nSec prior to the clock transition. The conversion will begin on the next low to high transition of the clock. The start may be set high at any time during a conversion to reset and begin again.
4. At the end of conversion, the E.O.C. will remain high until the converter is reset. The parallel data is valid for the entire time the E.O.C. is high.
5. The serial output is non-return to zero.
6. For the user's design flexibility, digital and analog grounds are brought out separately and must be externally connected. For optimum results, this external connection should be made as close to the converter as is possible.

9



CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electro-static fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

ORDERING INFORMATION

MODEL	DESCRIPTION
HS 5251C-12	Comm., 12-Bits, Low Power ADC
HS 5251B-12	MIL, 12-Bits, Low Power ADC