

Section 20 Electrical Characteristics

20.1 Absolute Maximum Ratings

Table 20.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	-0.3 to +7.0	V
Program voltage	V_{PP}	-0.3 to +13.5	V
Input voltage (except port C)	V_{in}	-0.3 to $V_{CC} + 0.3$	V
Input voltage (port C)	V_{in}	-0.3 to $AV_{CC} + 0.3$	V
Analog power supply voltage	AV_{CC}	-0.3 to +7.0	V
Analog reference voltage	AV_{ref}	-0.3 to $AV_{CC} + 0.3$	V
Analog input voltage	V_{AN}	-0.3 to $AV_{CC} + 0.3$	V
Operating temperature	T_{opr}	-20 to +75*	°C
Storage temperature	T_{stg}	-55 to +125	°C

Caution: Operating the LSI in excess of the absolute maximum rating may result in permanent damage.

Note: Normal Products: $T_{opr} = -40$ to $+85^{\circ}\text{C}$ for wide-temperature range products

20.2 DC Characteristics

Table 20.2 lists DC characteristics. Table 20.3 lists the permissible output current values.

Usage Conditions:

- Do not release AV_{CC} , AV_{ref} and AV_{SS} when the A/D converter is not in use. Connect AV_{CC} and AV_{ref} to V_{CC} and AV_{SS} to V_{SS} .
- The current consumption value is measured under conditions of $V_{IH\ min} = V_{CC} - 0.5\ V$ and $V_{IL\ max} = 0.5\ V$ with no load on any output pin and the on-chip pull-up MOS off.
- Even when the A/D converter is not used or is stand-by, connect AV_{CC} to AV_{ref} the power voltage(V_{CC}).

Table 20.2 DC Characteristics (1)

Conditions: $V_{CC} = 5.0\ V \pm 10\%$, $AV_{CC} = 5.0\ V \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\ V$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\ V$, $\phi = 20\ MHz$, $T_a = -20\ to\ +75^{\circ}C^{*}$)

Normal Products: $T_a = -40\ to\ +85^{\circ}C$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Measurement Unit	Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2-MD0	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port C		2.2	—	$AV_{CC} + 0.3$	V	
	Other input pins		2.2	—	$V_{CC} + 0.3$	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2-MD0	V_{IL}	-0.3	—	0.5	V	
	Other input pins		-0.3	—	0.8	V	
Schmitt trigger input voltage	PA13-PA10, PA2, PA0, PB7-PB0	V_T^{+}	4.0	—	—	V	
		V_T^{-}	—	—	1.0	V	
		$V_T^{+} - V_T^{-}$	0.4	—	—	V	
Input leak current	$\overline{RES}$	I_{linl}	—	—	1.0	μA	$V_{in} = 0.5\ to\ V_{CC} - 0.5\ V$
	NMI, MD2-MD0		—	—	1.0	μA	$V_{in} = 0.5\ to\ V_{CC} - 0.5\ V$
	Port C		—	—	1.0	μA	$V_{in} = 0.5\ to\ AV_{CC} - 0.5\ V$
3-state leak current (while off)	Ports A and B, $\overline{CS3}$ - $\overline{CS0}$, A21-A0, AD15-AD0	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0.5\ to\ V_{CC} - 0.5\ V$
Input pull-up MOS current	PA3	$-I_p$	20	—	300	μA	$V_{in} = 0V$
Output high-level voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\ \mu A$
			3.5	—	—	V	$I_{OH} = -1\ mA$

Table 20.2 DC Characteristics (2)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 20\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$)

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Output low level voltage	All output pins	V _{OL}	—	—	0.4	V	I _{OL} = 1.6 mA
			—	—	1.2	V	I _{OL} = 8 mA
Input capacitance	RES	C _{in}	—	—	30	pF	V _{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All other input pins		—	—	20	pF	T _a = 25°C
Current consumption	Ordinary operation	I _{CC}	—	60	90	mA	f = 12.5 MHz
			—	80	110	mA	f = 16.6 MHz
			—	100	130	mA	f = 20 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
			—	50	80	mA	f = 16.6 MHz
			—	60	90	mA	f = 20 MHz
	Standby		—	0.01	5 ^{*1}	μA	T _a ≤ 50°C
			—	—	20.0 ^{*2}	μA	50°C < T _a
Analog power supply current	During A/D conversion	AI _{CC}	—	1.0	2	mA	
	While A/D converter is waiting		—	0.01	5	μA	
Reference power supply current	During A/D conversion	AI _{ref}	—	0.5	1	mA	AV _{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5	μA	
RAM stand-by voltage		V _{RAM}	2.0	—	—	V	

Notes: 1. 50 μA for the SH7032.
2. 300 μA for the SH7032.

Table 20.2 DC Characteristics (3)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 16.6\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*)$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	$V_{CC} - 0.7$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port C		2.2	—	$AV_{CC} + 0.3$	V	
	Other input pins		2.2	—	$V_{CC} + 0.3$	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	−0.3	—	0.5	V	
	Other input pins		−0.3	—	0.8	V	
Schmidt trigger input voltage	PA13–10, PA2, PA0, PB7–PB0	V_{T^+}	4.0	—	—	V	
		V_{T^-}	—	—	1	V	
		$V_{T^+} - V_{T^-}$	0.4	—	—	V	
Input leak current	$\overline{RES}$	I_{linl}	—	—	1.0	μA	$V_{in} = 0.5$ to $V_{CC} - 0.5\text{ V}$
	NMI, MD2–MD0		—	—	1.0	μA	$V_{in} = 0.5$ to $V_{CC} - 0.5\text{ V}$
	Port C		—	—	1.0	μA	$V_{in} = 0.5$ to $AV_{CC} - 0.5\text{ V}$
3-state leak current (while off)	Ports A and B, $\overline{CS3}$ – $\overline{CS0}$, A21–A0, AD15–AD0	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0.5$ to $V_{CC} - 0.5\text{ V}$
Input pull-up MOS current	PA3	− I_p	20	—	300	μA	$V_{in} = 0\text{ V}$
Output high-level voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\text{ }\mu\text{A}$
			3.5	—	—	V	$I_{OH} = -1\text{ mA}$
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
			—	—	1.2	V	$I_{OL} = 8\text{ mA}$

Table 20.2 DC Characteristics (4)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 16.6\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*)$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input capacitance	RES	C_{in}	—	—	30	pF	$V_{in} = 0\text{ V}$
	NMI		—	—	30	pF	$f = 1\text{ MHz}$
	All other input pins		—	—	20	pF	$T_a = 25^\circ\text{C}$
Current consumption	Ordinary operation	I_{CC}	—	60	90	mA	$f = 12.5\text{ MHz}$
			—	80	110	mA	$f = 16.6\text{ MHz}$
	Sleep		—	40	70	mA	$f = 12.5\text{ MHz}$
			—	50	80	mA	$f = 16.6\text{ MHz}$
	Standby		—	0.01	5 ^{*1}	μA	$T_a \leq 50^\circ\text{C}$
			—	—	20.0 ^{*2}	μA	$50^\circ\text{C} < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	1.0	2.0	mA	
	While A/D converter is waiting		—	0.01	5	μA	
Reference power supply current	During A/D conversion	AI_{CC}	—	0.5	1	mA	$AV_{ref} = 5.0\text{ V}$
	While A/D converter is waiting		—	0.01	5	μA	
RAM stand-by	voltage	V_{RAM}	2.0	—	—	V	

Notes: 1. $50\text{ }\mu\text{A}$ for the SH7032.
2. $300\text{ }\mu\text{A}$ for the SH7032.

Table 20.2 DC Characteristics (5)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ to }5.5\text{ V}$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0\text{ V to }AV_{CC}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 12.5\text{ MHz}$, $T_a = -20\text{ to }+75^\circ\text{C}^*)$

Normal Products: $T_a = -40\text{ to }+85^\circ\text{C}$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input high-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IH}	$V_{CC} \times 0.9$	—	$V_{CC} + 0.3$	V	
	EXTAL		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
	Port C		$V_{CC} \times 0.7$	—	$AV_{CC} + 0.3$	V	
	Other input pins		$V_{CC} \times 0.7$	—	$V_{CC} + 0.3$	V	
Input low-level voltage	$\overline{RES}$, NMI, MD2–MD0	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	Other input pins		–0.3	—	$V_{CC} \times 0.2$	V	
Schmidt trigger input voltage	PA13–10, PA2, PA0, PB7–PB0	V_{T^+}	$V_{CC} \times 0.9$	—	—	V	
		V_{T^-}	—	—	$V_{CC} \times 0.2$	V	
		$V_{T^+} - V_{T^-}$	$V_{CC} \times 0.07$	—	—	V	
Input leak current	$\overline{RES}$	I_{linl}	—	—	1.0	μA	$V_{in} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	NMI, MD2–MD0		—	—	1.0	μA	$V_{in} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
	Port C		—	—	1.0	μA	$V_{in} = 0.5\text{ to }AV_{CC} - 0.5\text{ V}$
3-state leak current (while off)	Ports A and B, $\overline{CS3}$ – $\overline{CS0}$, A21–A0, AD15–AD0	$ I_{TSI} $	—	—	1.0	μA	$V_{in} = 0.5\text{ to }V_{CC} - 0.5\text{ V}$
Input pull-up MOS current	PA3	$-I_p$	20	—	300	μA	$V_{in} = 0\text{ V}$
Output high-level voltage	All output pins	V_{OH}	$V_{CC} - 0.5$	—	—	V	$I_{OH} = -200\text{ }\mu\text{A}$
			$V_{CC} - 1.0$	—	—	V	$I_{OH} = -1\text{ mA}$
Output low level voltage	All output pins	V_{OL}	—	—	0.4	V	$I_{OL} = 1.6\text{ mA}$
			—	—	1.2	V	$I_{OL} = 8\text{ mA}$

Table 20.2 DC Characteristics (6)

Conditions: $V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $AV_{CC} = 3.0\text{ to }5.5\text{ V}$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0\text{ V to }AV_{CC}$, $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 12.5\text{ MHz}$, $T_a = -20\text{ to }+75^\circ\text{C}^*)$

Normal Products: $T_a = -40\text{ to }+85^\circ\text{C}$ for wide-temperature range products.

Item		Symbol	Min	Typ	Max	Unit	Measurement Conditions
Input capacitance	RES	C _{in}	—	—	30	pF	V _{in} = 0 V
	NMI		—	—	30	pF	f = 1 MHz
	All other input pins		—	—	20	pF	T _a = 25°C
Current consumption	Ordinary operation	I _{CC}	—	60	90	mA	f = 12.5 MHz
	Sleep		—	40	70	mA	f = 12.5 MHz
	Standby		—	0.01	5 ^{*1}	μA	T _a ≤ 50°C
			—	—	20.0 ^{*2}	μA	50°C < T _a
Analog power supply current	During A/D conversion	A _I CC	—	0.5	1.5	mA	AV _{CC} = 3.0 V
			—	1.0	2.0	mA	AV _{CC} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	μA	
Reference power supply current	During A/D conversion	A _I ref	—	0.4	0.8	mA	AV _{ref} = 3.0 V
			—	0.5	1	mA	AV _{ref} = 5.0 V
	While A/D converter is waiting		—	0.01	5.0	μA	
RAM stand-by voltage		V _{RAM}	2.0	—	—	V	

Notes: 1. 50 μA for the SH7032.
2. 300 μA for the SH7032.
3. I_{CC} depends on V_{CC} and f as follows.
 $I_{CC}\text{ max.} = 1.0\text{ (mA)} + 1.29\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [ordinary operation]
 $I_{CC}\text{ max.} = 1.0\text{ (mA)} + 1.00\text{ (mA/MHz} \cdot \text{V)} \times V_{CC} \times f$ [sleep]

Table 20.3 Permitted Output Current Values

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$)

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$)

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Case A			Case B						Unit
		12.5 MHz			16.6 MHz			20 MHz			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output low-level permissible current (per pin)	I_{OL}	—	—	10	—	—	10	—	—	10	mA
Output low-level permissible current (total)	ΣI_{OL}	—	—	80	—	—	80	—	—	80	mA
Output high-level permissible current (per pin)	$-I_{OH}$	—	—	2.0	—	—	2.0	—	—	2.0	mA
Output high-level permissible current (total)	$-\Sigma I_{OH}$	—	—	25	—	—	25	—	—	25	mA

Caution: To ensure LSI reliability, do not exceed the value for output current given in table 20.3.

20.3 AC Characteristics

The following AC timing chart represents the AC characteristics, not signal functions. For signal functions, see the explanation in the text.

20.3.1 Clock Timing

Table 20.4 Clock Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 20$ MHz, $T_a = -20$ to $+75^{\circ}\text{C}^*)$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 20$ MHz, $T_a = -20$ to $+75^{\circ}\text{C}^*)$

Normal Products: $T_a = -40$ to $+85^{\circ}\text{C}$ for wide-temperature range products.

Item	Sym- bol	Case A		Case B				Unit	Figures
		12.5 MHz		16.6 MHz		20 MHz			
		Min	Max	Min	Max	Min	Max		
EXTAL input high level pulse width	t _{EXH}	20	—	10	—	10	—	ns	20.1
EXTAL input low level pulse width	t _{EXL}	20	—	10	—	10	—	ns	
EXTAL input rise time	t _{EXr}	—	10	—	5	—	5	ns	
EXTAL input fall time	t _{EXf}	—	10	—	5	—	5	ns	
Clock cycle time	t _{cyc}	80	500	60	500	50	500	ns	20.1, 20.2
Clock high pulse width	t _{CH}	30	—	20	—	20	—	ns	20.2
Clock low pulse width	t _{CL}	30	—	20	—	20	—	ns	
Clock rise time	t _{Cr}	—	10	—	5	—	5	ns	
Clock fall time	t _{Cf}	—	10	—	5	—	5	ns	
Reset oscillation settling time	t _{OSC1}	10	—	10	—	10	—	ms	20.3
Software standby oscillation settling time	t _{OSC2}	10	—	10	—	10	—	ms	

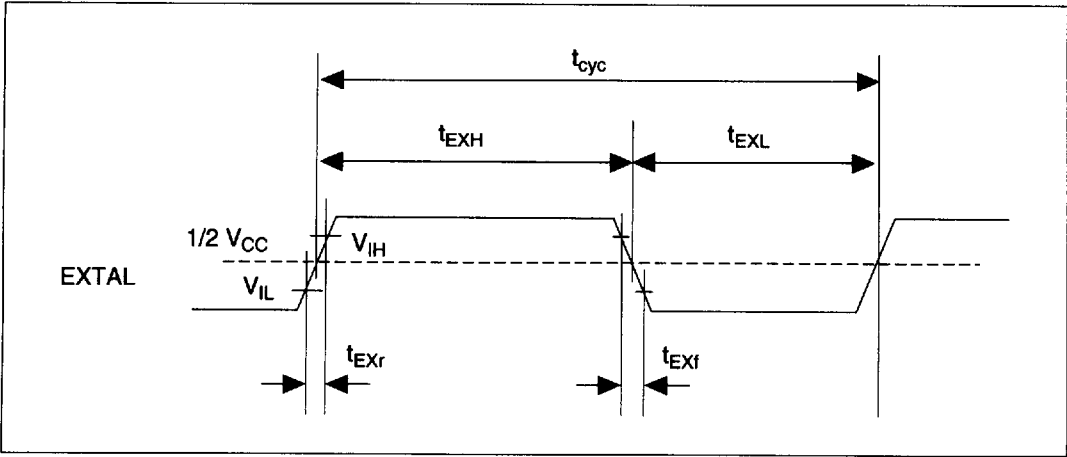


Figure 20.1 EXTAL Input Timing

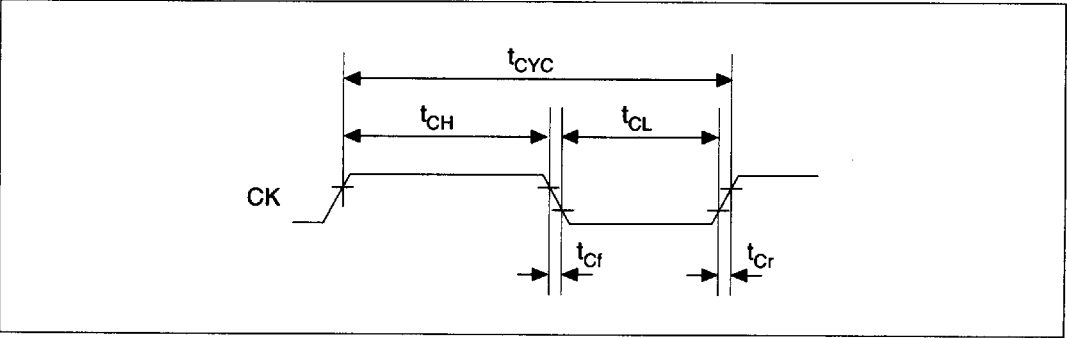


Figure 20.2 System Clock Timing

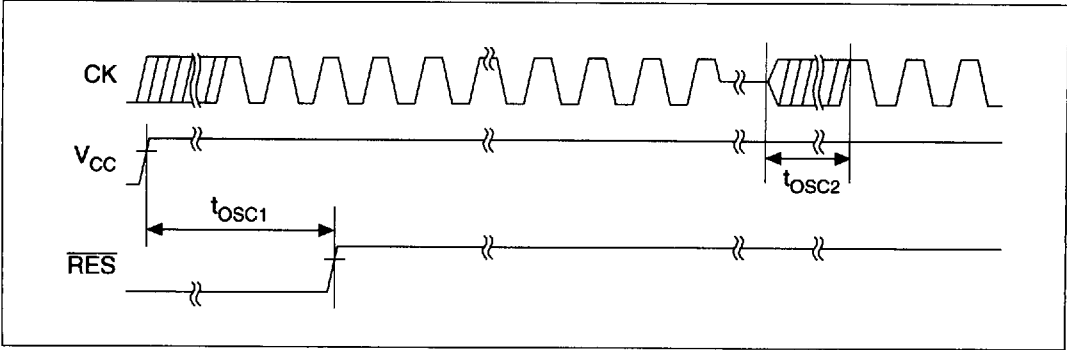


Figure 20.3 Oscillation Settling Time

20.3.2 Control Signal Timing

Table 20.5 Control Signal Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$)

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$)

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Case A		Case B				Unit	Figure
		12.5 MHz		16.6 MHz		20 MHz			
		Min	Max	Min	Max	Min	Max		
RES setup time	t _{RESS}	320	—	240	—	200	—	ns	20.4
RES pulse width	t _{RESW}	20	—	20	—	20	—	t _{cyc}	
NMI reset setup time	t _{NMIRS}	320	—	240	—	200	—	ns	
NMI reset hold time	t _{NMIRH}	320	—	240	—	200	—	ns	20.5
NMI setup time	t _{NMIS}	160	—	120	—	100	—	ns	
NMI hold time	t _{NMIH}	80	—	60	—	50	—	ns	
IRQ0–IRQ7 setup time (edge detection time)	t _{IRQES}	160	—	120	—	100	—	ns	20.6
IRQ0–IRQ7 setup time (level detection time)	t _{IRQLS}	160	—	120	—	100	—	ns	
IRQ0–IRQ7 hold time	t _{IRQEH}	80	—	60	—	50	—	ns	
IRQOUT output delay time)	t _{IRQOD}	—	80	—	60	—	50	ns	20.7
Bus request setup time	t _{BRQS}	80	—	60	—	50	—	ns	
Bus acknowledge delay time 1	t _{BACD1}	—	80	—	60	—	50	ns	
Bus acknowledge delay time 2	t _{BACD2}	—	80	—	60	—	50	ns	
Bus 3-state delay time	t _{BZD}	—	80	—	60	—	50	ns	

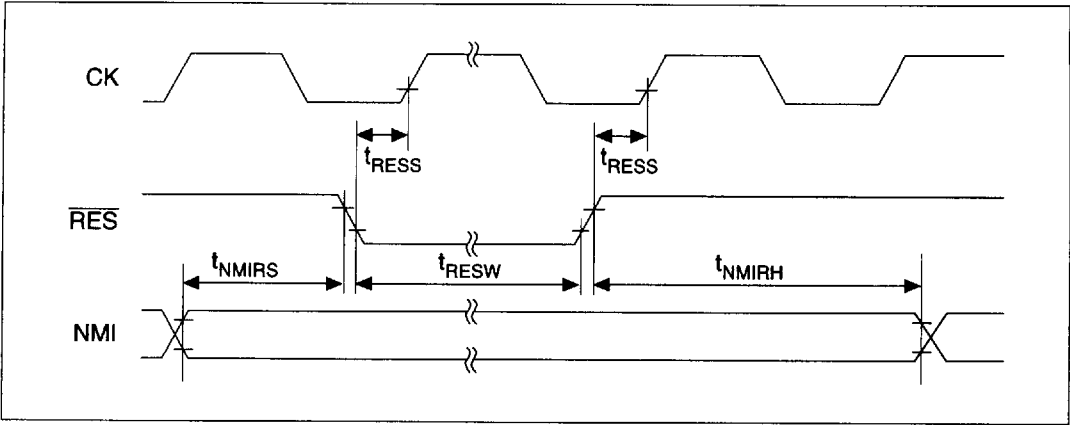


Figure 20.4 Reset Input Timing

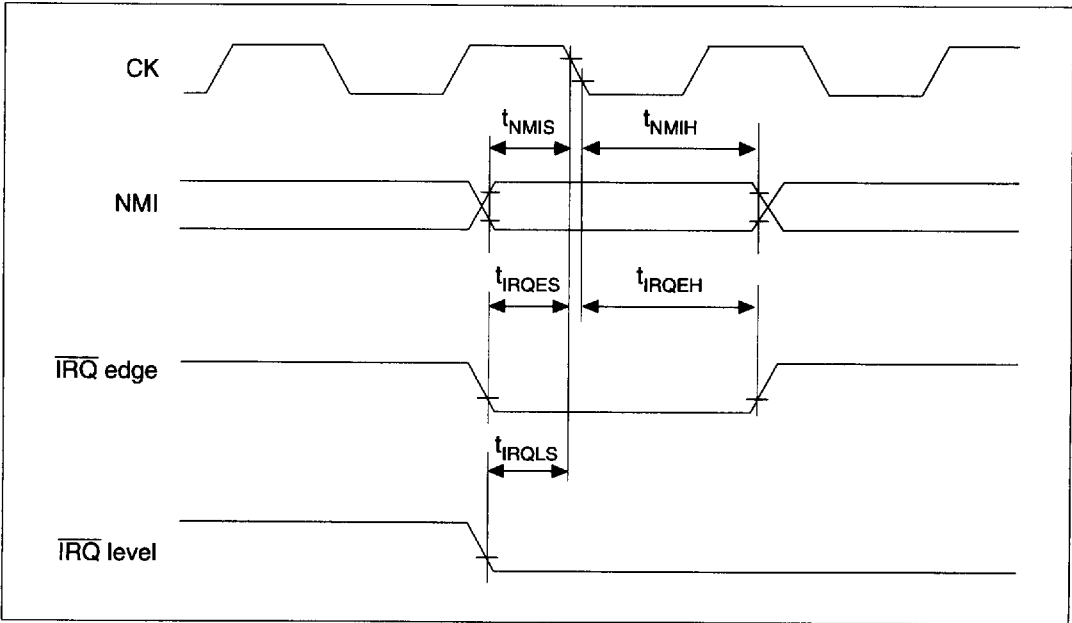


Figure 20.5 Interrupt Signal Input Timing

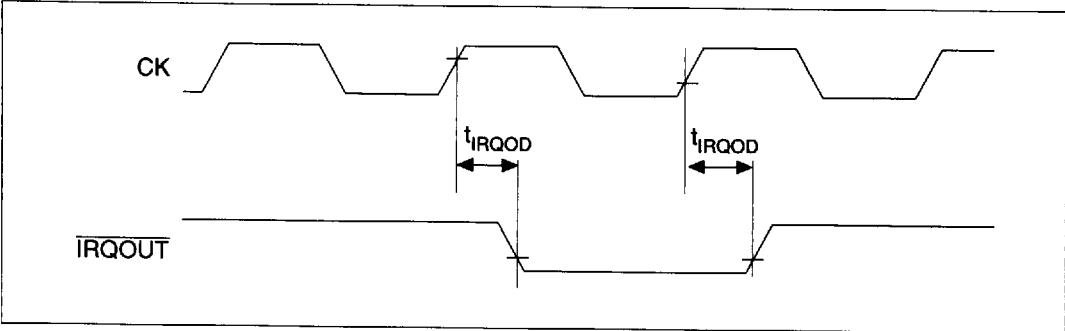


Figure 20.6 Interrupt Signal Output Timing

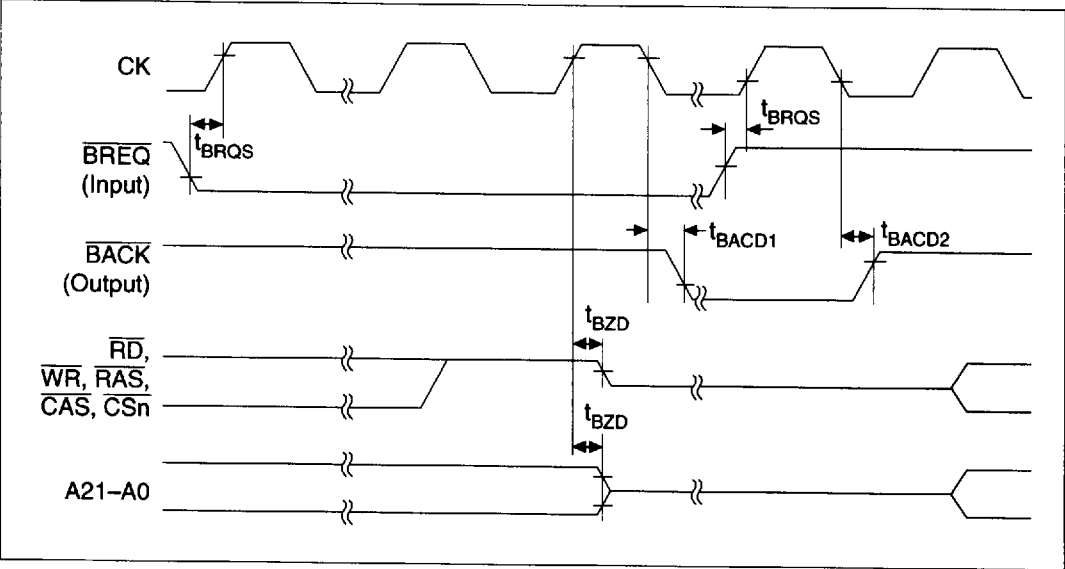


Figure 20.7 Bus Release Timing

20.3.3 Bus Timing

Table 20.6 Bus Timing (1)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 20\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	—	20^{*1}	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
$\overline{CS}$ delay time 1	t_{CSD1}	—	25	ns	20.8, 20.9, 20.20
$\overline{CS}$ delay time 2	t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	20	ns	20.19
$\overline{CS}$ delay time 4	t_{CSD4}	—	20	ns	
Access time 1 from read strobe	35% duty ^{*2} t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.8,
	50% duty	$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2 from read strobe	35% duty ^{*2} t_{RDAC2}	$t_{cyc} \times (n+1.65) - 20^{*3}$	—	ns	20.9, 20.10
	50% duty	$t_{cyc} \times (n+1.5) - 20^{*3}$	—	ns	
Access time 3 from read strobe	35% duty ^{*2} t_{RDAC3}	$t_{cyc} \times (n+0.65) - 20^{*3}$	—	ns	20.19
	50% duty	$t_{cyc} \times (n+0.5) - 20^{*3}$	—	ns	
Read strobe delay time	t_{RSD}	—	20	ns	20.8, 20.9, 20.11–20.15, 20.19, 20.24–20.28
Read data setup time	t_{RDS}	15	—	ns	20.8, 20.9, 20.11–20.14,
Read data hold time	t_{RDH}	0	—	ns	20.19
Write strobe delay time 1	t_{WSD1}	—	20	ns	20.9, 20.13, 20.14, 20.19, 20.20
Write strobe delay time 2	t_{WSD2}	—	20	ns	20.9, 20.13, 20.14, 20.19
Write strobe delay time 3	t_{WSD3}	—	20	ns	20.11, 20.12
Write strobe delay time 4	t_{WSD4}	—	20	ns	20.11, 20.12, 20.20
Write data delay time 1	t_{WDD1}	—	35	ns	20.9, 20.13, 20.14, 19
Write data delay time 2	t_{WDD2}	—	20	ns	20.11, 20.12
Write data hold time	t_{WDH}	0	—	ns	20.9, 20.11–20.14

Table 20.6 Bus Timing (1) (cont)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 20\text{ MHz}$, $T_a = -20\text{ to }+75^\circ\text{C}^*$

Normal Products: $T_a = -40\text{ to }+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Parity output delay time 1	t_{WPDD1}	—	40	ns	20.9, 20.13, 20.14
Parity output delay time 2	t_{WPDD2}	—	20	ns	20.11, 20.12
Parity output hold time	t_{WPDH}	0	—	ns	20.9, 20.11–20.14
Wait setup time	t_{WTS}	14	—	ns	20.10, 20.15, 20.19
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1	t_{ACC1}	$t_{cyc} - 30^{*4}$	—	ns	20.8, 20.11, 20.12
Read data access time 2	t_{ACC2}	$t_{cyc} \times (n+2) - 30^{*3}$	—	ns	20.9, 20.10, 20.13, 20.14
$\overline{\text{RAS}}$ delay time 1	t_{RASD1}	—	20	ns	20.11–20.14,
$\overline{\text{RAS}}$ delay time 2	t_{RASD2}	—	30	ns	20.16–20.18
$\overline{\text{CAS}}$ delay time 1	t_{CASD1}	—	20	ns	20.11
$\overline{\text{CAS}}$ delay time 2	t_{CASD2}	—	20	ns	20.13, 20.14,
$\overline{\text{CAS}}$ delay time 3	t_{CASD3}	—	20	ns	20.16–20.18
Column address setup time	t_{ASC}	0	—	ns	20.11, 20.12
Read data access 35% duty ^{*2}	t_{CAC1}	$t_{cyc} \times 0.65 - 19$	—	ns	
time from $\overline{\text{CAS}}$ 1 50% duty		$t_{cyc} \times 0.5 - 19$	—	ns	
Read data access time from $\overline{\text{CAS}}$ 2	t_{CAC2}	$t_{cyc} \times (n+1) - 25^{*3}$	—	ns	20.13, 20.14, 20.15
Read data access time from $\overline{\text{CAS}}$ 1	t_{RAC1}	$t_{cyc} \times 1.5 - 20$	—	ns	20.11, 20.12
Read data access time from $\overline{\text{RAS}}$ 2	t_{RAC2}	$t_{cyc} \times (n+2.5) - 20^{*3}$	—	ns	20.13, 20.14, 20.15
High-speed page mode $\overline{\text{CAS}}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.12

Table 20.6 Bus Timing (1) (cont)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 20\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
$\overline{AH}$ delay time 1	t_{AHD1}	—	20	ns	20.19
$\overline{AH}$ delay time 2	t_{AHD2}	—	20	ns	
Multiplexed address delay time	t_{MAD}	—	30	ns	
Multiplexed address hold time	t_{MAH}	0	—	ns	
DACK0, DACK1 delay time 1	t_{DACD1}	—	23	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
DACK0, DACK1 delay time 2	t_{DACD2}	—	23	ns	
DACK0, DACK1 delay time 3	t_{DACD3}	—	20	ns	20.9, 20.13, 20.14, 20.19
DACK0, DACK1 delay time 4	t_{DACD4}	—	20	ns	20.11, 20.12
DACK0, DACK1 delay time 5	t_{DACD5}	—	20	ns	
Read delay time	35% duty ^{*2} t_{RDD}	—	$t_{cyc} \times 0.35 + 12$	ns	20.8, 20.9, 20.11–20.15, 20.19, 20.24–20.28
	50% duty	—	$t_{cyc} \times 0.5 + 15$	ns	
Data setup time for $\overline{CAS}$	t_{DS}	0 ^{*5}	—	ns	20.11, 20.13
$\overline{CAS}$ setup time for $\overline{RAS}$	t_{CSR}	10	—	ns	20.16, 20.17, 20.18
Row address hold time	t_{RAH}	10	—	ns	20.11, 20.13
Write command hold time	t_{WCH}	15	—	ns	
Write command setup time	35% duty ^{*2} t_{WCS}	0	—	ns	20.11
	50% duty t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	t_{cyc} –20	—	ns	20.12

- Notes: 1. HBS and LBS signals are 25 ns.
2. When frequency is 10 MHz or more.
3. n is the number of wait cycles.
4. Access time from addresses A0 to A21 is t_{cyc} -25.
5. –5ns for parity output of DRAM long-pitch access.

Table 20.7 Bus Timing (2)

Conditions: $V_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = 5.0 \text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5 \text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0 \text{ V}$, $\phi = 16.6 \text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	—	25^{*1}	ns	20.8, 20.9, 20.11–20.14, 20.19, 20.20
$\overline{CS}$ delay time 1	t_{CSD1}	—	30	ns	20.8, 20.9, 20.20
$\overline{CS}$ delay time 2	t_{CSD2}	—	25	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	25	ns	20.19
$\overline{CS}$ delay time 4	t_{CSD4}	—	25	ns	
Access time 1 from read strobe	35% duty ^{*2} t_{RDAC1}	$t_{cyc} \times 0.65 - 20$	—	ns	20.8, 20.9,
	50% duty	$t_{cyc} \times 0.5 - 20$	—	ns	
Access time 2 from read strobe	35% duty ^{*2} t_{RDAC2}	$t_{cyc} \times (n + 1.65) - 20^{*3}$	—	ns	20.9, 20.10
	50% duty	$t_{cyc} \times (n + 1.5) - 20^{*3}$	—	ns	
Access time 3 from read strobe	35% duty ^{*1} t_{RDAC3}	$t_{cyc} \times (n + 0.65) - 20^{*3}$	—	ns	20.19
	50% duty	$t_{cyc} \times (n + 0.5) - 20^{*3}$	—	ns	
Read strobe delay time	t_{RSD}	—	25	ns	20.8, 20.9, 20.19
Read data setup time	t_{RDS}	15	—	ns	20.8, 20.9, 20.11–20.14,
Read data hold time	t_{RDH}	0	—	ns	20.19
Write strobe delay time 1	t_{WSD1}	—	25	ns	20.9, 20.13, 20.14, 20.19, 20.20
Write strobe delay time 2	t_{WSD2}	—	25	ns	20.9, 20.13, 20.14, 20.19
Write strobe delay time 3	t_{WSD3}	—	25	ns	20.11, 20.12
Write strobe delay time 4	t_{WSD4}	—	25	ns	20.11, 20.12, 20.20
Write data delay time 1	t_{WDD1}	—	45	ns	20.9, 20.13, 20.14, 20.19
Write data delay time 2	t_{WDD2}	—	25	ns	20.11, 20.12
Write data hold time	t_{WDH}	0	—	ns	20.9, 20.11–20.14
Parity output delay time 1	t_{WPDD1}	—	45	ns	20.9, 20.13, 20.14
Parity output delay time 2	t_{WPDD2}	—	25	ns	20.11, 20.12
Parity output hold time	t_{WPDH}	0	—	ns	20.9, 20.11–20.14

Table 20.7 Bus Timing (2) (cont)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 16.6\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Wait setup time	t_{WTS}	19	—	ns	20.10, 20.15, 20.19
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1	t_{ACC1}	$t_{cyc} - 30^{*4}$	—	ns	20.8, 20.11, 20.12
Read data access time 2	t_{ACC2}	$t_{cyc} \times (n+2) - 30^{*3}$	—	ns	20.9, 20.10, 20.13, 20.14
$\overline{RAS}$ delay time 1	t_{RASD1}	—	25	ns	20.11–20.14,
$\overline{RAS}$ delay time 2	t_{RASD2}	—	35	ns	20.16–20.18
$\overline{CAS}$ delay time 1	t_{CASD1}	—	25	ns	20.11
$\overline{CAS}$ delay time 2	t_{CASD2}	—	25	ns	20.13, 20.14,
$\overline{CAS}$ delay time 3	t_{CASD3}	—	25	ns	20.16–20.18
Column address setup time	t_{ASC}	0	—	ns	20.11, 20.12
Read data access time from CAS 1	t_{CAC1}	$t_{cyc} \times 0.65 - 19$	—	ns	
		50% duty	$t_{cyc} \times 0.5 - 19$	—	ns
Read data access time from $\overline{CAS}$ 2	t_{CAC2}	$t_{cyc} \times (n + 1) - 25^{*3}$	—	ns	20.13, 20.14, 20.15
Read data access time from $\overline{RAS}$ 1	t_{RAC1}	$t_{cyc} \times 1.5 - 20$	—	ns	20.11, 20.12
Read data access time from $\overline{RAS}$ 2	t_{RAC2}	$t_{cyc} \times (n + 2.5) - 20^{*3}$	—	ns	20.13, 20.14, 20.15
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.12
$\overline{AH}$ delay time 1	t_{AHD1}	—	25	ns	20.19
$\overline{AH}$ delay time 2	t_{AHD2}	—	25	ns	
Multiplexed address delay time	t_{MAD}	—	30	ns	
Multiplexed address hold time	t_{MAH}	0	—	ns	

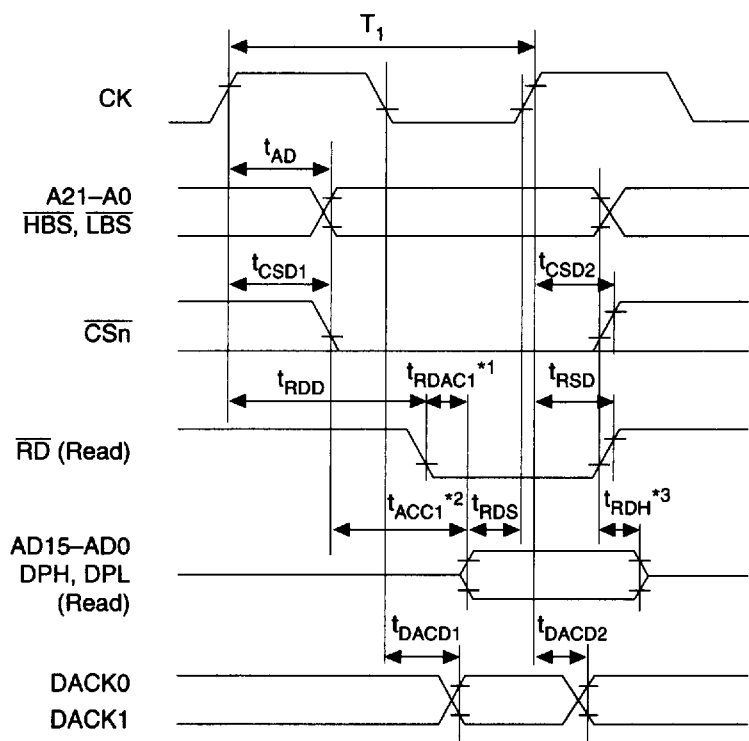
Table 20.7 Bus Timing (2) (cont)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $\phi = 16.6\text{ MHz}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

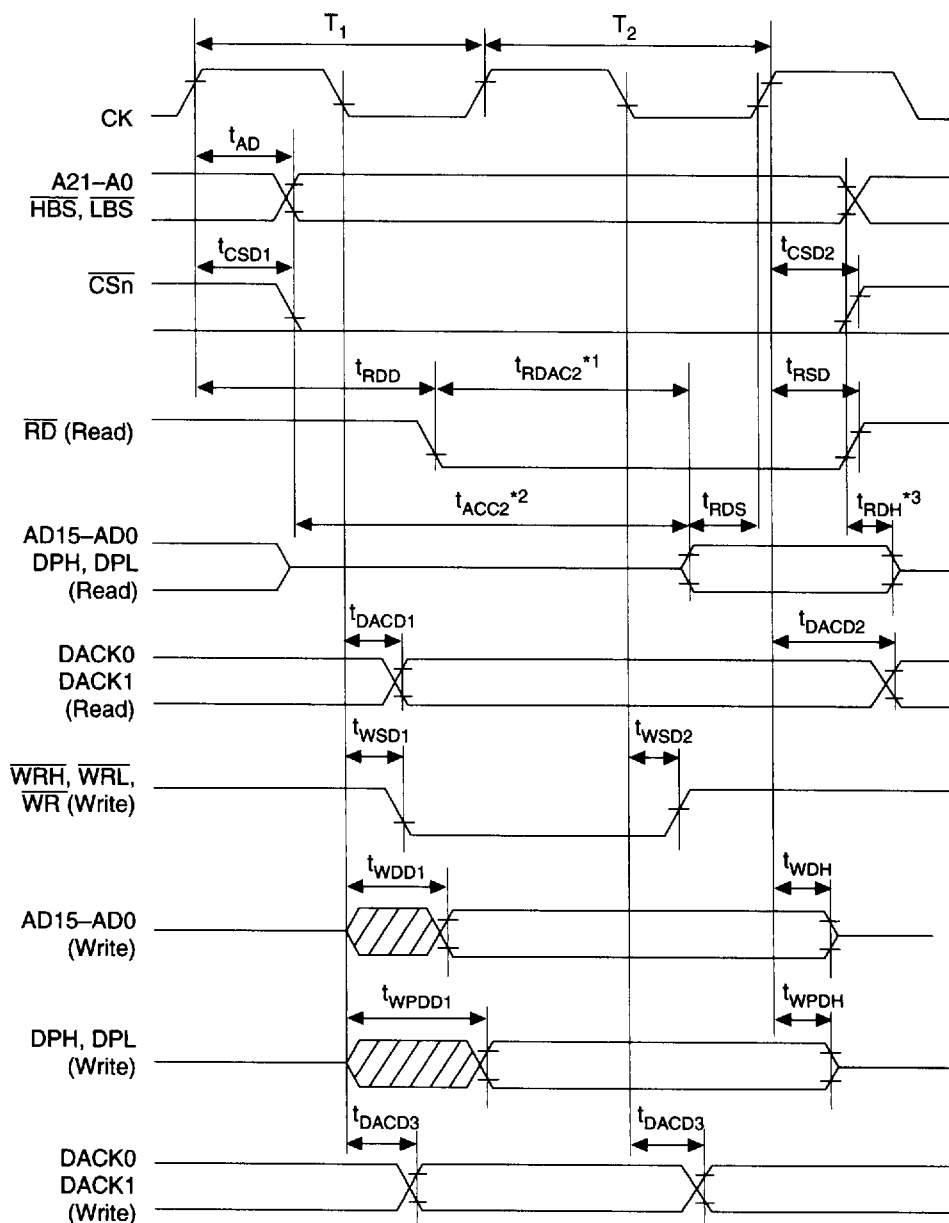
Item	Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1	t_{DACD1}	—	25	ns	20.8, 20.9, 20.11–20.14,
DACK0, DACK1 delay time 2	t_{DACD2}	—	25	ns	20.19, 20.20
DACK0, DACK1 delay time 3	t_{DACD3}	—	25	ns	20.9, 20.13, 20.14, 20.19
DACK0, DACK1 delay time 4	t_{DACD4}	—	25	ns	20.11, 20.12
DACK0, DACK1 delay time 5	t_{DACD5}	—	25	ns	
Read delay time	35% duty ^{*2} 50% duty	t_{RDD}	$t_{cyc} \times 0.35 + 12$	ns	20.8, 20.9, 20.11–20.15,
			$t_{cyc} \times 0.5 + 15$	ns	20.19, 20.24–20.28
Data setup time for $\overline{CAS}$	t_{DS}	0 ^{*5}	—	ns	20.11, 20.13
$\overline{CAS}$ setup time for $\overline{RAS}$	t_{CSR}	10	—	ns	20.16, 20.17, 20.18
Row address hold time	t_{RAH}	10	—	ns	20.11, 20.13
Write command hold time	t_{WCH}	15	—	ns	
Write command setup time	35% duty ^{*2} 50% duty	t_{WCS}	0	ns	20.11
			0	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	t_{cyc} –20	—	ns	20.12

- Notes
1. HBS and LBS signals are 30 ns.
 2. When frequency is 10 MHz or more
 3. n is the number of wait cycles.
 4. Access time from addresses A0 to A21 is t_{cyc} -25.
 5. –5ns for parity output of DRAM long-pitch access



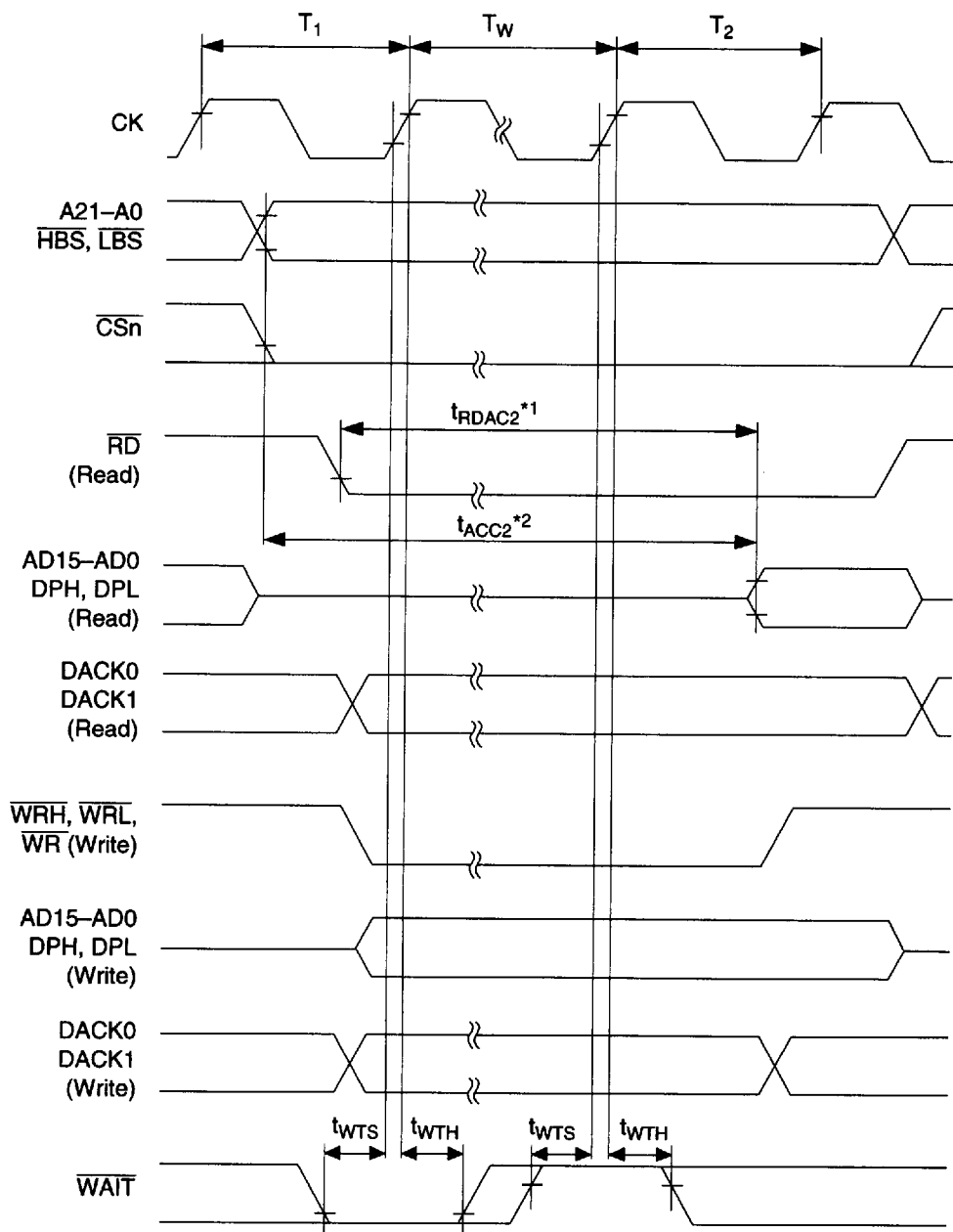
- Notes:
1. For t_{RDAC1} , use $t_{cyc} \times 0.65 - 20$ (for 35% duty) or $t_{cyc} \times 0.5 - 20$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.
 2. For t_{ACC1} , use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) - t_{RDS} .
 3. t_{RDH} is measured from A21-A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.8 Basic Bus Cycle: One-State Access



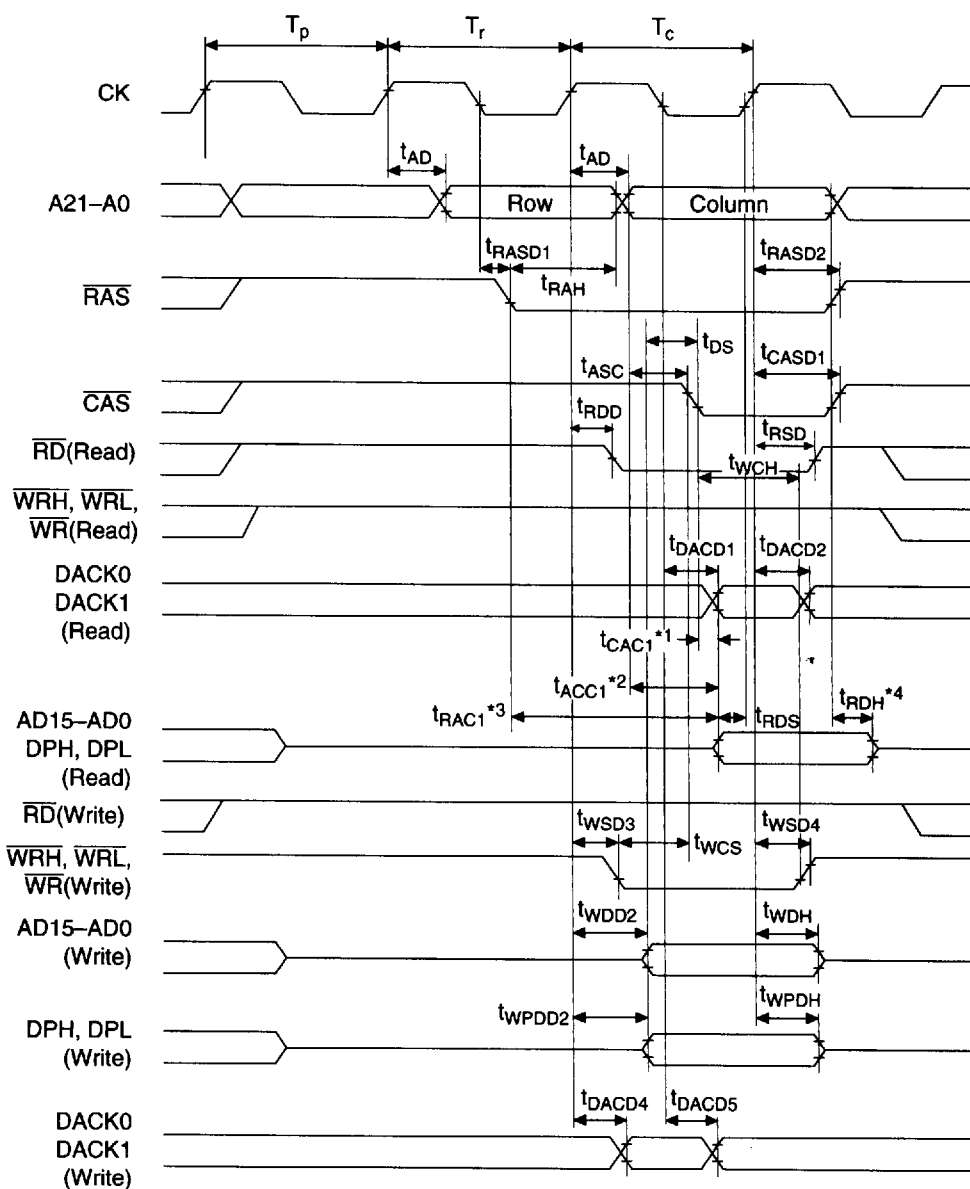
- Notes:
1. For t_{RDAC2} , use $t_{cyc} \times (n + 1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
 2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) - t_{RDS} .
 3. t_{RDH} is measured from A21-A0, $\overline{CS}_n$, or $\overline{RD}$, whichever is negated first.

Figure 20.9 Basic Bus Cycle: Two-State Access



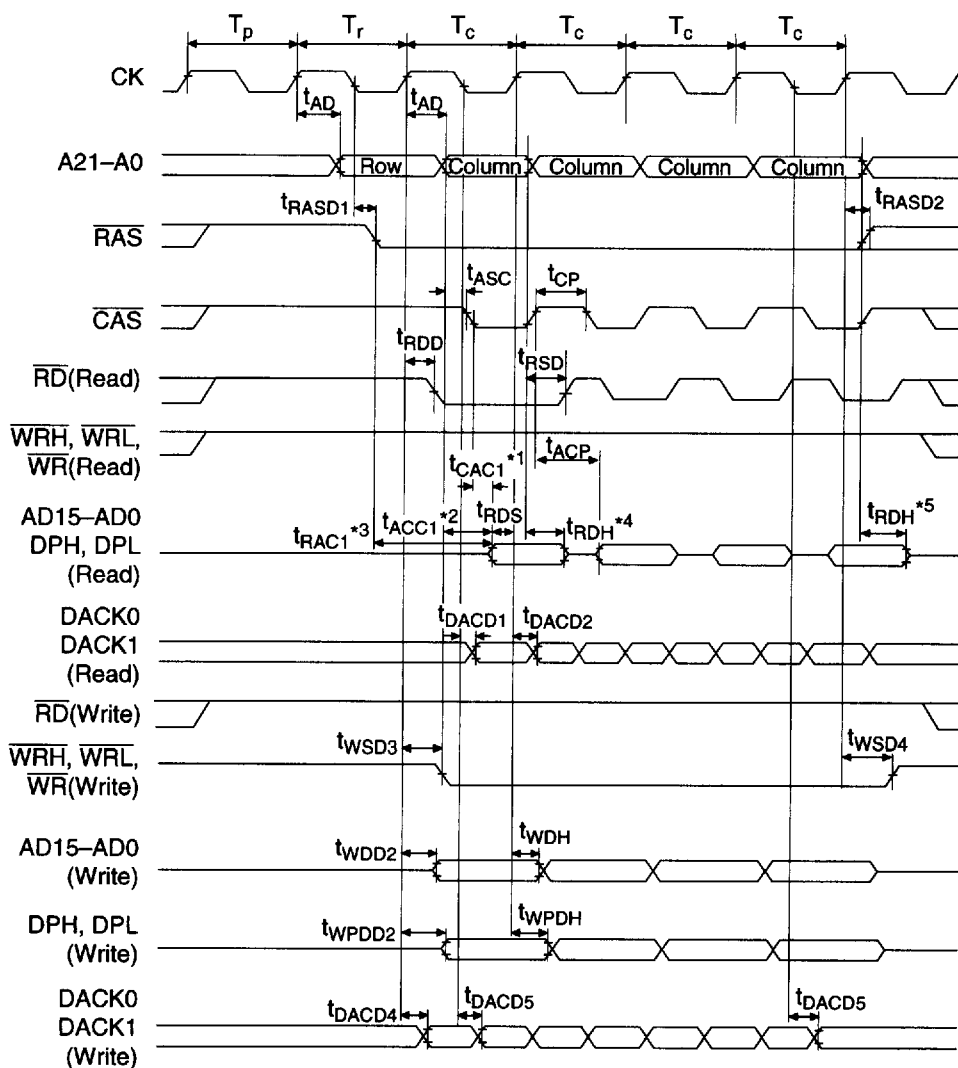
- Notes:
1. For t_{RDAC2} , use $t_{cyc} \times (n+1.65) - 20$ (for 35% duty) or $t_{cyc} \times (n+1.5) - 20$ (for 50% duty) instead of $t_{cyc} \times (n+2) - t_{RDD} - t_{RDS}$.
 2. For t_{ACC2} , use $t_{cyc} \times (n+2) - 30$ instead of $t_{cyc} \times (n+2) - t_{AD}$ (or t_{CSD1}) - t_{RDS} .

Figure 20.10 Basic Bus Cycle: Two States + Wait State



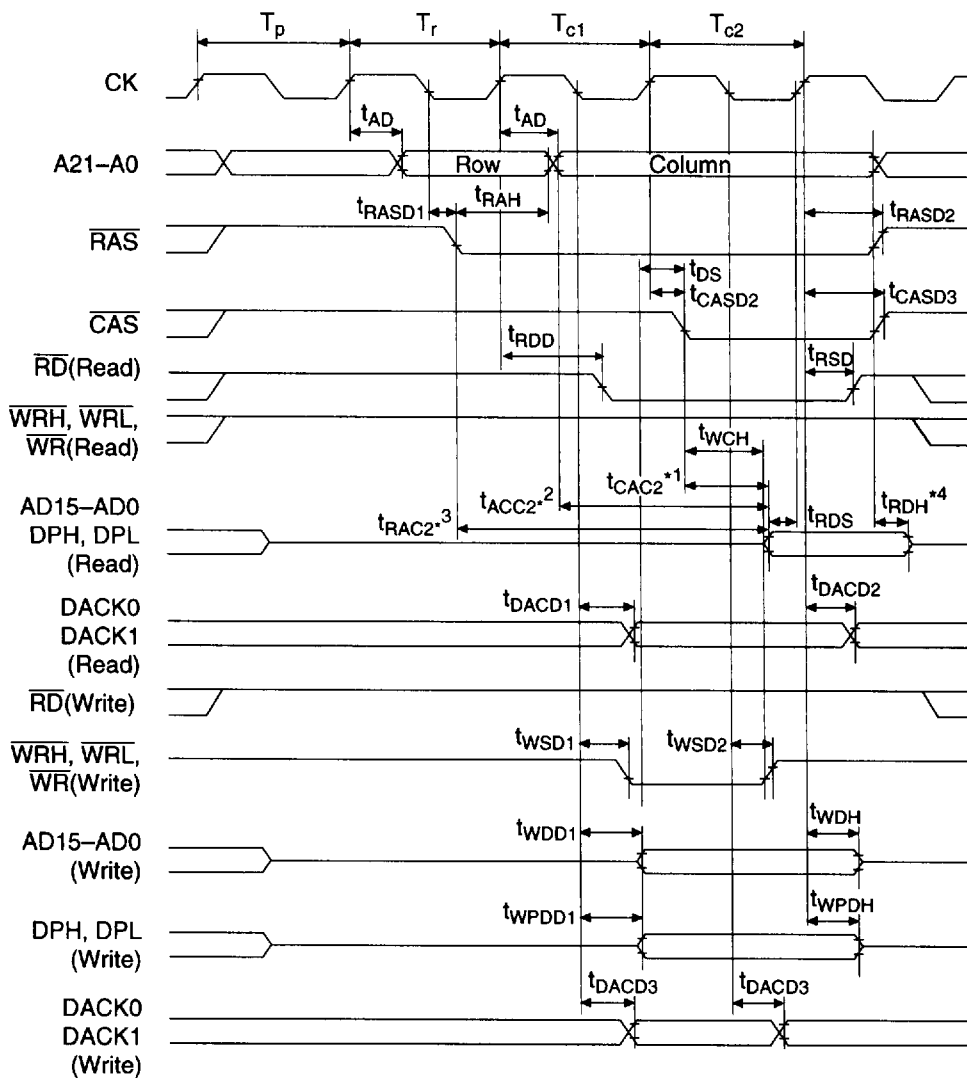
- Notes:
1. For t_{CAC1} , use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
 2. For t_{ACC1} , use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
 3. For t_{RAC1} , use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
 4. t_{RDH} is measured from A21-A0, RAS, or CAS, whichever is negated first.

Figure 20.11 DRAM Bus Cycle (Short Pitch, Normal Mode)



- Notes:
1. For t_{CAC1} , use $t_{cyc} \times 0.65 - 19$ (for 35% duty) or $t_{cyc} \times 0.5 - 19$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
 2. For t_{ACC1} , use $t_{cyc} - 30$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
 3. For t_{RAC1} , use $t_{cyc} \times 1.5 - 20$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
 4. t_{RDH} is measured from A21-A0 or $\overline{CAS}$, whichever is negated first.
 5. t_{RDH} is measured from A21-A0, $\overline{RAS}$, or $\overline{CAS}$, whichever is negated first.

Figure 20.12 DRAM Bus Cycle (Short Pitch, High-Speed Page Mode)



- Notes:
1. For t_{CAC2} , use $t_{cyc} \times (n + 1) - 25$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
 2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 30$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
 3. For t_{RAC2} , use $t_{cyc} \times (n + 2.5) - 20$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
 4. t_{RDH} is measured from A21-A0, $\overline{CAS}$, or $\overline{RAS}$, whichever is negated first.

Figure 20.13 DRAM Bus Cycle: (Long Pitch, Normal Mode)

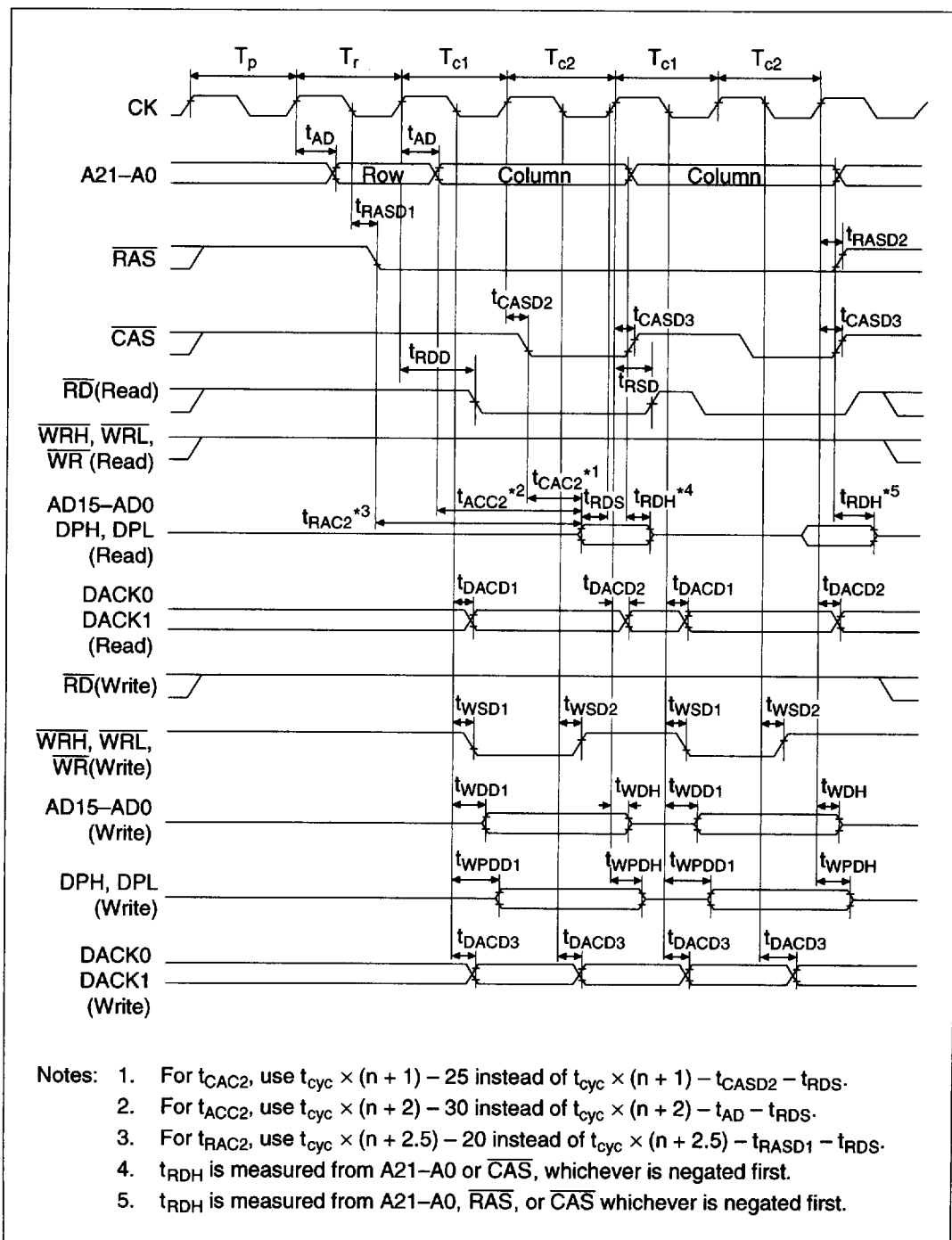


Figure 20.14 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode)

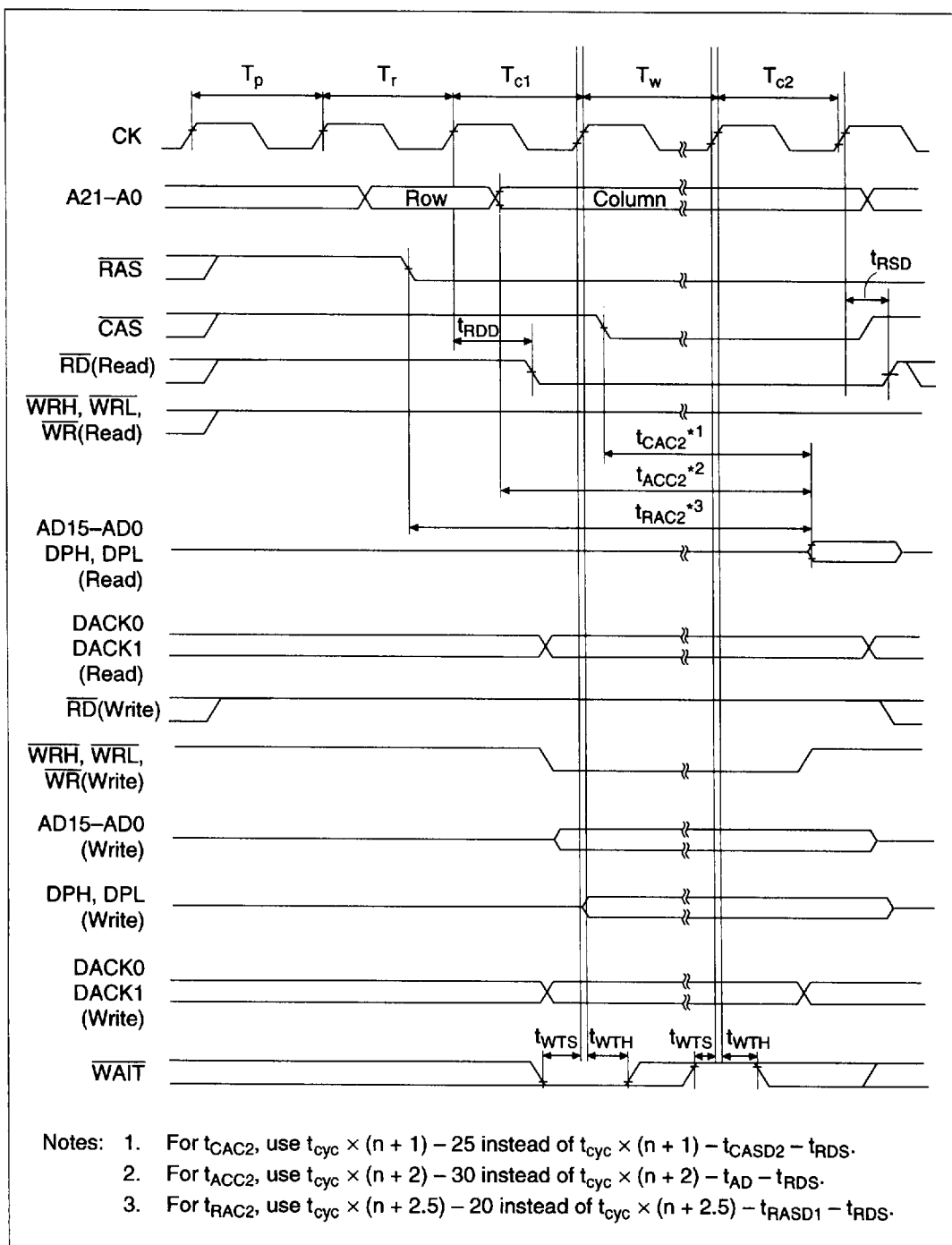


Figure 20.15 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode + Wait State)

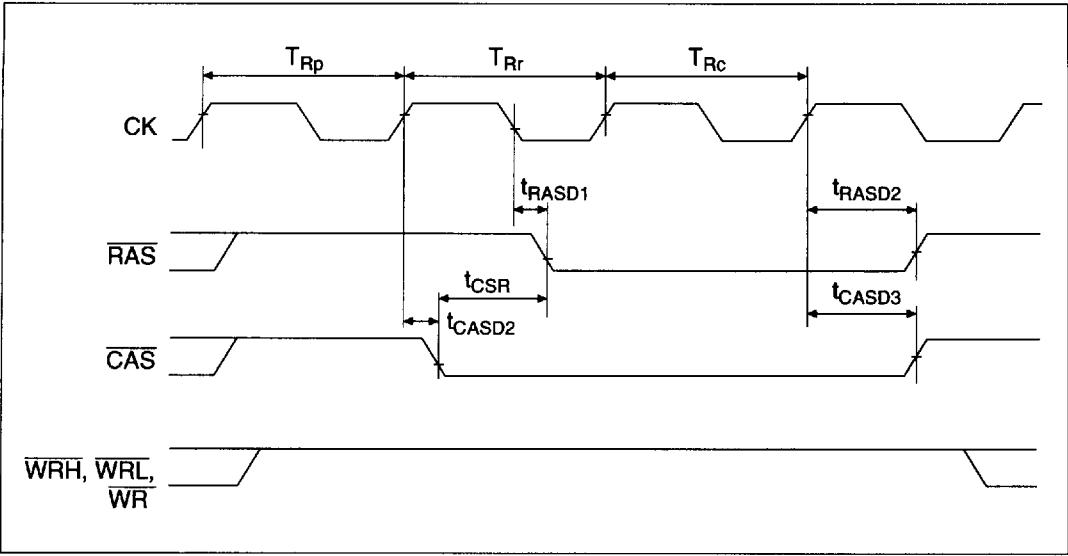


Figure 20.16 CAS-before-RAS Refresh (Short Pitch)

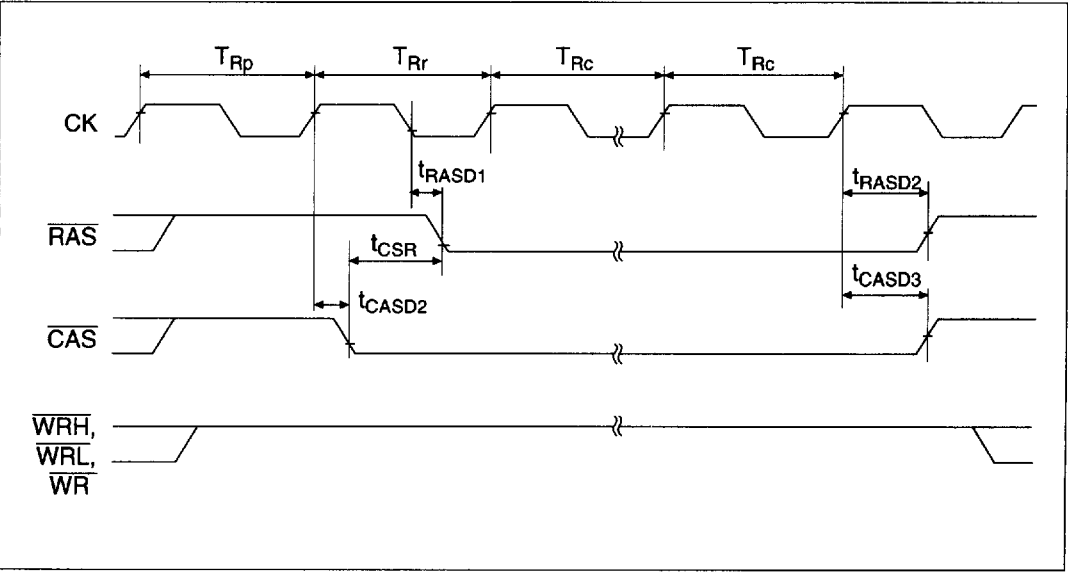


Figure 20.17 CAS-before-RAS Refresh (Long Pitch)

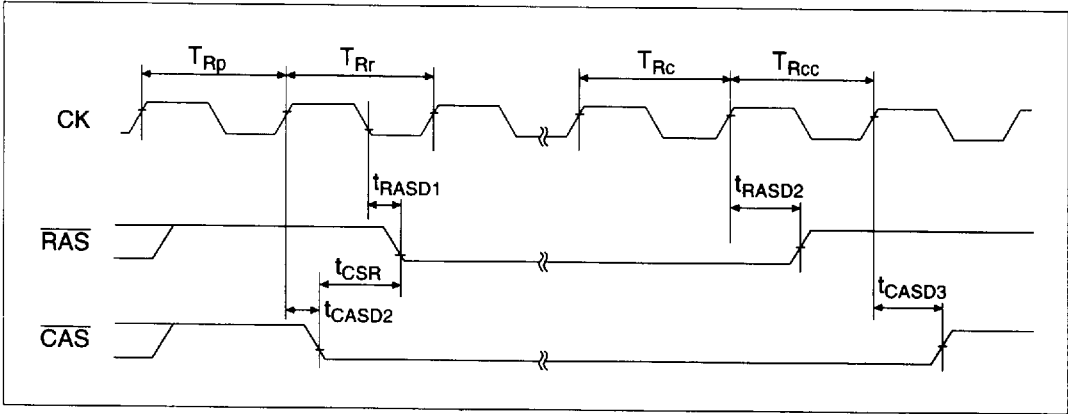


Figure 20.18 Self Refresh

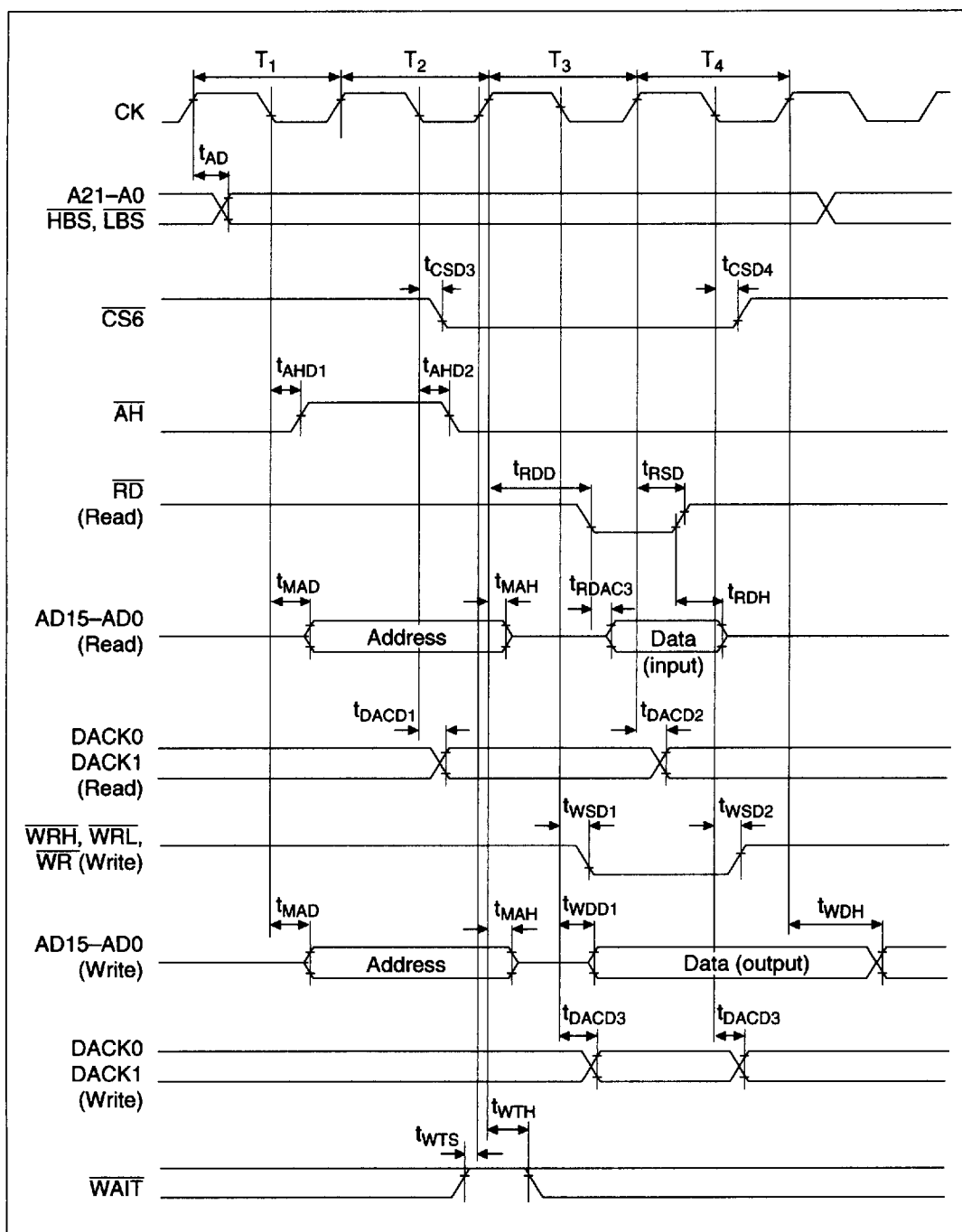


Figure 20.19 Address/Data Multiplex I/O Bus Cycle

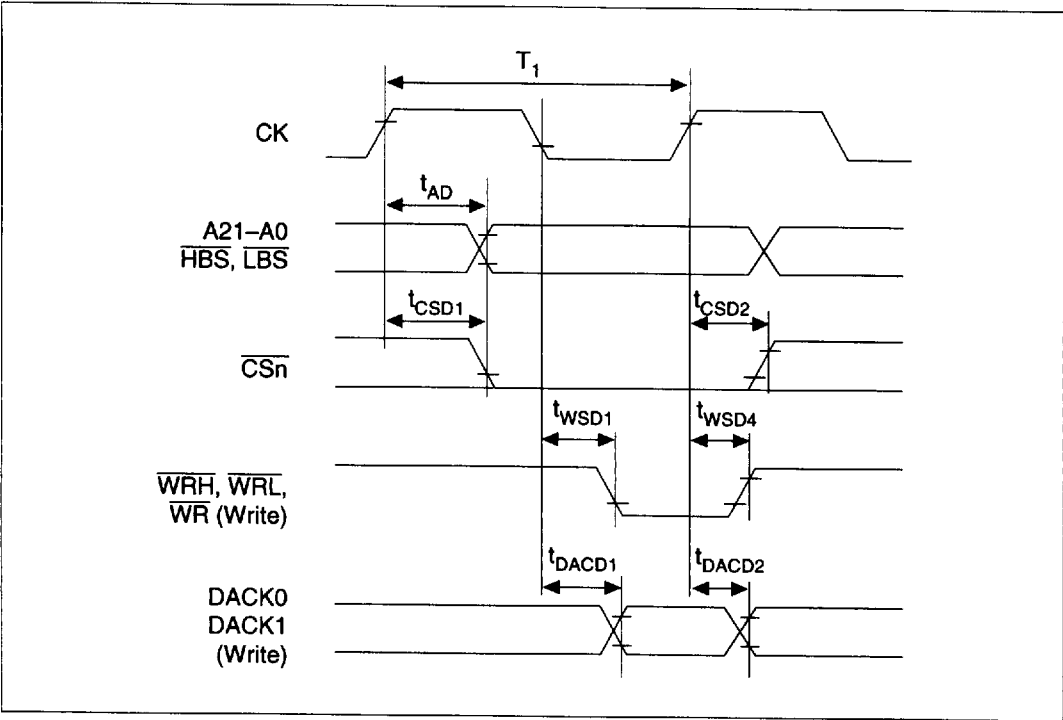


Figure 20.20 DMA Single Transfer/1 State Access Write

Table 20.8 Bus Timing (3)

Conditions: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Address delay time	t_{AD}	—	40	ns	20.21, 20.22, 20.24–20.27, 20.32, 20.33
$\overline{CS}$ delay time 1	t_{CSD1}	—	40	ns	20.21, 20.22, 20.33
$\overline{CS}$ delay time 2	t_{CSD2}	—	40	ns	
$\overline{CS}$ delay time 3	t_{CSD3}	—	40	ns	20.32
$\overline{CS}$ delay time 4	t_{CSD4}	—	40	ns	
Access time 1 from read strobe	35% duty*1 50% duty t_{RDAC1}	$t_{cyc} \times 0.65 - 35$ $t_{cyc} \times 0.5 - 35$	—	ns	20.21,
			—	ns	
Access time 2 from read strobe	35% duty*1 50% duty t_{RDAC2}	$t_{cyc} \times (n+1.65) - 35^{*2}$ $t_{cyc} \times (n+1.5) - 35^{*2}$	—	ns	20.22, 20.23
			—	ns	
Access time 3 from read strobe	35% duty*1 50% duty t_{RDAC3}	$t_{cyc} \times (n+0.65) - 35^{*2}$ $t_{cyc} \times (n+0.5) - 35^{*2}$	—	ns	20.32
			—	ns	
Read strobe delay time	t_{RSD}	—	40	ns	20.21, 20.22, 20.32
Read data set-up time	t_{RDS}	25	—	ns	20.21, 20.22,
Read data hold time	t_{RDH}	0	—	ns	20.24–20.27, 20.32
Write strobe delay time 1	t_{WSD1}	—	40	ns	20.22, 20.26, 20.27, 20.32, 20.33
Write strobe delay time 2	t_{WSD2}	—	30	ns	20.22, 20.26, 20.27, 20.32
Write strobe delay time 3	t_{WSD3}	—	40	ns	20.24, 20.25
Write strobe delay time 4	t_{WSD4}	—	40	ns	20.24, 20.25, 20.33
Write data delay time 1	t_{WDD1}	—	70	ns	20.22, 20.26, 20.27, 20.32
Write data delay time 2	t_{WDD2}	—	40	ns	20.24, 20.26
Write data hold time	t_{WDH}	–10	—	ns	20.22, 20.24–20.27, 20.32
Parity output delay time 1	t_{WPDD1}	—	80	ns	20.22, 20.24, 20.27
Parity output delay time 2	t_{WPDD2}	—	40	ns	20.24, 20.25
Parity output hold time	t_{WPDH}	–10	—	ns	20.22, 20.23–20.27

Table 20.8 Bus Timing (3) (cont)

Conditions: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Min	Max	Unit	Figures
Wait setup time	t_{WTS}	40	—	ns	20.23, 20.28, 20.32
Wait hold time	t_{WTH}	10	—	ns	
Read data access time 1	t_{ACC1}	$t_{cyc} - 44$	—	ns	20.21, 20.24, 20.25
Read data access time 2	t_{ACC2}	$t_{cyc} \times (n+2) - 44^{*2}$	—	ns	20.22, 20.23, 20.26, 20.28
RAS delay time 1	t_{RASD1}	—	40	ns	20.24–20.27, 20.29–
RAS delay time 2	t_{RASD2}	—	40	ns	20.31
CAS delay time 1	t_{CASD1}	—	40	ns	20.24
CAS delay time 2	t_{CASD2}	—	40	ns	20.26, 20.27, 20.29–
CAS delay time 3	t_{CASD3}	—	40	ns	20.31
Column address setup time	t_{ASC}	0	—	ns	20.24, 20.25
Read data access time from CAS 1	t_{CAC1}	35% duty ^{*1}	$t_{cyc} \times 0.65 - 35$	—	ns
		50% duty	$t_{cyc} \times 0.5 - 35$	—	ns
Read data access time from CAS 2	t_{CAC2}	$t_{cyc} \times (n+1) - 35^{*2}$	—	ns	20.26, 20.27, 20.28
Read data access time from RAS 1	t_{RAC1}	$t_{cyc} \times 1.5 - 35$	—	ns	20.24, 20.25
Read data access time from RAS 2	t_{RAC2}	$t_{cyc} \times (n+2.5) - 35^{*2}$	—	ns	20.26, 20.27, 20.28
High-speed page mode CAS precharge time	t_{CP}	$t_{cyc} \times 0.25$	—	ns	20.25
AH delay time 1	t_{AHD1}	—	40	ns	20.32
AH delay time 2	t_{AHD2}	—	40	ns	
Multiplexed address delay time	t_{MAD}	—	40	ns	
Multiplexed address hold time	t_{MAH}	–10	—	ns	

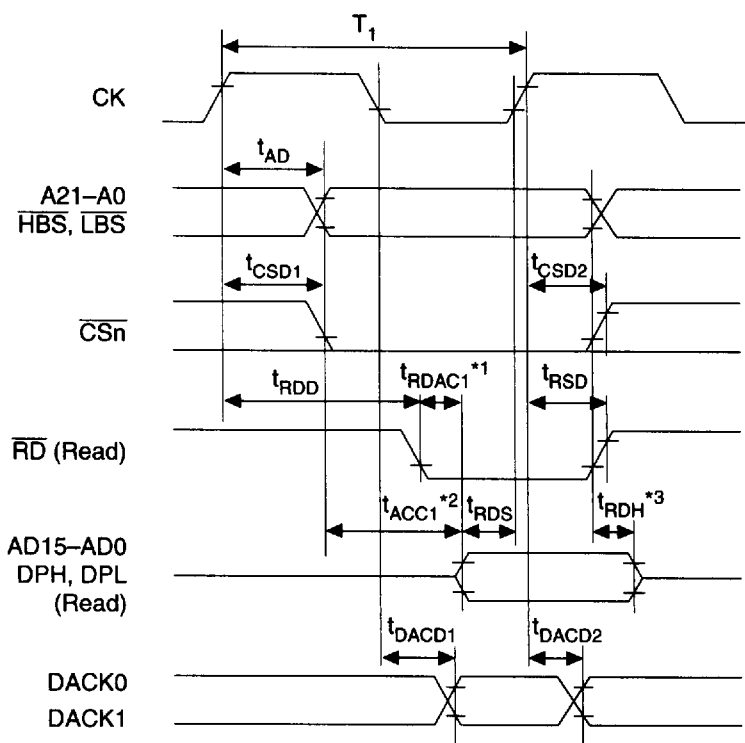
Table 20.8 Bus Timing (3) (cont)

Conditions: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $V_{CC} = AV_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^{\circ}\text{C}^*$

Normal Products: $T_a = -40$ to $+85^{\circ}\text{C}$ for wide-temperature range products

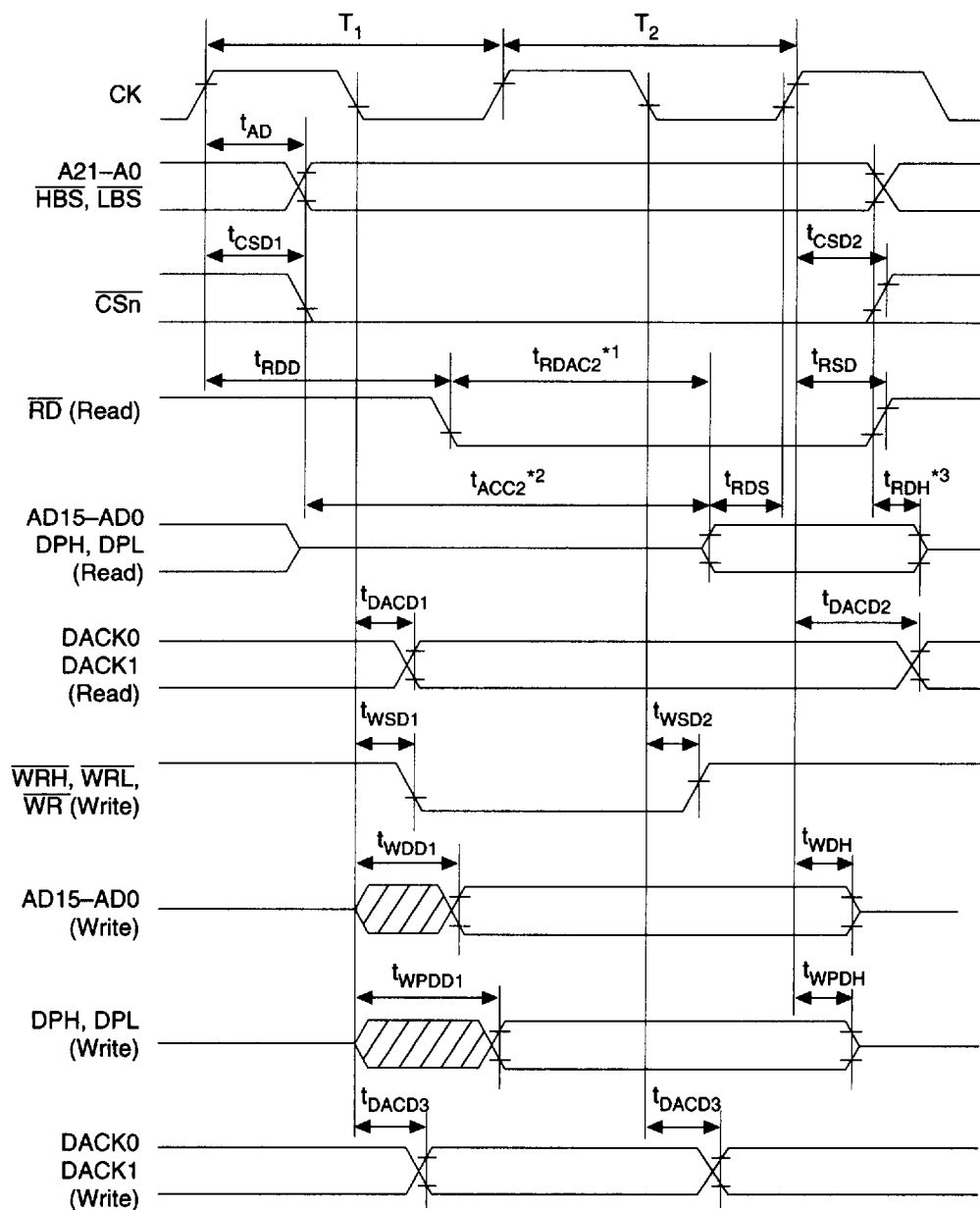
Item	Symbol	Min	Max	Unit	Figures
DACK0, DACK1 delay time 1	t_{DACD1}	—	40	ns	20.21, 20.22, 20.24–
DACK0, DACK1 delay time 2	t_{DACD2}	—	40	ns	20.27, 20.32, 20.33
DACK0, DACK1 delay time 3	t_{DACD3}	—	40	ns	20.22, 20.26, 20.27, 20.32
DACK0, DACK1 delay time 4	t_{DACD4}	—	40	ns	20.24, 20.25
DACK0, DACK1 delay time 5	t_{DACD5}	—	40	ns	
Read delay time	35% duty ^{*1} t_{RDD}	—	$t_{cyc} \times 0.35 + 35$	ns	20.21, 20.22, 20.24–
		—	$t_{cyc} \times 0.5 + 35$	ns	20.28, 20.32
Data setup time for $\overline{CAS}$	t_{DS}	0 ^{*3}	—	ns	20.24, 20.26
$\overline{CAS}$ setup time for $\overline{RAS}$	t_{CSR}	10	—	ns	20.29–20.31
Row address hold time	t_{RAH}	10	—	ns	20.24, 20.26
Write command hold time	t_{WCH}	15	—	ns	
Write command setup time	35% duty ^{*1} t_{WCS}	0	—	ns	20.24
	50% duty t_{WCS}	0	—	ns	
Access time from $\overline{CAS}$ precharge	t_{ACP}	t_{cyc} –20	—	ns	20.25

- Notes: 1. When frequency is 10 MHz or more.
2. n is the number of wait cycles.
3. –5 ns for parity output of DRAM long-pitch access



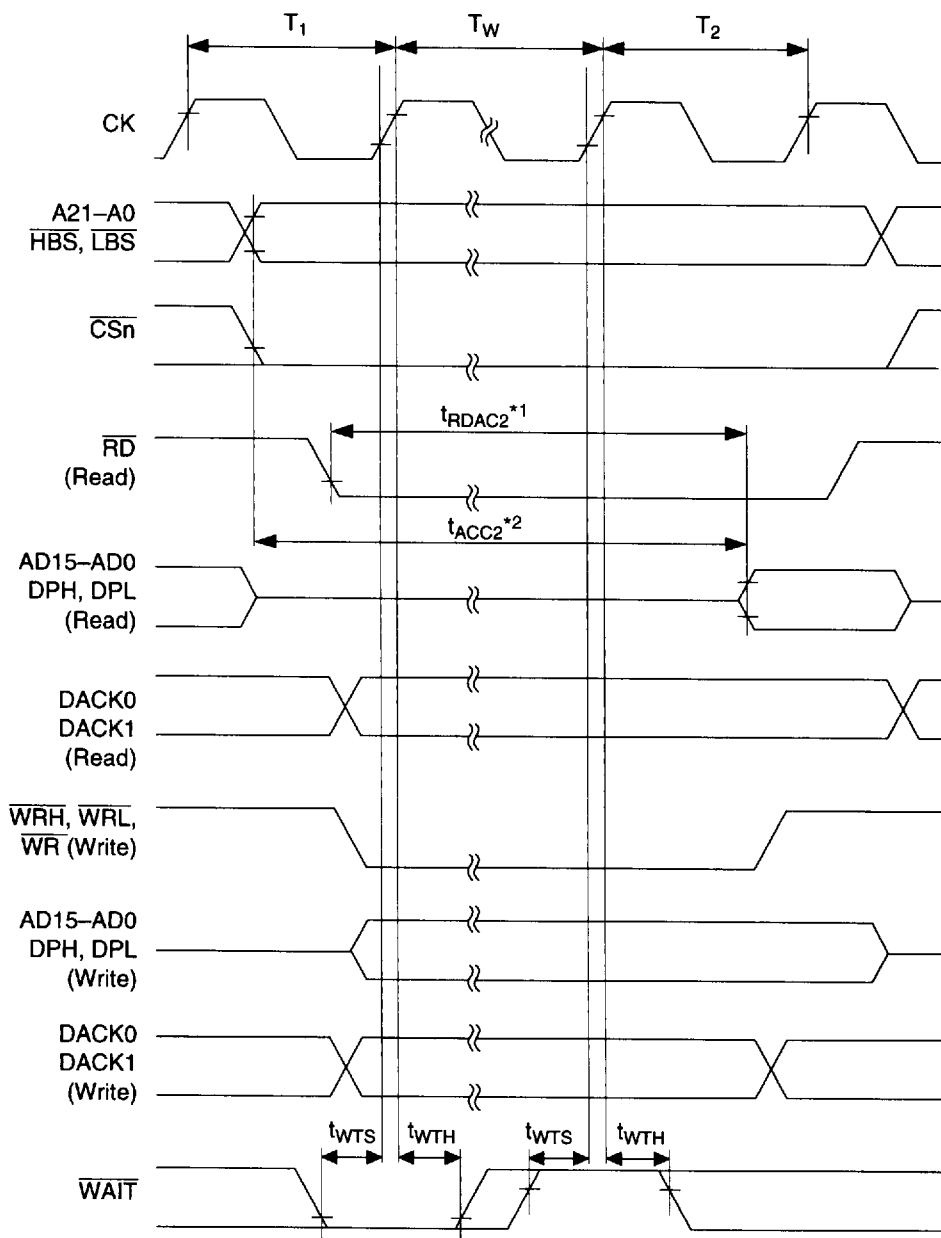
- Notes:
1. For t_{RDAC1} , use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{RDD} - t_{RDS}$.
 2. For t_{ACC1} , use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD}$ (or t_{CSD1}) - t_{RDS} .
 3. t_{RDH} is measured from A21-A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.21 Basic Bus Cycle: One-State Access



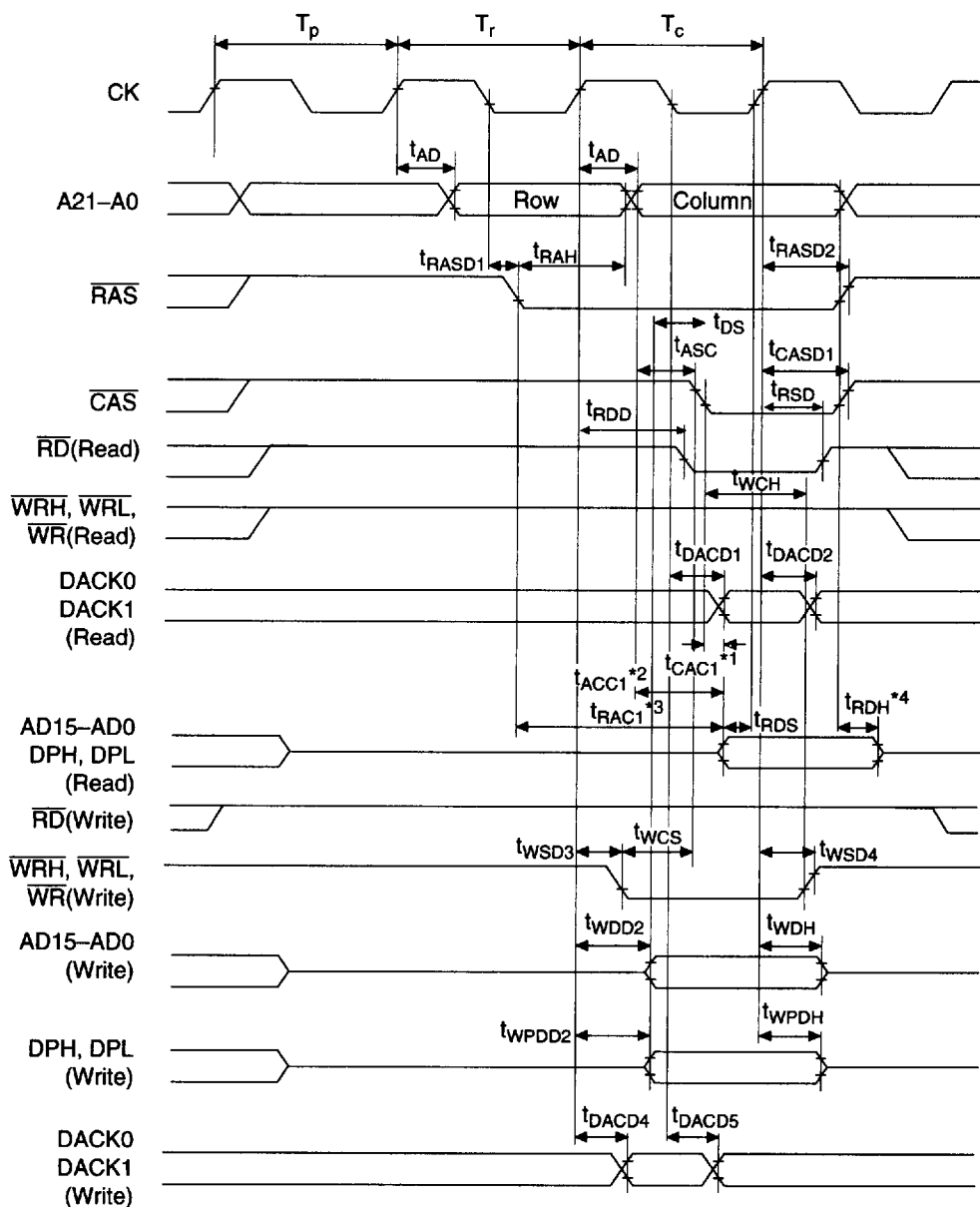
- Notes: 1. For t_{RDAC2} , use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) - t_{RDS} .
3. t_{RDH} is measured from A21-A0, $\overline{CSn}$, or $\overline{RD}$, whichever is negated first.

Figure 20.22 Basic Bus Cycle: Two-State Access



- Notes: 1. For t_{RDAC2} , use $t_{cyc} \times (n + 1.65) - 35$ (for 35% duty) or $t_{cyc} \times (n + 1.5) - 35$ (for 50% duty) instead of $t_{cyc} \times (n + 2) - t_{RDD} - t_{RDS}$.
2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD}$ (or t_{CSD1}) - t_{RDS} .

Figure 20.23 Basic Bus Cycle: Two States + Wait State



- Notes:
1. For t_{CAC1} , use $t_{cyc} \times 0.65 - 35$ (for 35% duty) or $t_{cyc} \times 0.5 - 35$ (for 50% duty) instead of $t_{cyc} - t_{AD} - t_{ASC} - t_{RDS}$.
 2. For t_{ACC1} , use $t_{cyc} - 44$ instead of $t_{cyc} - t_{AD} - t_{RDS}$.
 3. For t_{RAC1} , use $t_{cyc} \times 1.5 - 35$ instead of $t_{cyc} \times 1.5 - t_{RASD1} - t_{RDS}$.
 4. t_{RDH} is measured from A21-A0, RAS, or CAS, whichever is negated first.

Figure 20.24 DRAM Bus Cycle (Short Pitch, Normal Mode)

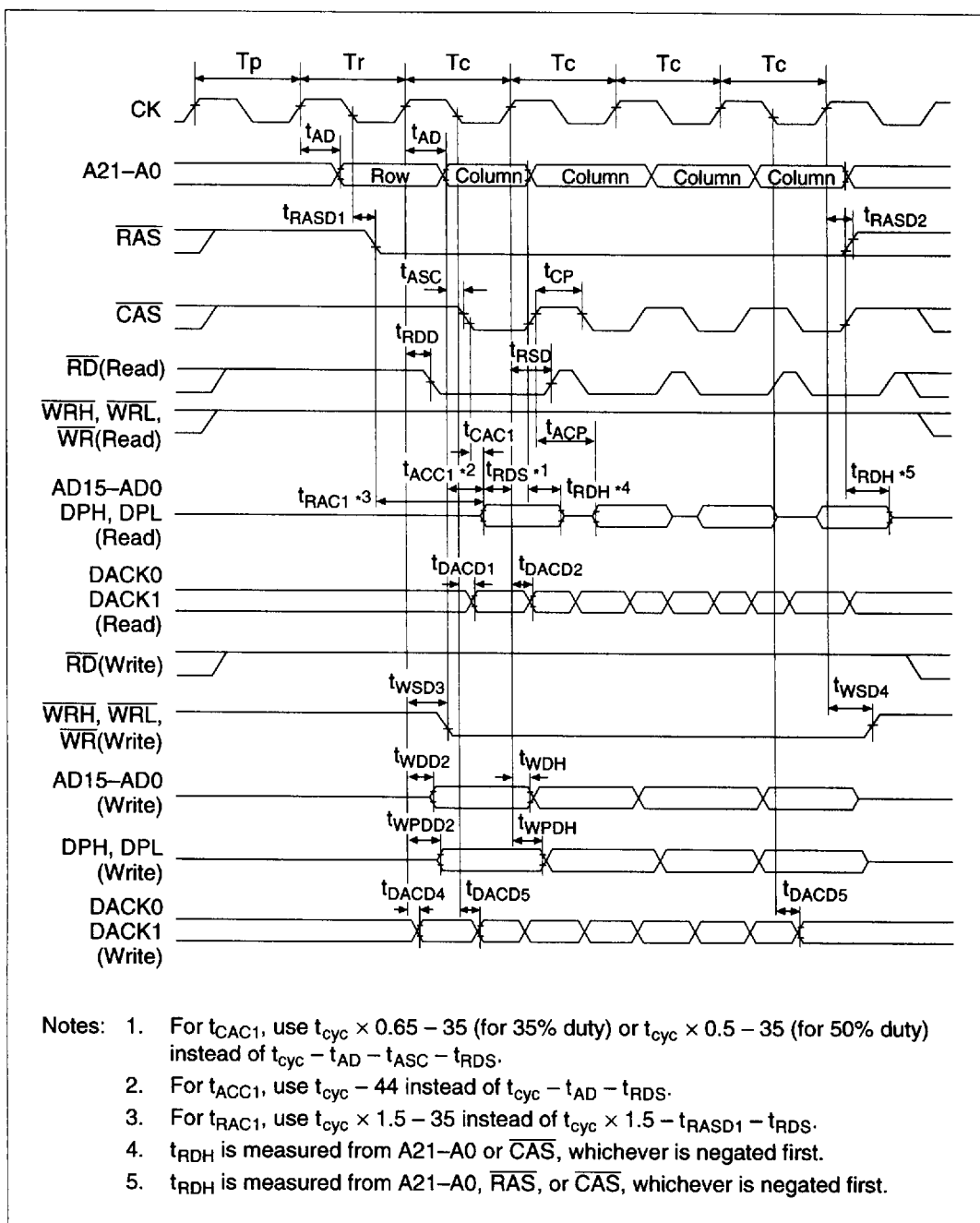
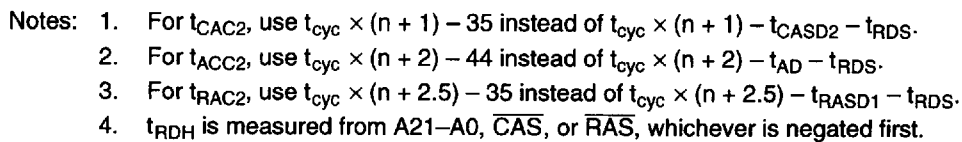
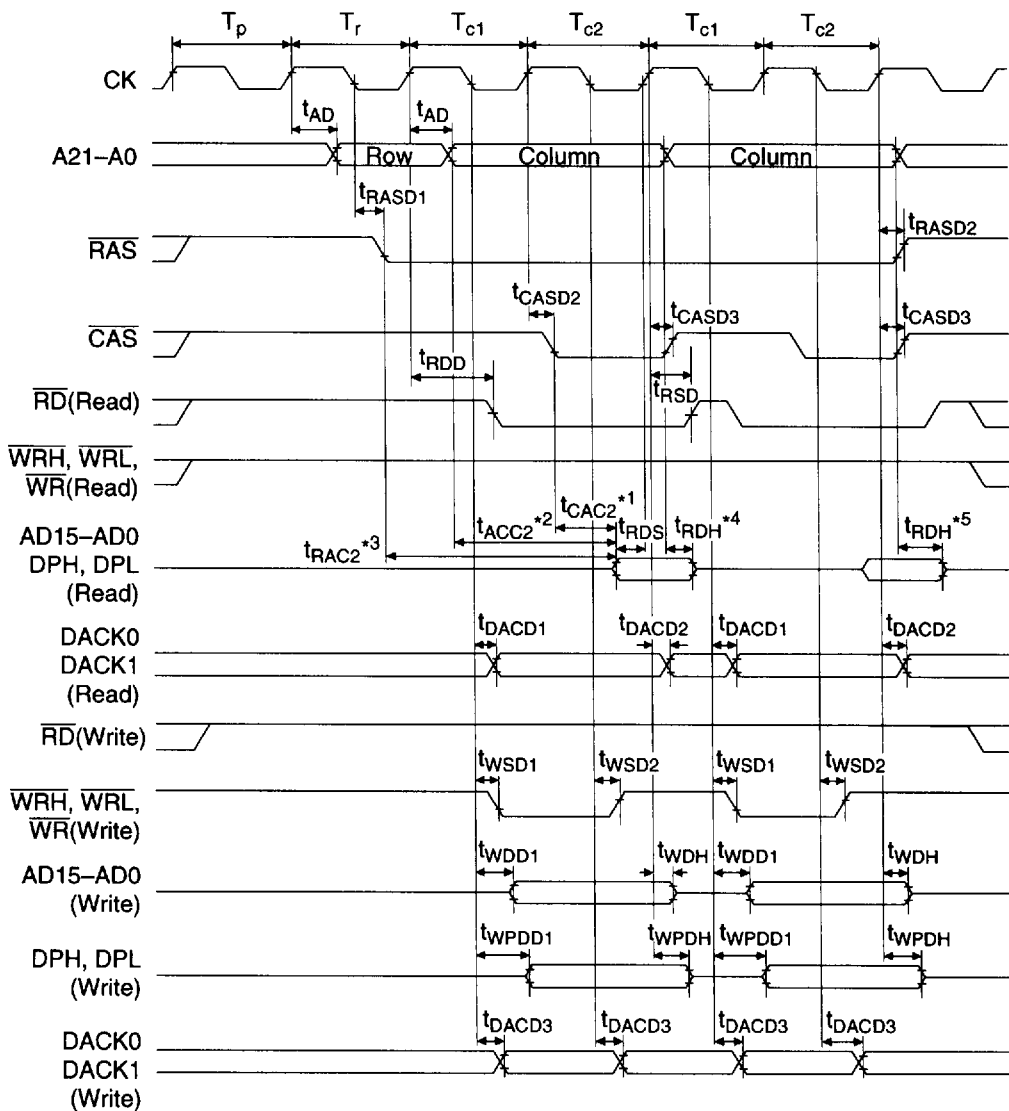


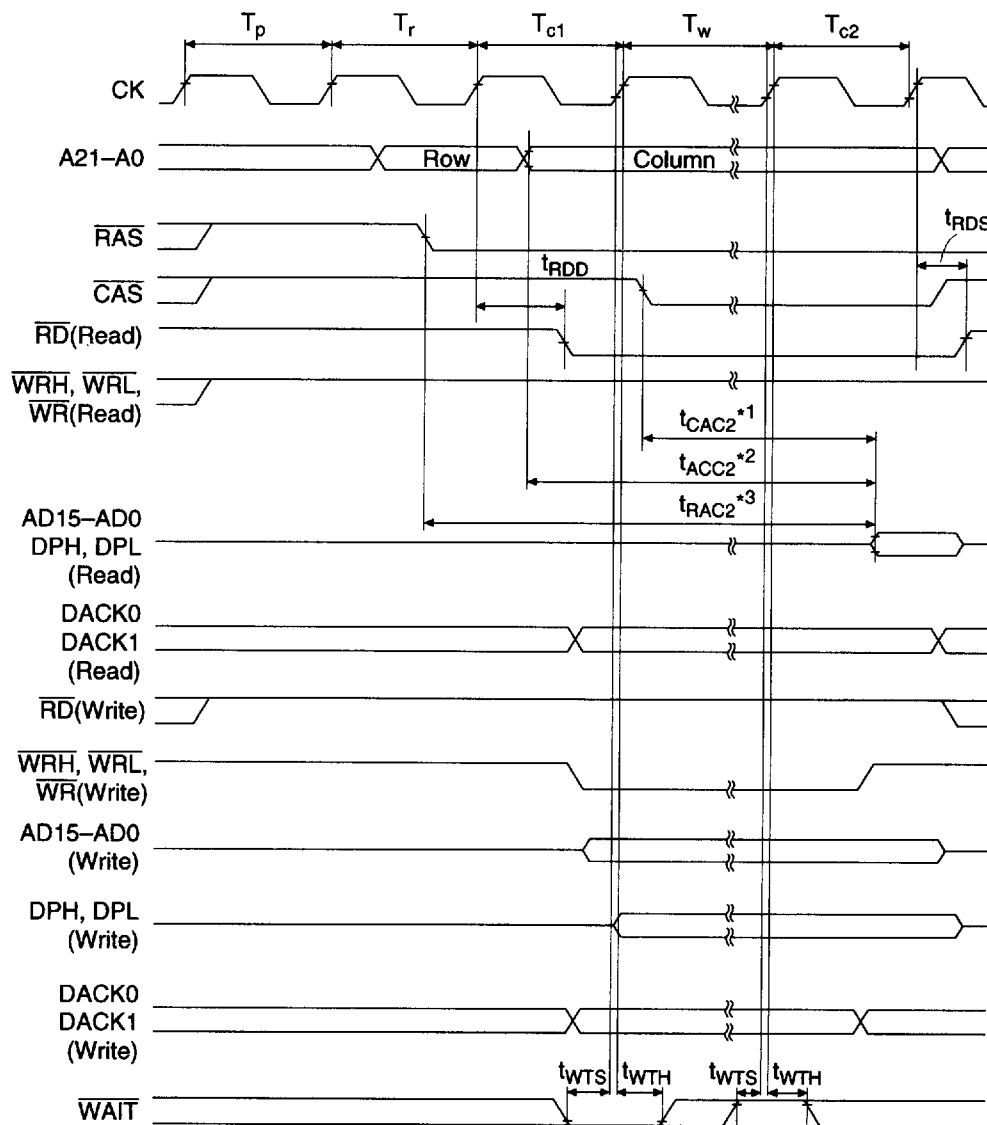
Figure 20.25 DRAM Bus Cycle (Short Pitch, High-Speed Page Mode)





- Notes:
1. For t_{CAC2} , use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
 2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
 3. For t_{RAC2} , use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.
 4. t_{RDH} is measured from A21-A0 or $\overline{CAS}$, whichever is negated first.
 5. t_{RDH} is measured from A21-A0, $\overline{RAS}$, or $\overline{CAS}$ whichever is negated first.

Figure 20.27 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode)



- Notes:
1. For t_{CAC2} , use $t_{cyc} \times (n + 1) - 35$ instead of $t_{cyc} \times (n + 1) - t_{CASD2} - t_{RDS}$.
 2. For t_{ACC2} , use $t_{cyc} \times (n + 2) - 44$ instead of $t_{cyc} \times (n + 2) - t_{AD} - t_{RDS}$.
 3. For t_{RAC2} , use $t_{cyc} \times (n + 2.5) - 35$ instead of $t_{cyc} \times (n + 2.5) - t_{RASD1} - t_{RDS}$.

Figure 20.28 DRAM Bus Cycle: (Long Pitch, High-Speed Page Mode + Wait State)

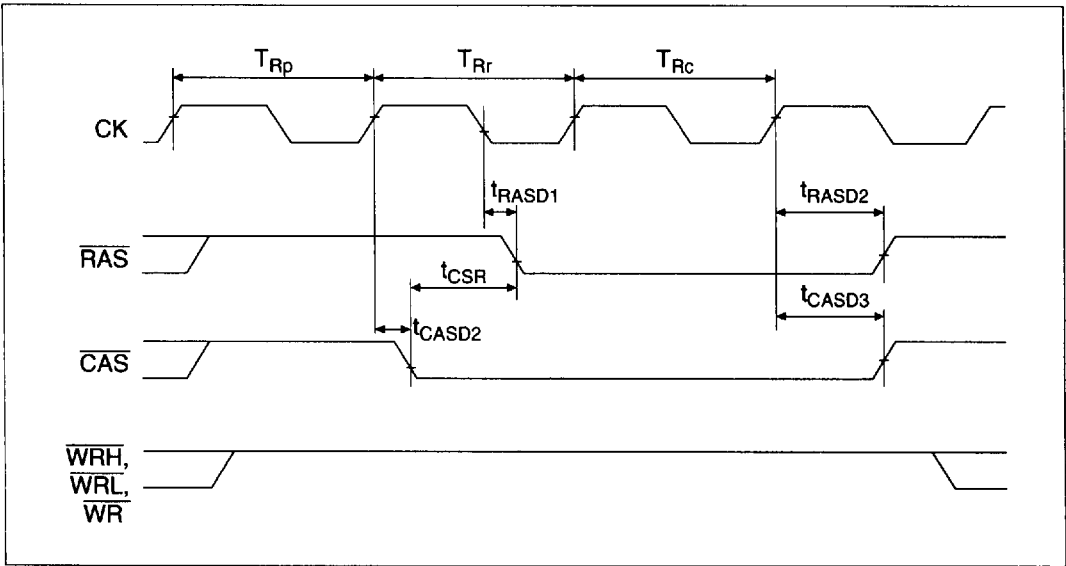


Figure 20.29 CAS-before-RAS Refresh (Short Pitch)

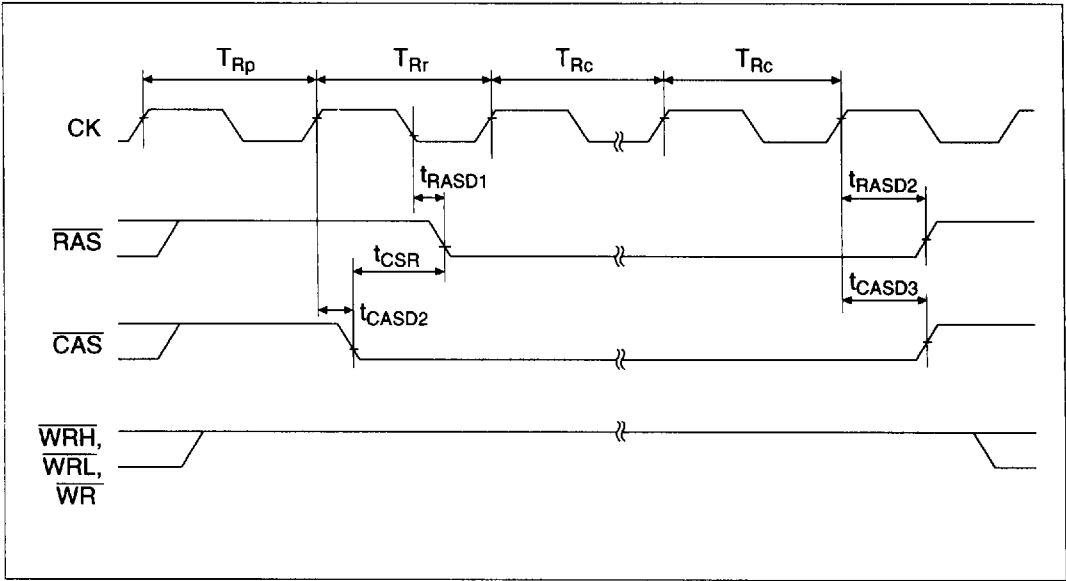


Figure 20.30 CAS-before-RAS Refresh (Long Pitch)

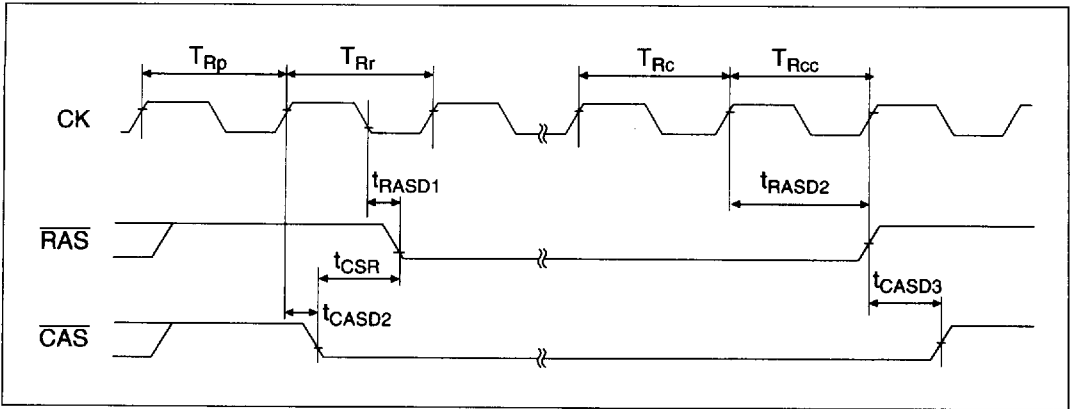


Figure 20.31 Self Refresh

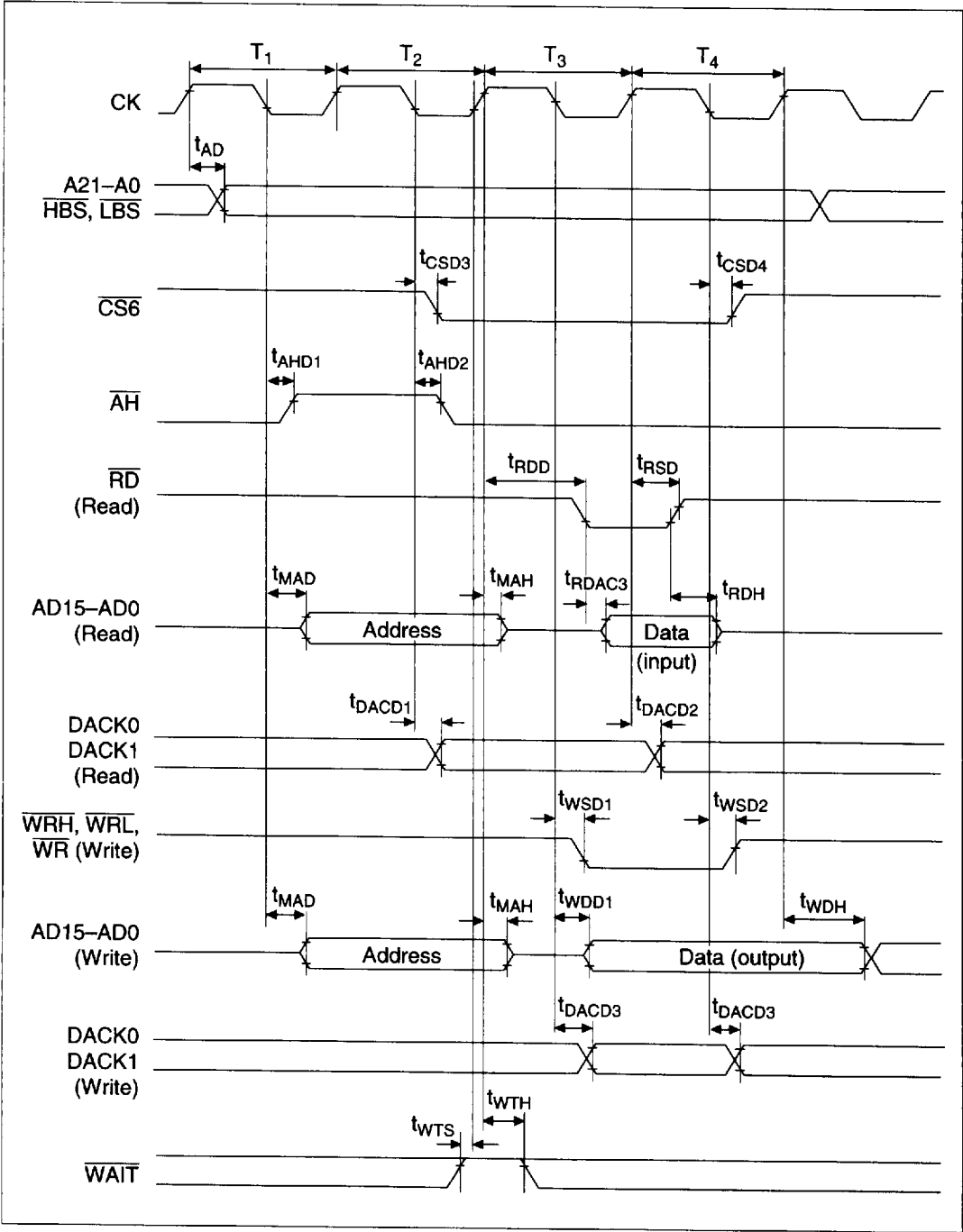


Figure 20.32 Address/Data Multiplex I/O Bus Cycle

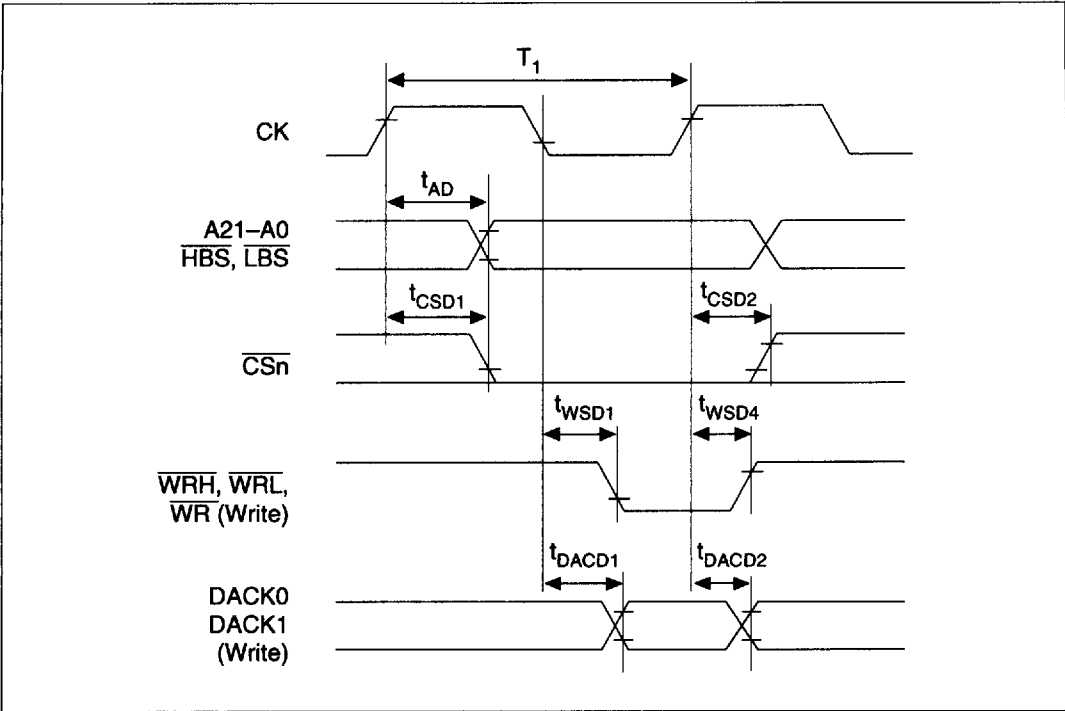


Figure 20.33 DMA Single Transfer/Single State Access Write

20.3.4 DMAC Timing

Table 20.9 DMAC Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Case A		Case B			Unit	Figure
		12.5 MHz		16.6 MHz		20 MHz		
		Min	Max	Min	Max	Min	Max	
DREQ0, DREQ1 setup time	t_{DRQS}	80	—	40	—	27	—	ns 20.34
DREQ0, DREQ1 hold time	t_{DRQH}	30	—	30	—	30	—	ns
DREQ0, DREQ1 low level width	t_{DRQW}	1.5	—	1.5	—	1.5	—	t_{cyc} 20.35

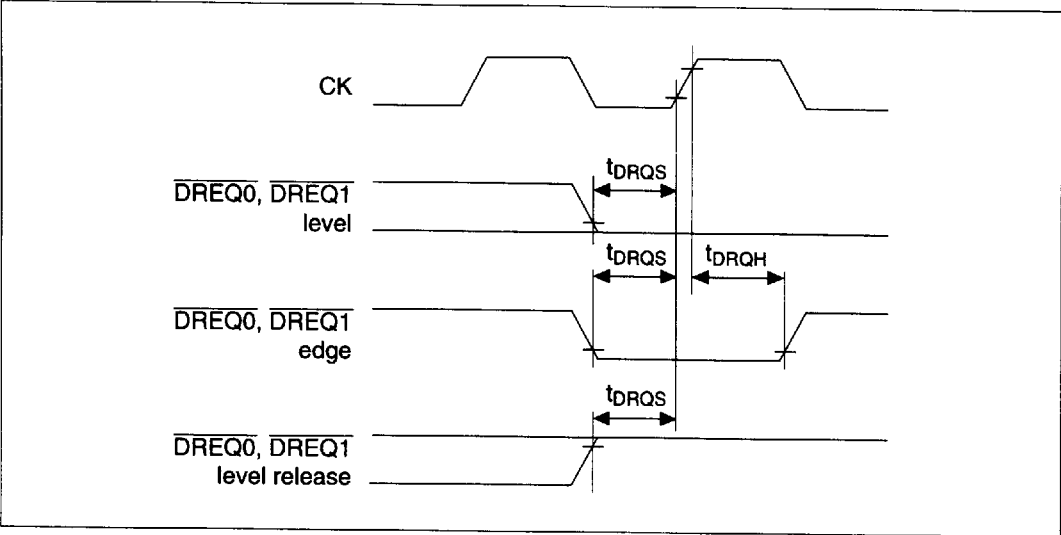


Figure 20.34 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (1)

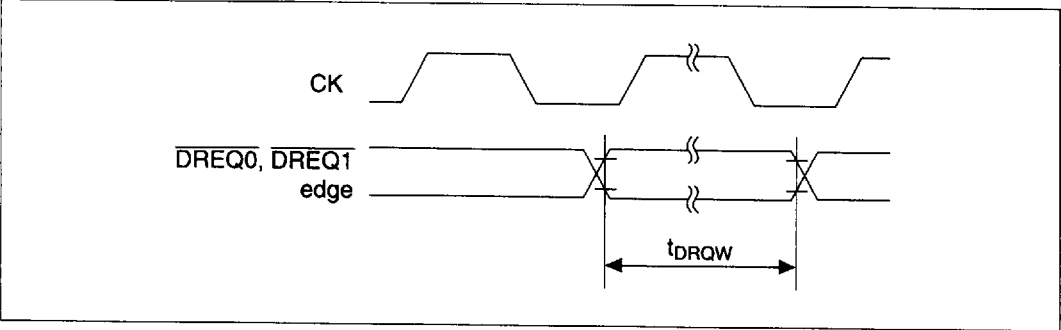


Figure 20.35 $\overline{\text{DREQ0}}$, $\overline{\text{DREQ1}}$ Input Timing (2)

20.3.5 16-bit Integrated Timer Pulse Unit Timing

Table 20.10 16-bit Integrated Timer Pulse Unit Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^{\circ}\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $T_a = -20$ to $+75^{\circ}\text{C}^*$

Normal Products: $T_a = -40$ to $+85^{\circ}\text{C}$ for wide-temperature range products.

Item	Symbol	Case A		Case B					Figure
		12.5 MHz		16.6 MHz		20 MHz			
		Min	Max	Min	Max	Min	Max	Unit	
Output compare delay time	t _{TOCD}	—	100	—	100	—	100	ns	20.36
Input capture setup time	t _{TICS}	50	—	45	—	35	—	ns	
Timer clock input setup time	t _{TCKS}	50	—	50	—	50	—	ns	20.37
Timer clock pulse width (single edge)	t _{TCKWH/L}	1.5	—	1.5	—	1.5	—	t _{cyc}	
Timer clock pulse width (both edges)	t _{TCKWL/L}	2.5	—	2.5	—	2.5	—	t _{cyc}	

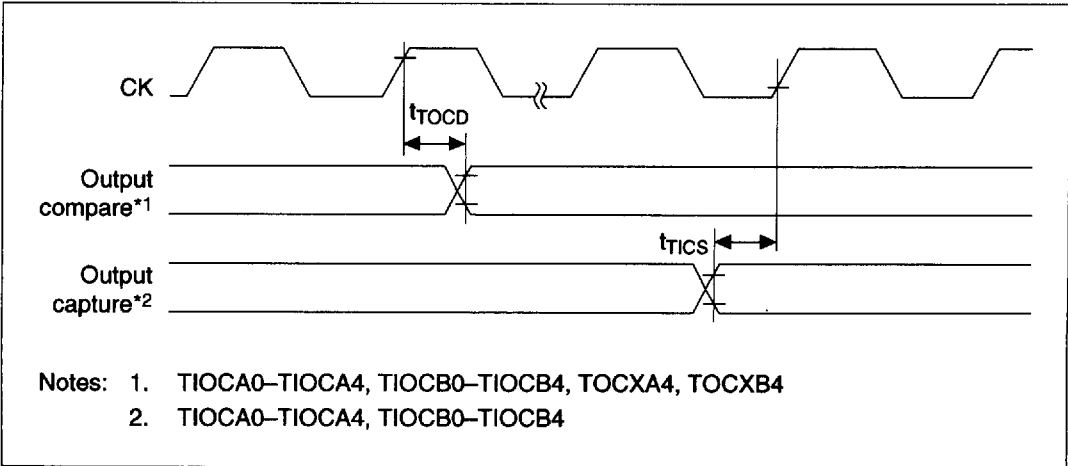


Figure 20.36 ITU Input/Output Timing

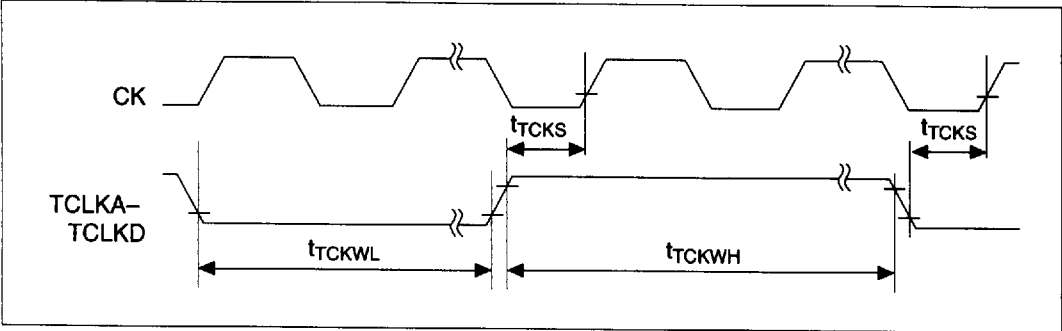


Figure 20.37 ITU Clock Input Timing

20.3.6 Programmable Timing Pattern Controller and I/O Port Timing

Table 20.11 Programmable Timing Pattern Controller and I/O Port Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 16.6$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case C: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 20$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Cases A, B and C			Figure
		Min	Max	Unit	
Port output delay time	t_{PWD}	—	100	ns	20.38
Port input hold time	t_{PRH}	50	—	ns	
Port input setup time	t_{PRS}	50	—	ns	

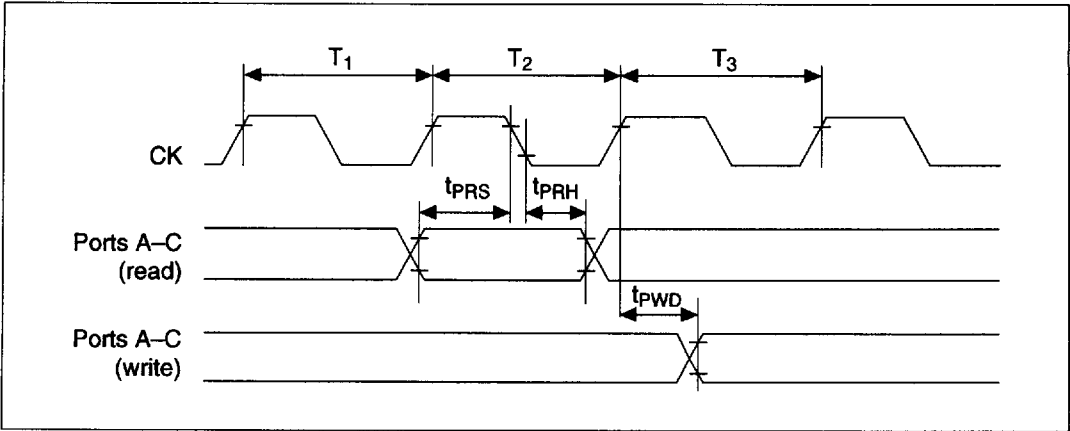


Figure 20.38 Programmable Timing Pattern Controller Output Timing

20.3.7 Watchdog Timer Timing

Table 20.12 Watchdog Timer Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 16.6$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case C: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 20$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Cases A, B and C		Unit	Figure
		Min	Max		
WDTOVF delay time	t_{WOVD}	—	100	ns	20.39

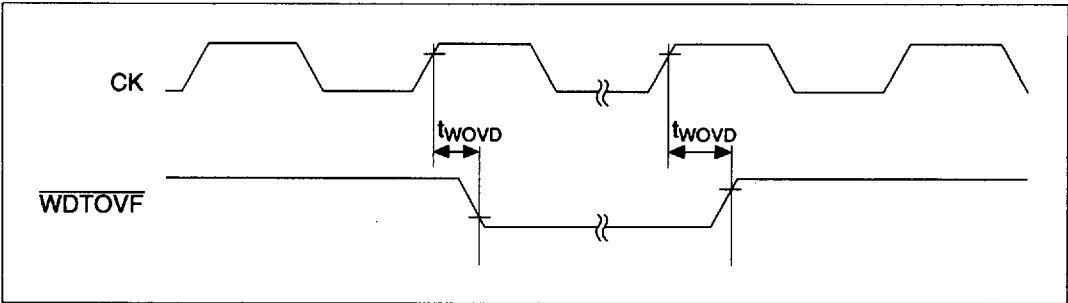


Figure 20.39 Watchdog Timer Output Timing

20.3.8 Serial Communications Interface Timing

Table 20.13 Serial Communications Interface Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 16.6$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case C: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $f = 20$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Cases A, B and C		Unit	Figure
		Min	Max		
Input clock cycle	t_{scyc}	4	—	t_{cyc}	20.40
Input clock cycle (clocked synchronization)	t_{scyc}	6	—	t_{cyc}	
Input clock pulse width	t_{sckw}	0.4	0.6	t_{scyc}	
Input clock rise time	t_{sckr}	—	1.5	t_{cyc}	
Input clock fall time	t_{sckf}	—	1.5	t_{cyc}	
Transmission data delay time (clocked synchronization)	t_{TXD}	—	100	ns	20.41
Receive data setup time (clocked synchronization)	t_{RXS}	100	—	ns	
Receive data hold time (clocked synchronization)	t_{RXH}	100	—	ns	

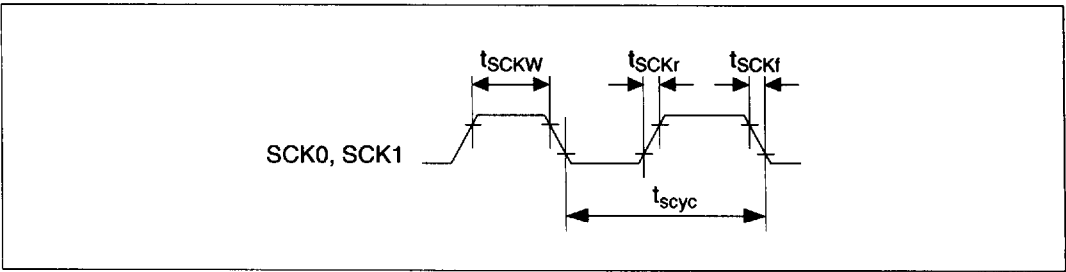


Figure 20.40 Input Clock Timing

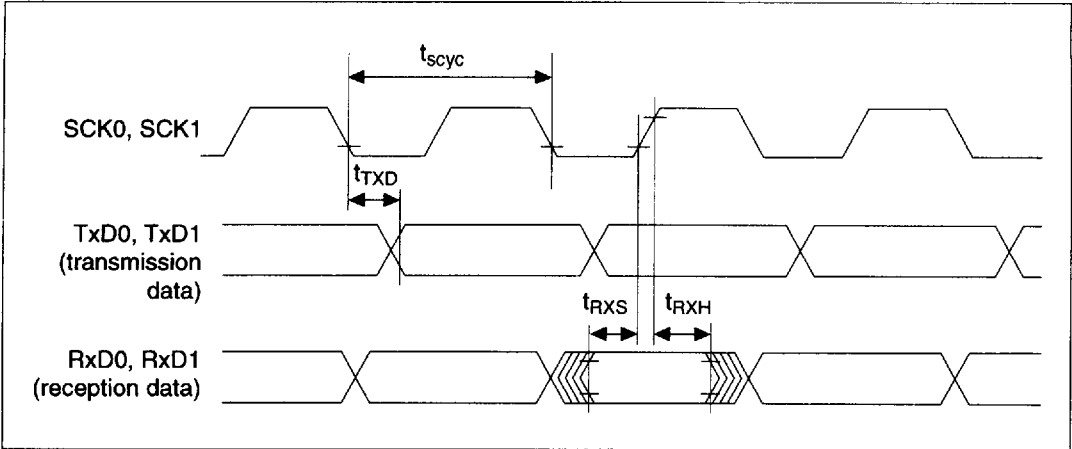


Figure 20.41 SCI I/O Timing (Clocked Synchronization Mode)

20.3.9 A/D Converter Timing

Table 20.14 A/D Converter Timing

Case A: $V_{CC} = 3.0$ to 5.5 V, $AV_{CC} = 3.0$ to 5.5 V, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 12.5$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case B: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 16.6$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Case C: $V_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = 5.0$ V $\pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5$ V to AV_{CC} , $V_{SS} = AV_{SS} = 0$ V, $\phi = 20$ MHz, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	Symbol	Cases A, B and C		Unit	Figure
		Min	Max		
External trigger input start delay time	t_{TRGS}	50	—	ns	20.42
A/D converter time (266 cycles)	t_{CONV}	—	266	t_{cyc}	20.43
A/D converter time (134 cycles)	t_{CONV}	—	134	t_{cyc}	
$\overline{ADTRG}$ pulse width	t_{TRGW}	2.0	—	t_{cyc}	20.42

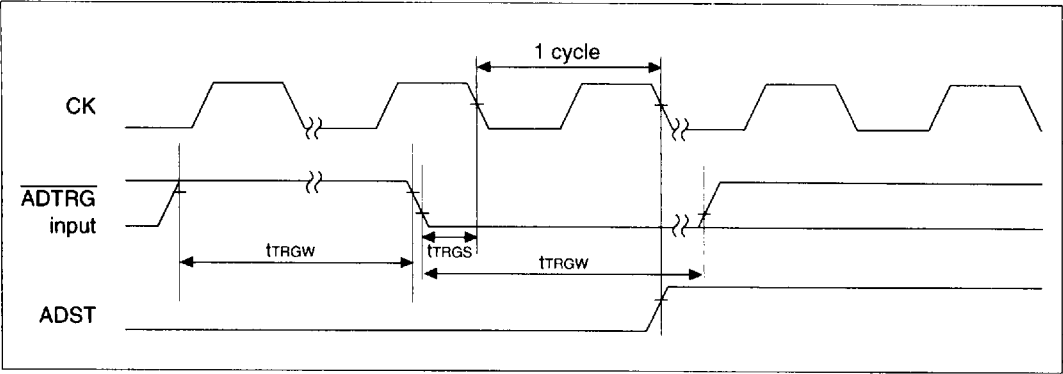


Figure 20.42 External Trigger Input Timing

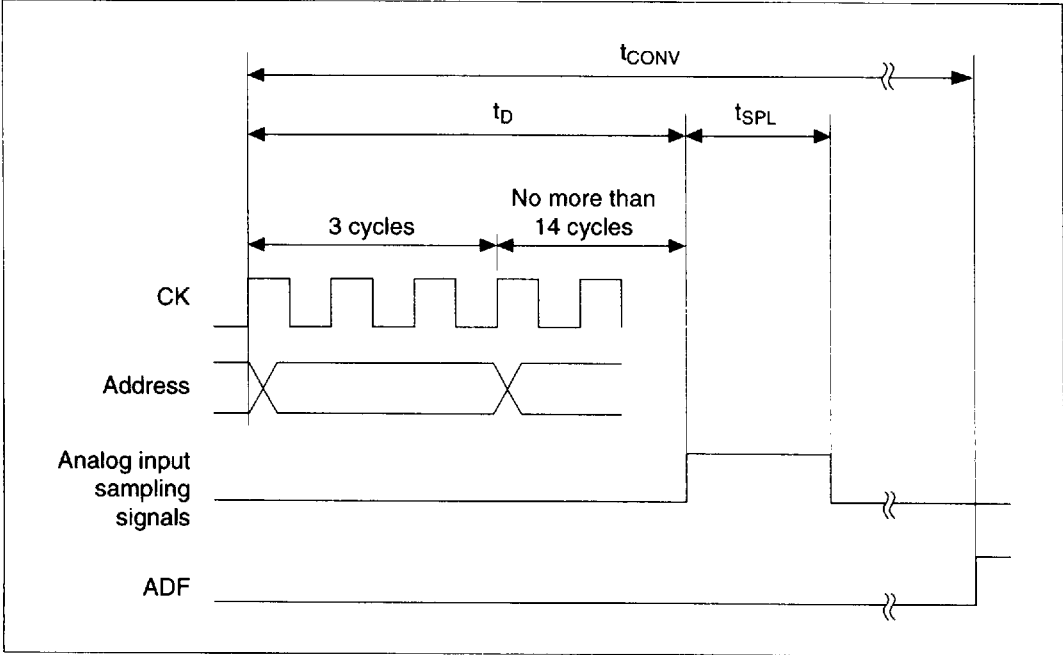
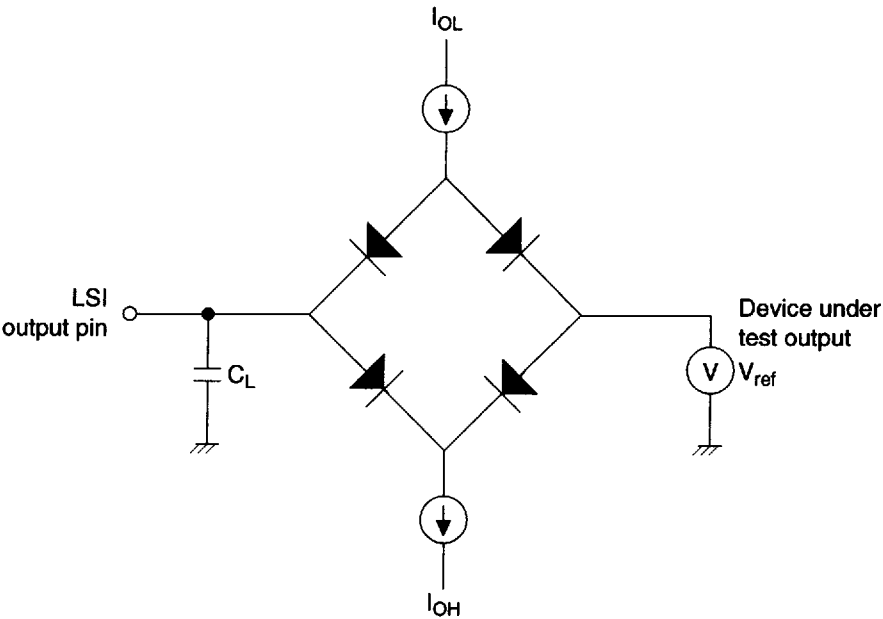


Figure 20.43 Analog Conversion Timing

20.3.10 AC Characteristics Measurement Conditions



C_L is set as follows for each pin.
30pF: CK, $\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{CS0}}\text{--}\overline{\text{CS7}}$, $\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, $\overline{\text{AH}}$, $\overline{\text{LRQOUT}}$, $\overline{\text{RAS}}$, $\overline{\text{DACK0}}$, $\overline{\text{DACK1}}$
50pF: A21–A0, AD15–AD0, DPH, DPL, $\overline{\text{RD}}$, $\overline{\text{WRH}}$, $\overline{\text{WRL}}$, $\overline{\text{HBS}}$, $\overline{\text{LBS}}$, $\overline{\text{WR}}$
70pF: All port outputs and peripheral module output pins other than the above.
 I_{OL} and I_{OH} values are as shown in section 20.2, DC Characteristics, and table 20.3, Permitted Output Current Values.

Figure 20.44 Output Load Circuit

20.4 A/D Converter Characteristics

Table 20.15 A/D Converter Characteristics (1)

Conditions: $V_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = 5.0\text{ V} \pm 10\%$, $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 4.5\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	12.5 MHz			16.6 MHz			20 MHz			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution	10	10	10	10	10	10	10	10	10	bit
Conversion time	—	—	11.2	—	—	8.4	—	—	6.7	μS
Analog input capacitance	—	—	20	—	—	20	—	—	20	pF
Permissible signal-source impedance	—	—	3	—	—	3	—	—	3	$\text{k}\Omega$
Nonlinearity error	—	—	± 3	—	—	± 3	—	—	± 3	LSB
Offset error	—	—	± 3	—	—	± 3	—	—	± 3	LSB
Full-scale error	—	—	± 3	—	—	± 3	—	—	± 3	LSB
Quantization error	—	—	± 0.5	—	—	± 0.5	—	—	± 0.5	LSB
Absolute accuracy	—	—	± 4	—	—	± 4	—	—	± 4	LSB

Table 20.15 A/D Converter Characteristics (2)

Conditions: $V_{CC} = 3.0$ to 5.5 V , $AV_{CC} = 3.0$ to 5.5 V , $AV_{CC} = V_{CC} \pm 10\%$, $AV_{ref} = 3.0\text{ V}$ to AV_{CC} , $V_{SS} = AV_{SS} = 0\text{ V}$, $T_a = -20$ to $+75^\circ\text{C}^*$

Normal Products: $T_a = -40$ to $+85^\circ\text{C}$ for wide-temperature range products.

Item	12.5 MHz			Unit
	Min	Typ	Max	
Resolution	10	10	10	bit
Conversion time	—	—	11.2	μS
Analog input capacitance	—	—	20	pF
Permissible signal-source impedance	—	—	3	$\text{k}\Omega$
Nonlinearity error	—	—	± 4.0	LSB
Offset error	—	—	± 4.0	LSB
Full-scale error	—	—	± 4.0	LSB
Quantization error	—	—	± 0.5	LSB
Absolute accuracy	—	—	± 6.0	LSB

20.5 Usage Note

The ZTAT version and the mask ROM version satisfy the electrical properties given in this document. However, effective values of the electrical properties, the operating margin, and the noise margin may differ with the manufacturing processes, on-chip ROM, and layout patterns. When conducting a system evaluation test using the ZTAT version, conduct a similar evaluation test of the mask ROM version before it replaces the ZTAT version.