



Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— 20 ns
- Low active power
— 550 mW
- Low standby power
— 110 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY6116A and CY6117A are high-performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}), and three-state drivers. The CY6116A and CY6117A have an automatic power-down feature, reducing the power consumption by 83% when deselected.

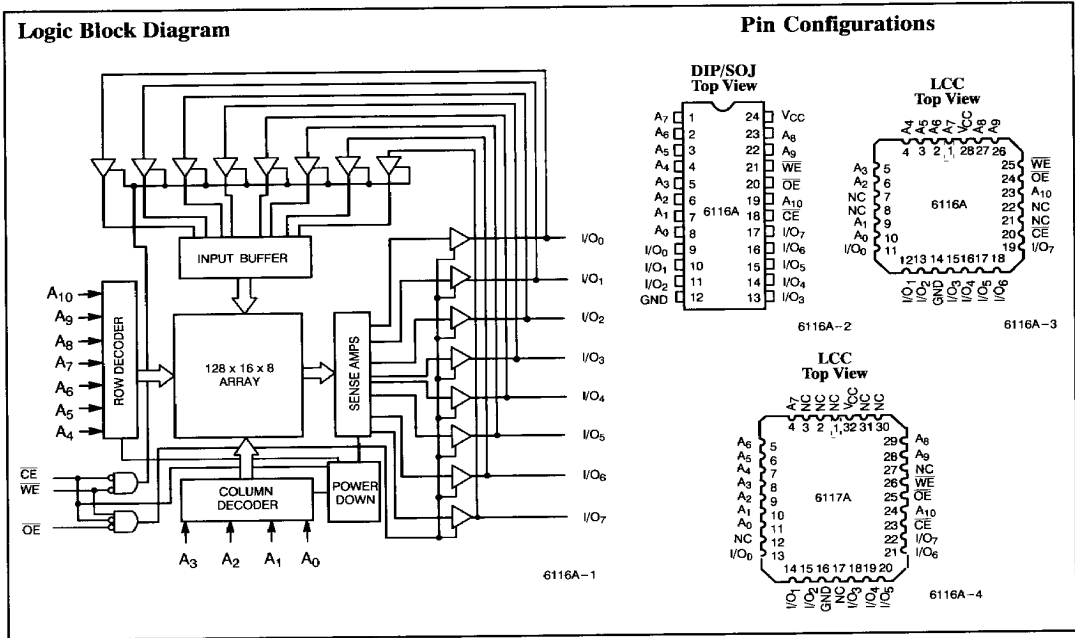
Writing to the device is accomplished when the chip enable (\overline{CE}) and write enable (\overline{WE}) inputs are both LOW. Data on the I/O pins (I/O₀ through I/O₇) is written into the memory location specified on the address pins (A₀ through A₁₀).

Reading the device is accomplished by taking chip enable (\overline{CE}) and output enable (\overline{OE}) LOW while write enable (\overline{WE}) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable (\overline{CE}) is HIGH or write enable (\overline{WE}) is LOW.

The CY6116A and CY6117A utilize a die coat to insure alpha immunity.

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SRAMS



Selection Guide

		6116A-20 6117A-20	6116A-25 6117A-25	6116A-35 6117A-35	6116A-45 6117A-45	6116A-55 6117A-55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	100	100	100	100	80
	Military		125	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	20	20	20	20
	Military		40	20	20	20

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to + 150°C
Ambient Temperature with Power Applied	- 55°C to + 125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12)	- 0.5V to + 7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to + 7.0V
DC Input Voltage	- 3.0V to + 7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military ^[1]	- 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

Parameters	Description	Test Conditions	6116A-20 6117A-20		6116A-25, 35, 45 6117A-25, 35, 45		6116A-55 6117A-55		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[3]		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA f = f _{MAX} = 1/t _{TRC}	Com'l		100	100	80	mA	
			Mil 25			125	100		
			35, 45			100			
I _{SB1}	Automatic CE Power-Down Current - TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} f = f _{MAX}	Com'l		40	20	20	mA	
			Mil 25			40	20		
			35, 45, 55			20			
I _{SB2}	Automatic CE Power-Down Current - CMOS Inputs	Max. V _{CC} , CE ≥ V _{IH} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l		20	20	20	mA	
			Mil			20	20		

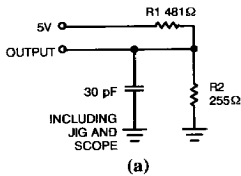
Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

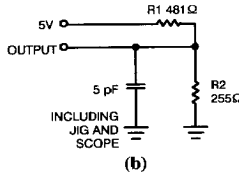
Notes:

- T_A is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- V_{IL (min.)} = -3.0V for pulse durations less than 30 ns.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

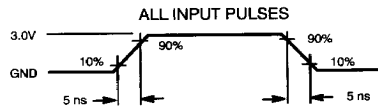
AC Test Loads and Waveforms



(a)



(b)



Equivalent to: THEVENIN EQUIVALENT
OUTPUT ——— 167Ω ——— 1.73V

6116A-5

6116A-6

Switching Characteristics Over the Operating Range^[2, 6]

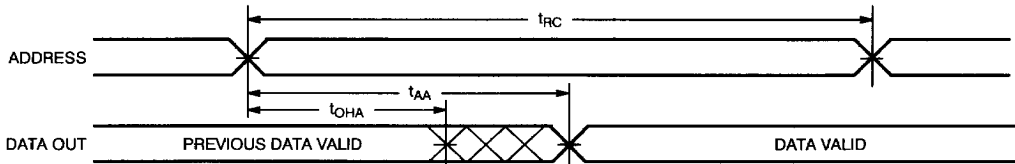
Parameters	Description	6116A-20		6116A-25		6116A-35		6116A-45		6116A-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	20		25		35		45		55		ns
t _{AA}	Address to Data Valid		20		25		35		45		55	ns
t _{OHA}	Data Hold from Address Change	5		5		5		5		5		ns
t _{ACE}	\overline{CE} LOW to Data Valid		20		25		35		45		55	ns
t _{DOE}	\overline{OE} LOW to Data Valid		10		12		15		20		25	ns
t _{LZOE}	\overline{OE} LOW to Low Z	3		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z ^[7]		8		10		12		15		20	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[8]	5		5		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[7, 8]		8		10		15		15		20	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		20		20		20		25		25	ns
WRITE CYCLE^[9]												
t _{WC}	Write Cycle Time	20		20		25		40		50		ns
t _{SCE}	\overline{CE} LOW to Write End	15		20		25		30		40		ns
t _{AW}	Address Set-Up to Write End	15		20		25		30		40		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	15		15		20		20		25		ns
t _{SD}	Data Set-Up to Write End	10		10		15		15		25		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{HZWE}	\overline{WE} LOW to High Z		7		7		10		15		20	ns
t _{LZWE}	\overline{WE} HIGH to Low Z	5		5		5		5		5		ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- \overline{WE} is HIGH for read cycle.
- Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL}.
- Address valid prior to or coincident with \overline{CE} transition LOW.
- Data I/O pins enter high-impedance state, as shown, when \overline{OE} is held LOW during write.
- If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

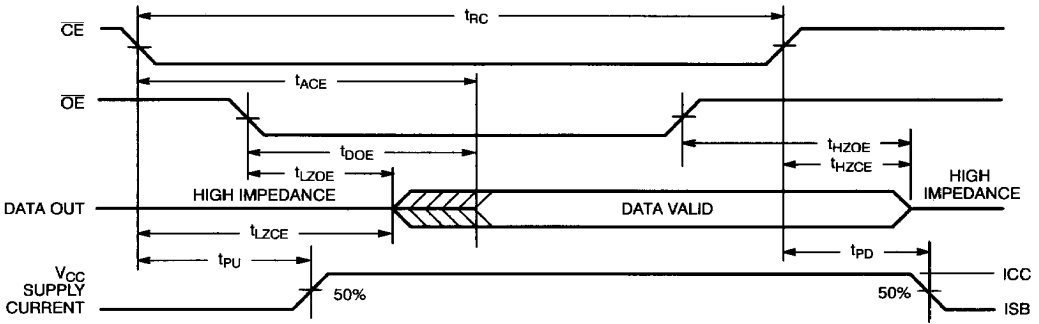
Switching Waveforms

Read Cycle No. 1^[10, 11]



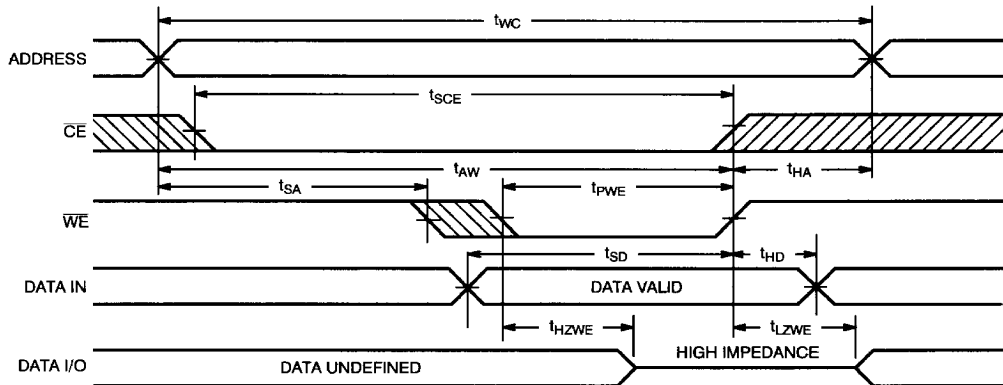
6116A-7

Read Cycle No. 2^[10, 12]



6116A-8

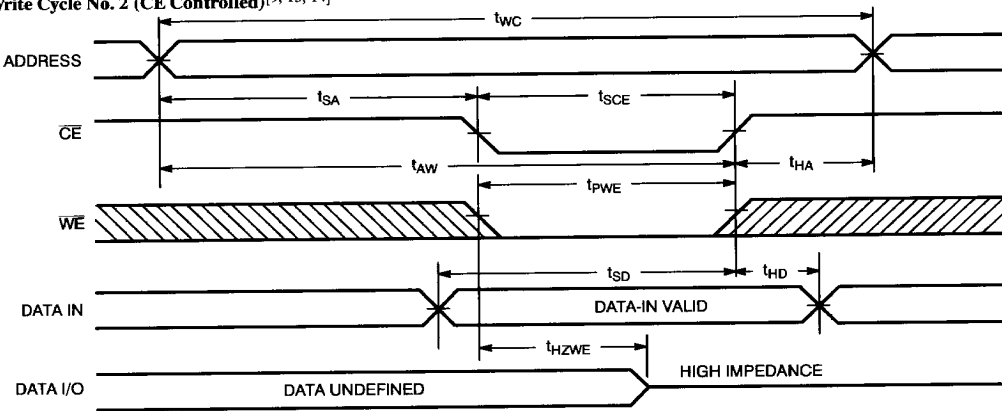
Write Cycle No. 1 (WE Controlled)^[9, 13]



6116A-9

Switching Waveforms (continued)

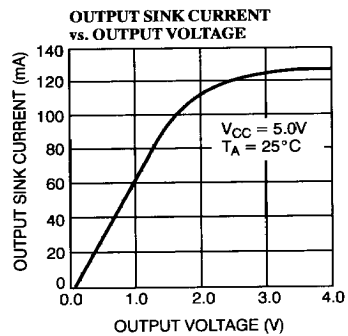
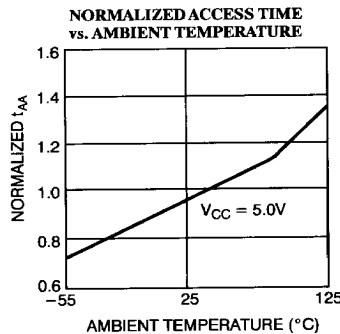
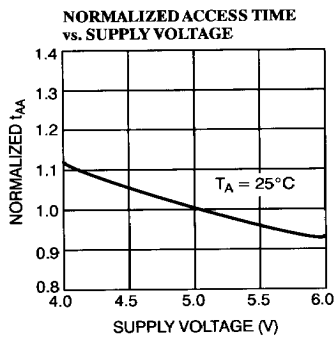
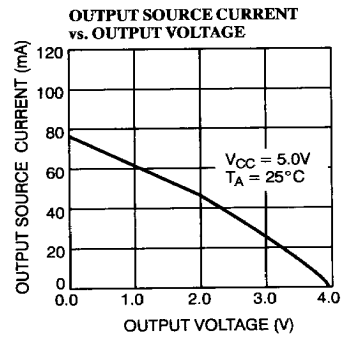
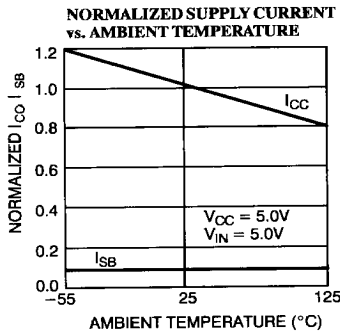
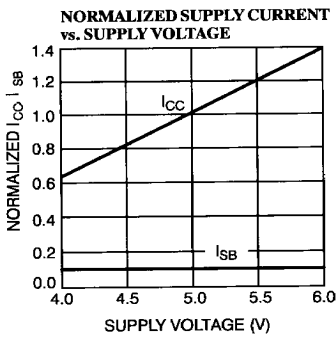
Write Cycle No. 2 (CE Controlled)^[9, 13, 14]



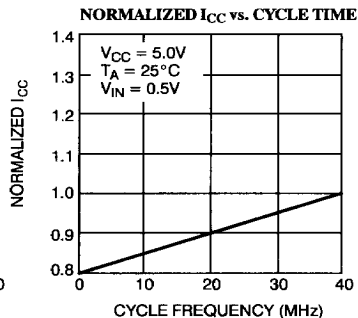
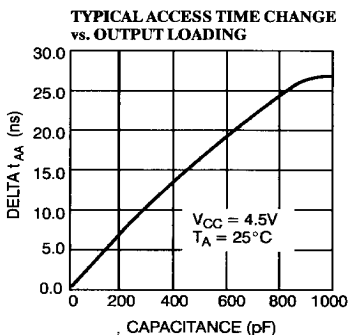
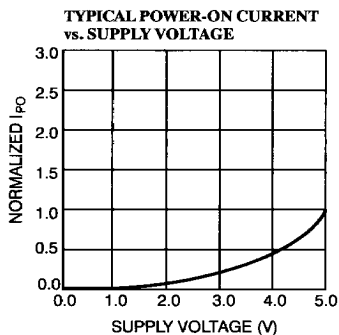
6116A-10

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SRAMS

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
20	CY6116A-20PC	P11	Commercial
	CY6116A-20DC	D12	
25	CY6116A-25PC	P11	Commercial
	CY6116A-25DC	D12	
	CY6116A-25LC	L64	
	CY6116A-25DMB	D12	Military
	CY6116A-25LMB	L64	
35	CY6116A-35PC	P11	Commercial
	CY6116A-35DC	D12	
	CY6116A-35LC	L64	
	CY6116A-35DMB	D12	Military
	CY6116A-35LMB	L64	
45	CY6116A-45PC	P11	Commercial
	CY6116A-45DC	D12	
	CY6116A-45LC	L64	
	CY6116A-45DMB	D12	Military
	CY6116A-45LMB	L64	
55	CY6116A-55PC	P11	Commercial
	CY6116A-55DC	D12	
	CY6116A-55LC	L64	
	CY6116A-55DMB	D12	Military
	CY6116A-55LMB	L64	

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY6117A-25LMB	L55	Military
35	CY6117A-35LMB	L55	Military
45	CY6117A-45LMB	L55	Military
55	CY6117A-55LMB	L55	Military

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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