SONY

CXK77V3211R -14L/14

32768-word by 32-bit High Speed Synchronous Static RAM

Description

The CXK77V3211R is a 32K x 32 high performance synchronous SRAM with a 2-bit burst counter and output register. All synchronous inputs pass through register controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion (CE2, $\overline{CE2}$), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$), four individual byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$), one byte write enable ($\overline{BWE}$), and global write enable ($\overline{SGW}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and power down control (ZZ). Two mode control pins ($\overline{LBO}$, $\overline{FT}$) define four different operation modes: Linear/Interleaved burst sequence and Flow-Thru/Pipelined operations.

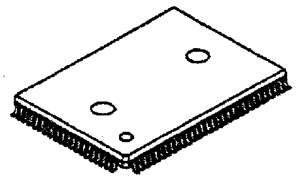
WRITE cycles can be from one to four bytes wide as controlled by $\overline{BW1}$ through $\overline{BW4}$ and $\overline{BWE}$ or $\overline{SGW}$. The output register is included on-chip and controlled by clock, it can be activated by connecting $\overline{FT}$ to high for high speed pipeline operation.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$). Burst order sequence can be controlled by connecting $\overline{LBO}$ to high for Interleaved burst order (i486/Pentium™) or by connecting $\overline{LBO}$ to low for Linear burst order.

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. WRITE pass through makes written data immediately available at the output register during READ cycle following a WRITE as controlled by $\overline{OE}$.

The CXK77V3211R operates from a +3.3V power supply and all inputs and outputs are LVTTL compatible. The device is ideally suited for i486 and Pentium™ systems and those systems which benefit from a very wide data bus.

100 pin LQFP (Plastic)



Structure

Silicon gate CMOS IC

Features

- Fast address access times and High frequency operation

Symbol	Flow-through		Pipeline	
	Access	Cycle	Access	Cycle
-14L/14	14ns	50MHz	8ns	66MHz

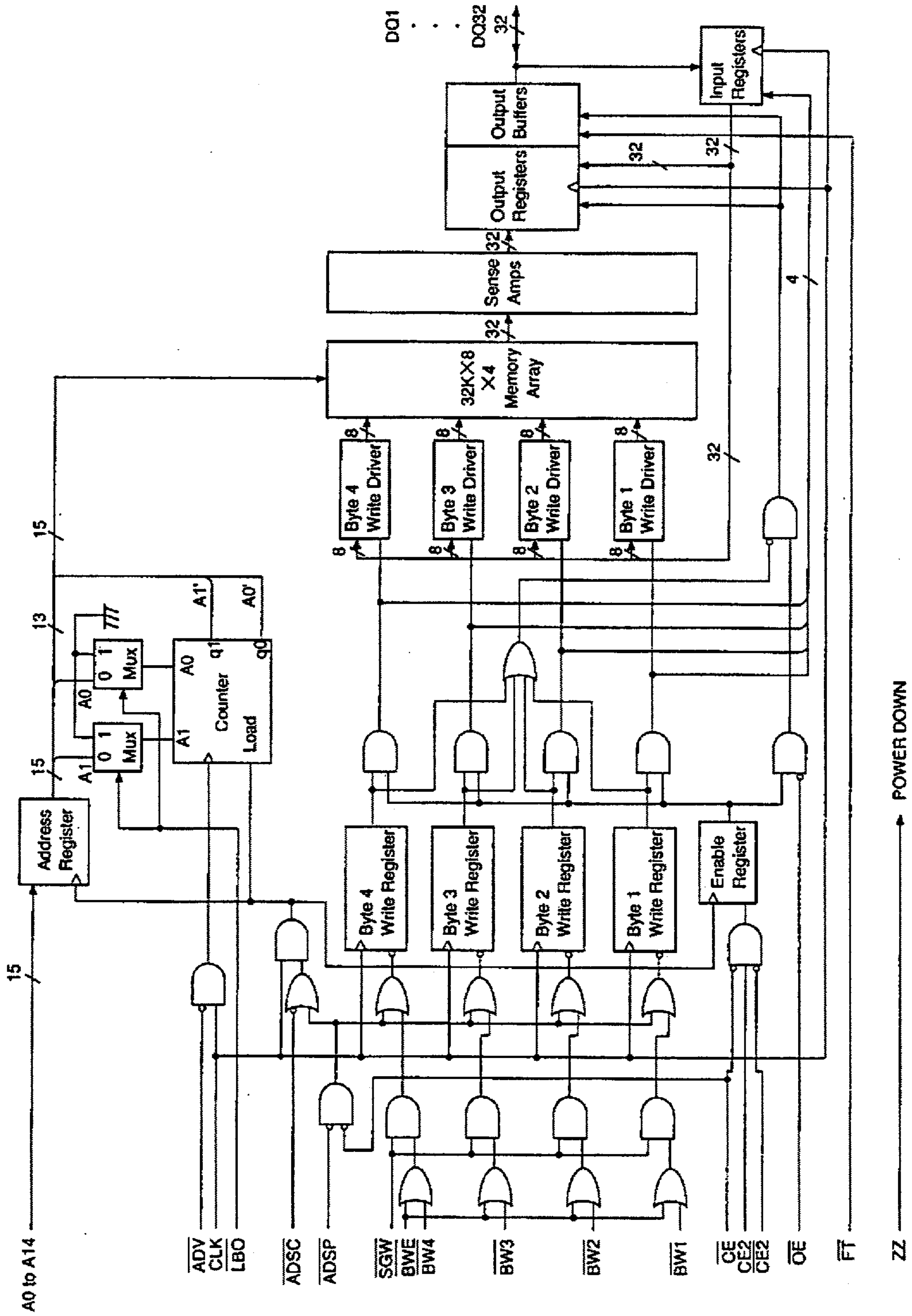
- Low supply current

Operation	:	210mA	(Max.)
Standby (-14)	:	20mA	(Max.)
Standby (-14L)	:	2mA	(Max.)

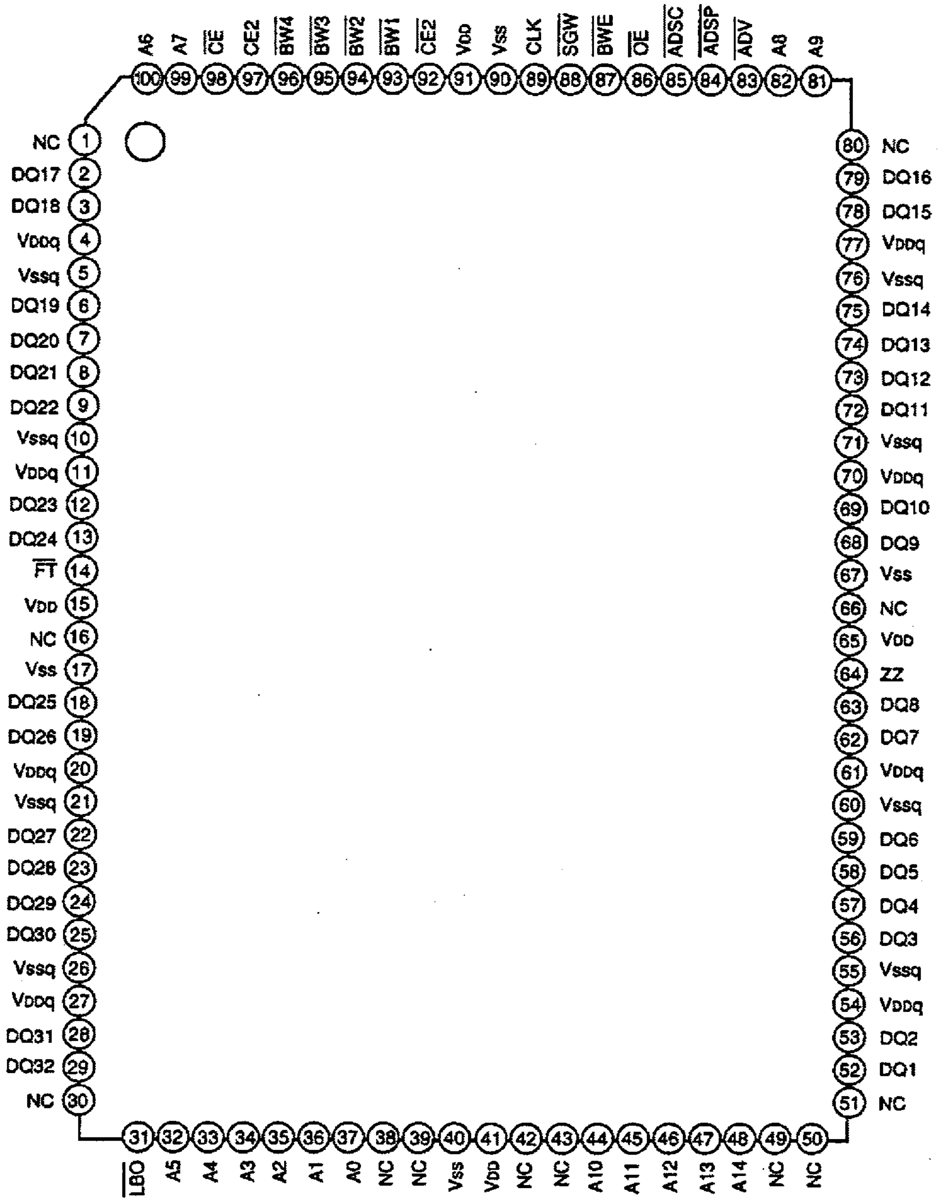
- 5V tolerant inputs except I/O pins
- A $\overline{FT}$ pin for pipelined or flow-thru architecture
- A $\overline{LBO}$ mode pin as burst control pin (i486/Pentium™ and Linear burst sequence)
- Single +3.3V ±5% power supply
- Common data inputs and data outputs
- All inputs and outputs are LVTTL compatible
- Four Individual BYTE WRITE enables, GLOBAL WRITE and BYTE WRITE ENABLE
- Three Chip Enables for simple depth expansion
- One cycle output disable for both pipelined and flow-thru operation
- Internal input registers for address, data and control signals
- Self-timed WRITE cycle
- Write pass through capability
- High 30pF output drive capability
- A ZZ pin for powerdown
- 100-lead LQFP package for high density, high speed operation

i486/Pentium is a trademark of Intel Corp.

Block Diagram



Pin Configuration



Pin Description

Symbol	I/O	Description
A0 to A14	I	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
$\overline{\text{BW1}}$, $\overline{\text{BW2}}$, $\overline{\text{BW3}}$, $\overline{\text{BW4}}$	I	Synchronous Individual Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A BYTE WRITE enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{\text{BW1}}$ controls DQ1 to DQ8. $\overline{\text{BW2}}$ controls DQ9 to DQ16. $\overline{\text{BW3}}$ controls DQ17 to DQ24. $\overline{\text{BW4}}$ controls DQ25 to DQ32. Data I/O are tristated if any of these four inputs are LOW.
CLK	I	Clock: This signal latches the address, data, chip enable, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
$\overline{\text{CE}}$	I	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{\text{ADSP}}$. This input is sampled only when a new external address is loaded.
$\overline{\text{CE2}}$	I	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
CE2	I	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
$\overline{\text{OE}}$	I	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
$\overline{\text{ADV}}$	I	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait status to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{\text{ADSP}}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
$\overline{\text{ADSP}}$	I	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be latched. A READ is performed using the new address, independent of the byte write enables and $\overline{\text{ADSC}}$ but dependent upon CE2 and $\overline{\text{CE2}}$. $\overline{\text{ADSP}}$ is ignored if CE is HIGH. Power down state is entered if CE2 is LOW or $\overline{\text{CE2}}$ is HIGH.
$\overline{\text{ADSC}}$	I	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be latched. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.
NC	–	No Connect: These signals are not internally connected.
DQ1 to DQ32	I/O	SRAM Data I/O: Byte 1 is DQ1 to DQ8; Byte 2 is DQ9 to DQ16; Byte 3 is DQ17 to DQ24; Byte 4 is DQ25 to DQ32. Input data must meet setup and hold times around the rising edge of CLK.
$\overline{\text{BWE}}$	I	Byte Write Enable: This active low input enables individual byte to write.
$\overline{\text{SGW}}$	I	Global Write: This active low input enables to write all bytes.
$\overline{\text{FT}}$	I	Flow Through: This active low input selects flow through output.
$\overline{\text{LBO}}$	I	Linear Burst: This active high input selects interleaved burst sequence.
ZZ	I	ZZ: This active high input enables the device in powerdown mode.
V_{DD}	Supply	Power Supply: +3.3V ± 5%
V_{SS}	Supply	Ground: GND
V_{DDQ}	Supply	Isolated Output Buffer Supply: +3.3V ± 5%
V_{SSQ}	Supply	Isolated Output Buffer Ground: GND

Interleaved Burst Sequence Table

Operation	Address used		
	A14 to A2	A1	A0
First access, latch external address	A14 to A2	A1	A0
Second access (first burst address)	latched A14 to A2	latched A1	latched $\overline{A0}$
Third access (second burst address)	latched A14 to A2	latched $\overline{A1}$	latched A0
Fourth access (third burst address)	latched A14 to A2	latched $\overline{A1}$	latched $\overline{A0}$

Interleaved Burst Address Table

First address	Second address	Third address	Fourth address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

Linear Burst Address Table

First address	Second address	Third address	Fourth address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

Pass-Through Truth Table

Previous cycle		Present cycle				Next cycle
Operation	$\overline{BWs}$	Operation	$\overline{CE}$	$\overline{BWs}$	$\overline{OE}$	Operation
Initial WRITE cycle, all bytes Address = A (n – 1), data = D (n – 1)	All L	Initial READ cycle Register A (n), Q = D (n – 1)	L	H	L	Read D (n)
Initial WRITE cycle, all bytes Address = A (n – 1), data = D (n – 1)	All L	No new cycle Q = D (n – 1)	H	H	L	No carryover from previous cycle
Initial WRITE cycle, all bytes Address = A (n – 1), data = D (n – 1)	All L	No new cycle Q = HIGH-Z	H	H	H	No carryover from previous cycle
Initial WRITE cycle, one byte Address = A (n – 1), data = D (n – 1)	One L	No new cycle Q = D (n – 1) for one byte	H	H	L	No carryover from previous cycle

Note) Previous cycle may be either BURST or NONBURST cycle.

Function	$\overline{\text{LBO}}$
Linear burst	L
Interleaved burst	H or NC

Function	$\overline{\text{FT}}$
Flow-thru output	L or NC
Pipelined output	H

Function	ZZ
Powerdown to I_{SB1}	H
Active	L or NC

Partial Truth Table

Function	$\overline{\text{SGW}}$	$\overline{\text{BWE}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	$\overline{\text{BW4}}$
READ	H	H	X	X	X	X
READ	H	L	H	H	H	H
WRITE byte 1	H	L	L	H	H	H
WRITE all bytes	H	L	L	L	L	L
WRITE all bytes	L	X	X	X	X	X

Absolute Maximum Rating (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{DD}	–0.5 to +4.6	V
Input voltage	V_{IN}	–0.5 to 6 (Max.)	V
Power dissipation	P_D	1.6	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · sec

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{DD}	3.135	3.3	3.465	V	1
Input high voltage	V_{IH}	2.0	–	5.5	V	1, 2
Input low voltage	V_{IL}	–0.3	–	0.8	V	1, 2

Note) 1. All voltage referenced to V_{SS} (GND).

2. Overshoot: $V_{IH} \leqq V_{DD}$ +2.0V for $t \leqq t_{KC}/2$.
Undershoot: $V_{IL} \geqq -2.0$V for $t \leqq t_{KC}/2$.

DC and Operating Characteristics (V_{DD} = 3.3V ± 5%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test condition		Min.	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{DD}		–1	1	μA
Output leakage current	I_{LO}	Output disabled, V_{OUT} = GND to V_{DD}		–1	1	μA
Operating supply current	I_{DD}-0MHz I_{DD}-66MHz	Device selected; all inputs $\leqq V_{IL}$ or $\geqq V_{IH}$; cycle time $\geqq t_{KC}$ min, V_{DD} = MAX; output open		–	20 210	mA
Static CMOS supply current	I_{DD1}-0MHz	All inputs $\leqq$ 0.2V or $\geqq V_{DD}$ –0.2V	-14L	–	2	mA
			-14		20	
Standby current	I_{SB1}	ZZ $\geqq V_{DD}$ –0.2V, All inputs $\leqq$ 0.2V or $\geqq V_{DD}$ –0.2V	-14L	–	2	mA
			-14		20	
Deselect supply current	I_{SB2}-0MHz I_{SB2}-66MHz	Device deselect		–	20 120	mA
Output High voltage	V_{OH}	I_{OH} = –5.0mA		2.4	–	V
Output Low voltage	V_{OL}	I_{OL} = 5.0mA		–	0.4	V

(V_{DD} = 3.3V$^{+10\%}_{-5\%}$ except for I_{DD1}, I_{SB1})

DC and Operating Characteristics for Special Modes-pins

Mode-pins	V_{IN}	I_{LI}
$\overline{FT}$ ZZ	$\geqq V_{IH}$ + 0.5V $< V_{IH}$ + 0.5V	<1μA >10KΩ to Vss
$\overline{LBO}$	$\geqq V_{IL}$ $< V_{IL}$	<1μA >10KΩ to V_{DD}

These Mode-pin input buffers ($\overline{FT}$, ZZ, $\overline{LBO}$) have special self-bias circuit to protect against coupling noise when these pins are not connected during normal operations.

AC Electrical Characteristics

($V_{DD} = 3.3V ^{+10\%}_{-5\%}$, Ta = 0 to +70°C)

Item		Symbol	-14L/-14		Unit
			Min.	Max.	
Flow-thru	Clock to output valid	t_{KQ}	–	14	ns
	Clock to output invalid	t_{KQX}	3	–	ns
	Clock to output in Low-Z	t_{LZ}[2]	3	–	ns
	Clock cycle time	t_{KC}	20	–	ns
Pipeline	Clock to output valid	t_{KQ}	–	8	ns
	Clock to output invalid	t_{KQX}	2	–	ns
	Clock to output in Low-Z	t_{LZ}[2]	2	–	ns
	Clock cycle time	t_{KC}	15	–	ns
Clock HIGH time		t_{KH}	4	–	ns
Clock LOW time		t_{KL}	4	–	ns
Clock to output in High-Z		t_{HZ}[2]	–	6	ns
$\overline{OE}$ to output valid		t_{OE}	–	6	ns
$\overline{OE}$ to output in Low-Z		t_{OLZ}[2]	0	–	ns
$\overline{OE}$ to output in High-Z		t_{OHZ}[2]	–	6	ns
Setup time		t_S	2.5	–	ns
Hold time		t_H	0.5	–	ns
ZZ setup		t_{ZZS}[3]	5	–	ns
ZZ hold		t_{ZZH}[3]	1	–	ns
ZZ recovery		t_{ZZR}	20	–	ns

1. All parameters are specified over the range 0 to 70°C.
2. These parameters are sampled and are not 100% tested.
3. Signal is asynchronous, however, to be recognized on any given clock the signal must meet specified setup and hold times.

I/O capacitance (Ta = 25°C, f = 1MHz)

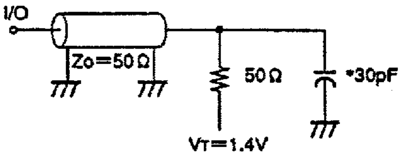
Item	Symbol	Test condition	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	4	5	pF
I/O capacitance	C_{OUT}	$V_{I/O}$ = 0V	6	7	pF

This parameter is sampled and is not 100% tested.

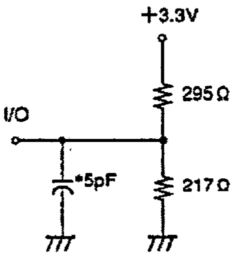
AC Test Conditions (V_{DD} = 3.3V $^{+10\%}_{-5\%}$, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 2.8V
Input pulse low level	V_{IL} = 0V
Input rise time	t_r = 1V/ns
Input fall time	t_f = 1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load conditions	Fig. 1 and Fig. 2

- * Include scope and jig capacitance.
- * Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- * Output load (2) for t_{LZ} and t_{HZ}, t_{OLZ} and t_{OHZ}.



Output load (1)
Fig. 1.



Output load (2)
Fig. 2.

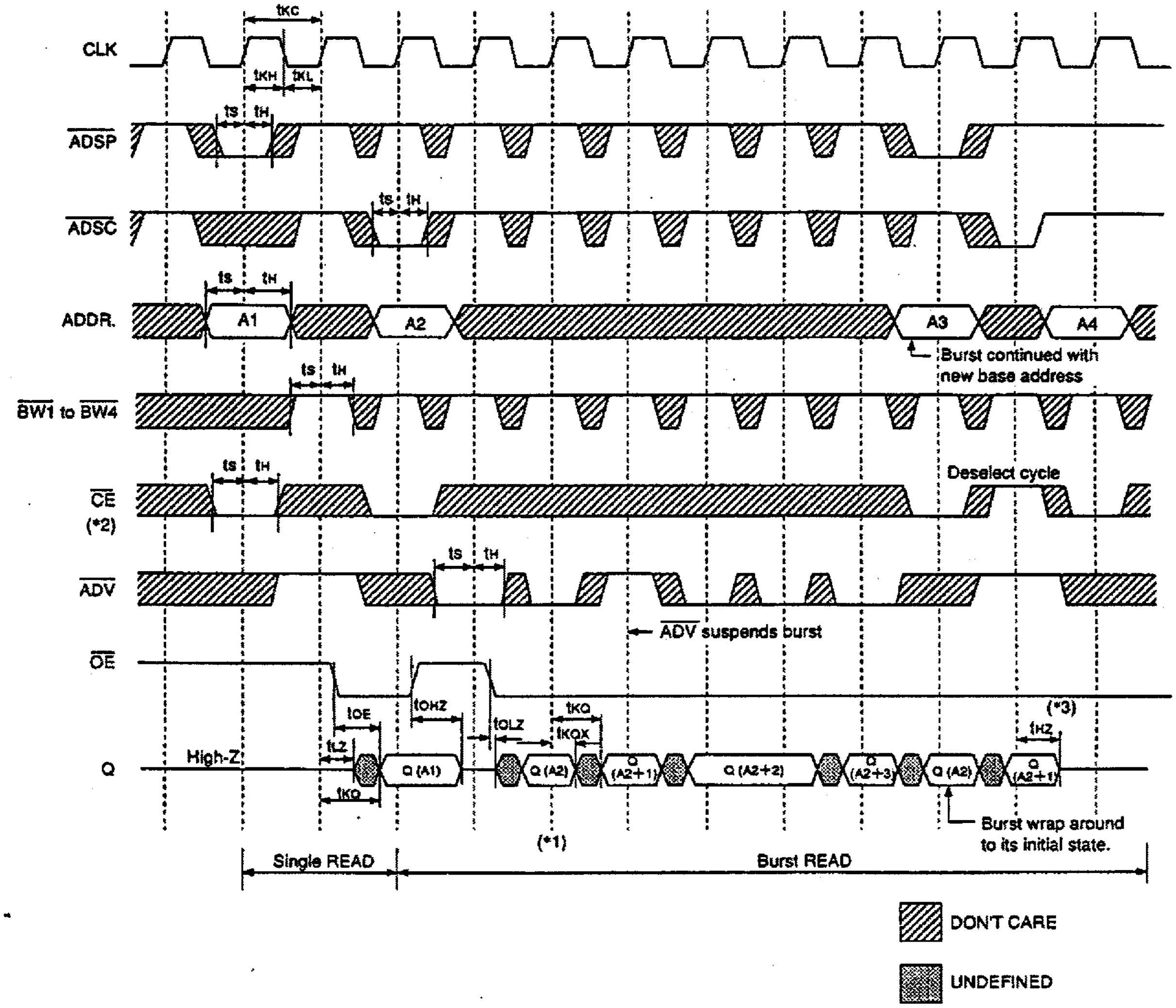
Truth Tables

Operation	Address used	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{BWx}$	$\overline{OE}$	CLK	DQ
Deselected cycle, power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected cycle, power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected cycle, power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected cycle, power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected cycle, power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ cycle, begin burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ cycle, begin burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE cycle, begin burst	External	L	L	H	H	L	X	L	X	L-H	D
READ cycle, begin burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ cycle, begin burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ cycle, continue burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ cycle, continue burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ cycle, continue burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ cycle, continue burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE cycle, continue burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE cycle, continue burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ cycle, suspend burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ cycle, suspend burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ cycle, suspend burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ cycle, suspend burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE cycle, suspend burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE cycle, suspend burst	Current	H	X	X	X	H	H	L	X	L-H	D

Note)

1. X means "don't care". H means logic HIGH. L means logic LOW. $\overline{BWx}$ = L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$) are LOW. $\overline{BWx}$ = H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1 to DQ8). $\overline{BW2}$ enables writes to Byte 2 (DQ9 to DQ16). $\overline{BW3}$ enables writes to Byte 3 (DQ17 to DQ24). $\overline{BW4}$ enables writes to Byte 4 (DQ25 to DQ32).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in HIGH-Z during power-up.
7. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

Read Timing (Pipeline)

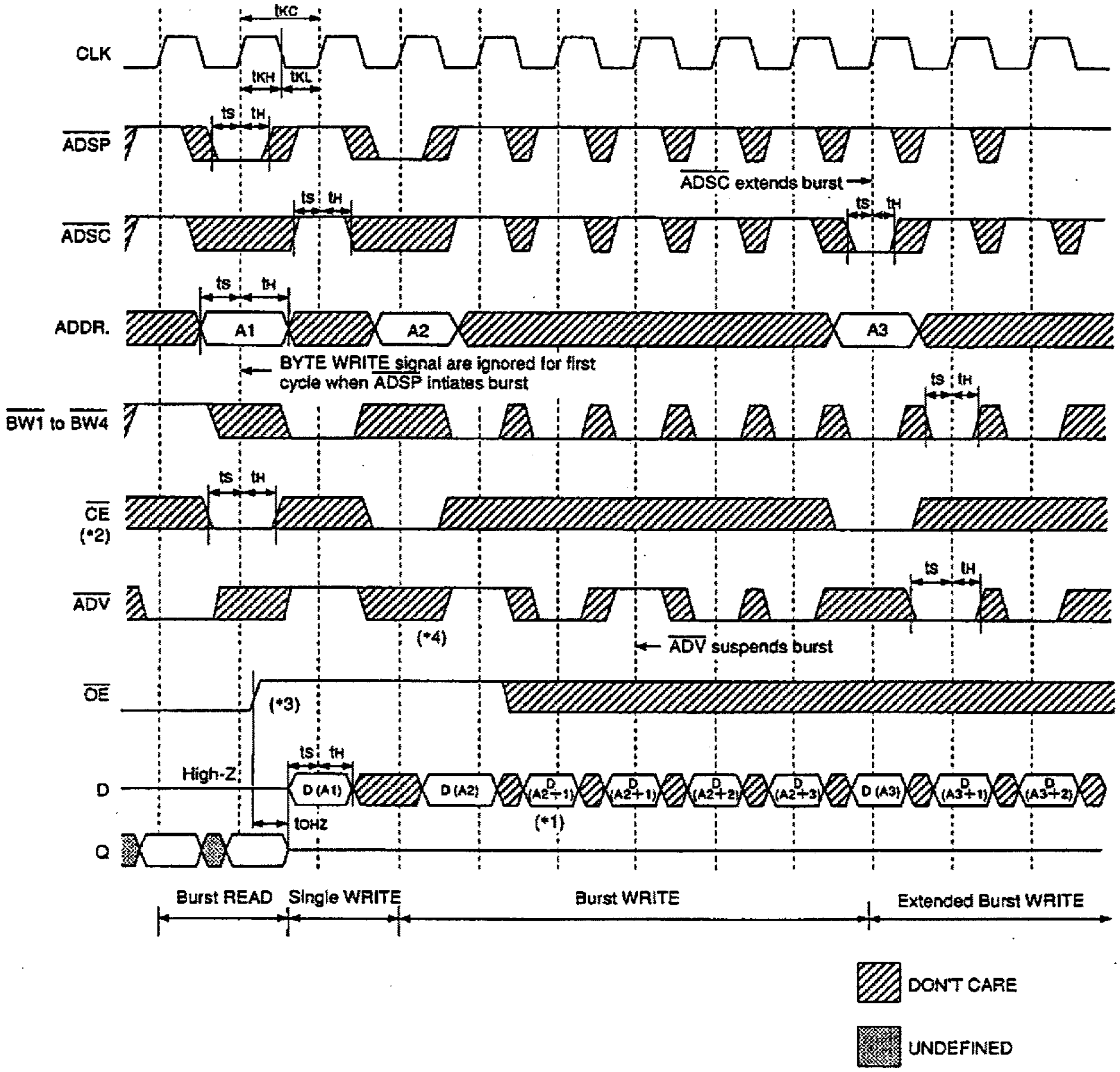


*1 Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

*2 $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE is LOW.

*3 On deselect cycle, Q is tri-stated immediately on the same cycle $\overline{\text{CE}}$ is LOW.

Write Timing (Pipeline)



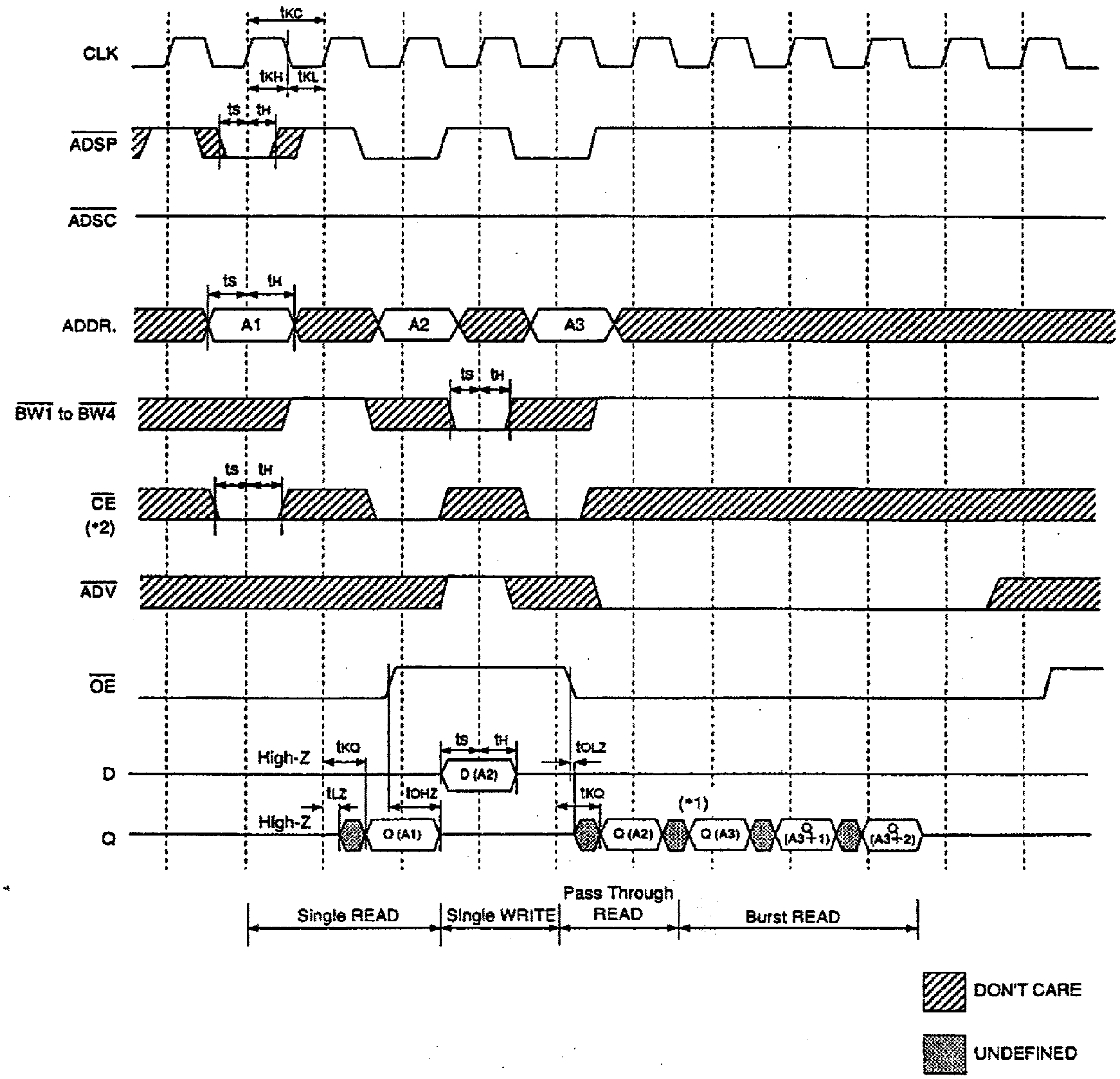
*1 Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

*2 $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.

*3 $\overline{\text{OE}}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.

*4 $\overline{\text{ADV}}$ must be HIGH to permit a WRITE to the loaded address.

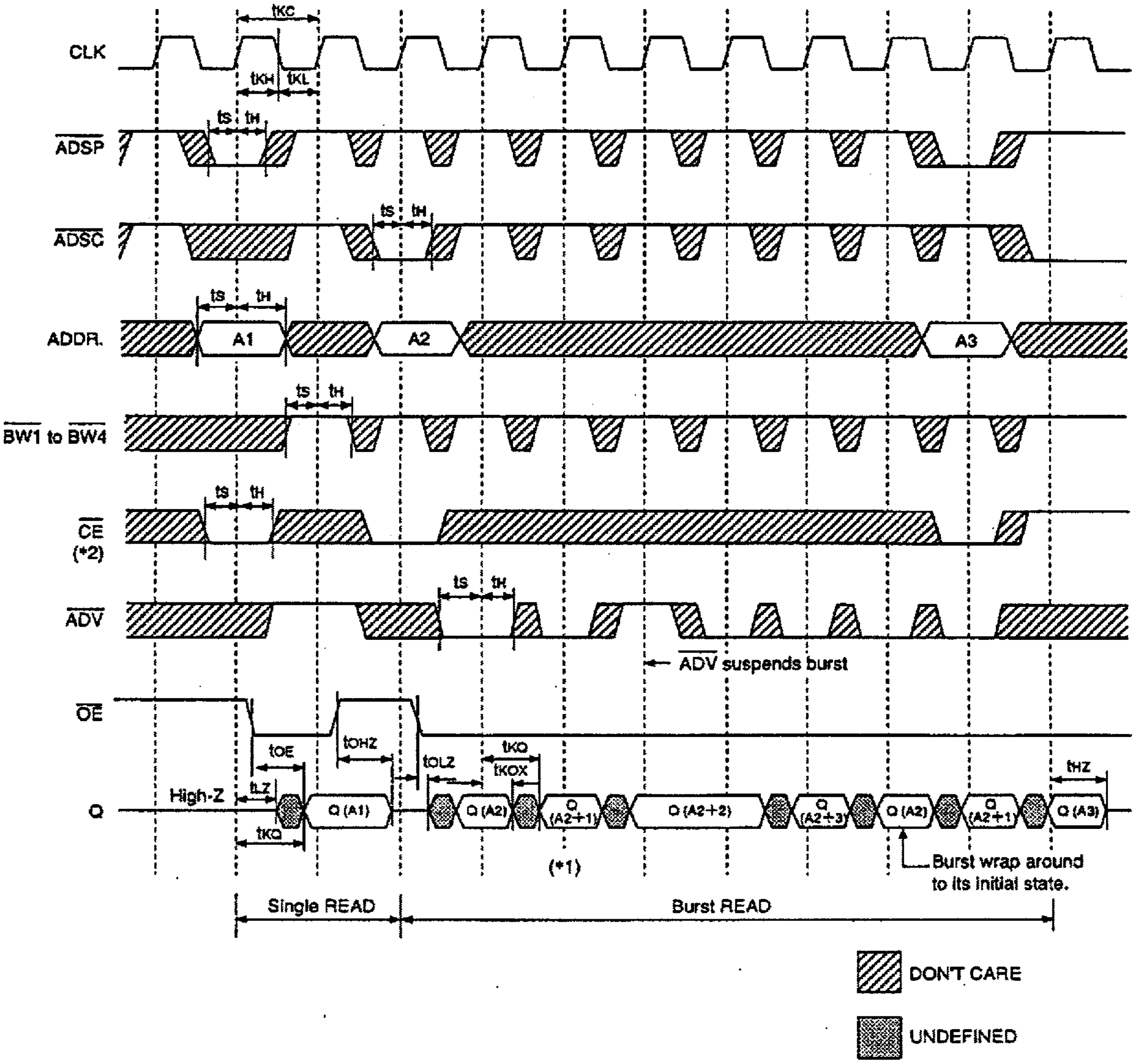
Read/Write Timing (Pipeline)



*1 Q (A3) refers to output from address A3. Q (A3 + 1) refers to output from the next internal burst address following A3.

*2 $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.

Read Timing (Flow-Thru)

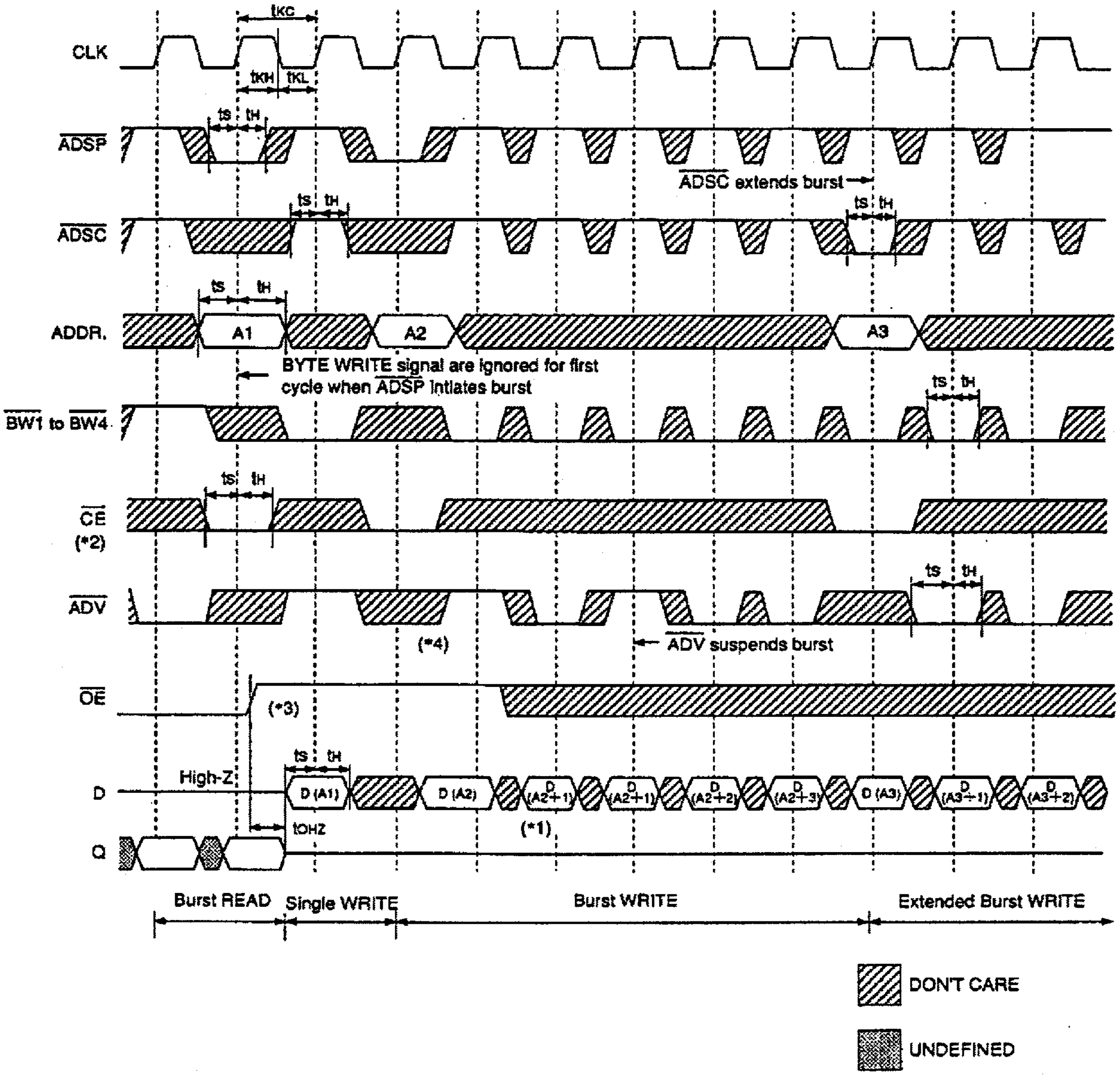


---

*1 Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

*2 $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE is LOW.

Write Timing (Flow-Thru)



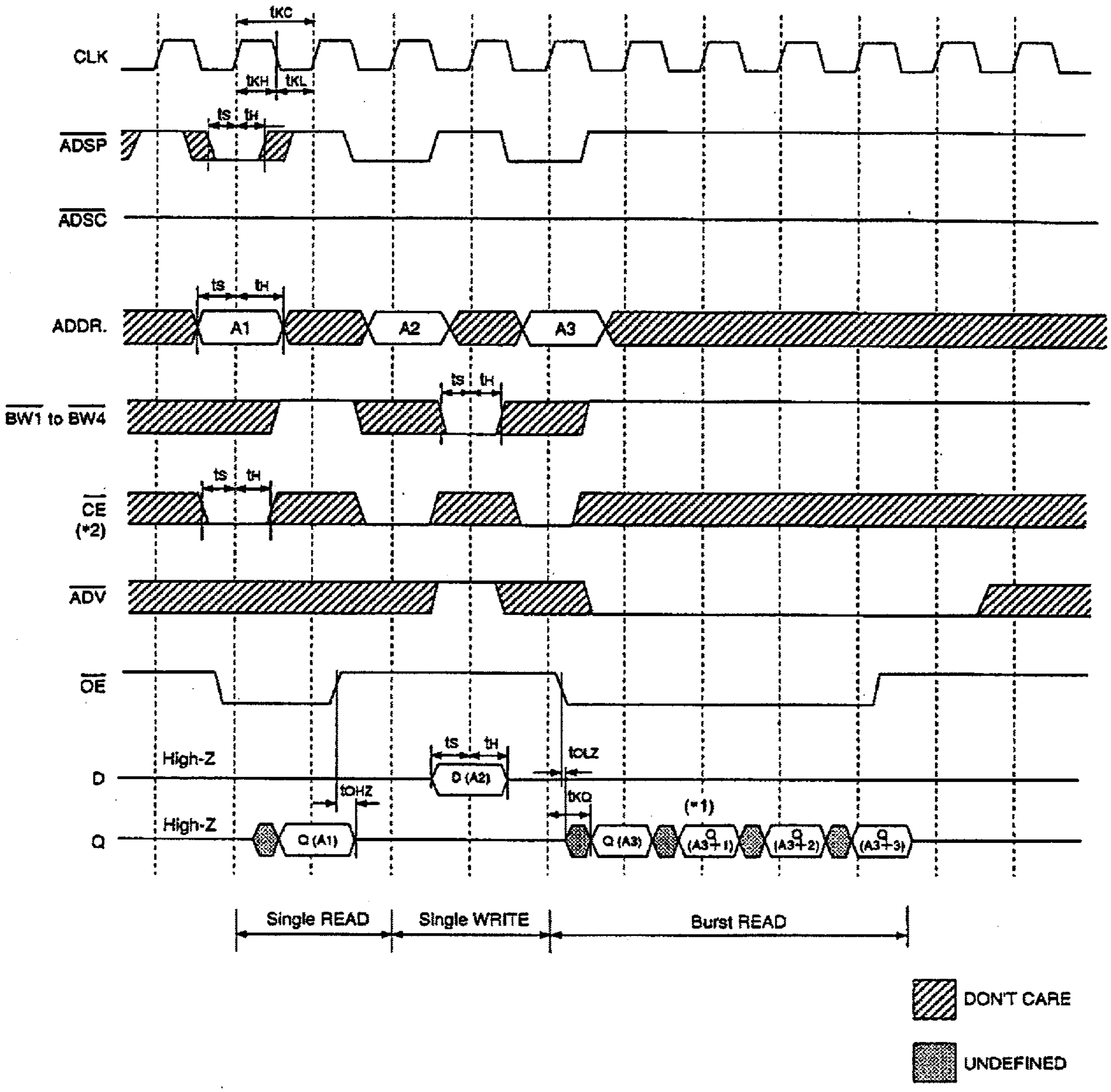
*1 Q (A2) refers to output from address A2. Q (A2 + 1) refers to output from the next internal burst address following A2.

*2 $\overline{\text{CE2}}$ and CE2 have timing identical to $\overline{\text{CE}}$. On this diagram, when $\overline{\text{CE}}$ is LOW, $\overline{\text{CE2}}$ is LOW and CE2 is HIGH. When $\overline{\text{CE}}$ is HIGH, $\overline{\text{CE2}}$ is HIGH and CE2 is LOW.

*3 $\overline{\text{OE}}$ must be HIGH before the input data setup and held HIGH throughout the data hold time. This prevents input/output data contention for the time period to the byte write enable inputs being sampled.

*4 $\overline{\text{ADV}}$ must be HIGH to permit a WRITE to the loaded address.

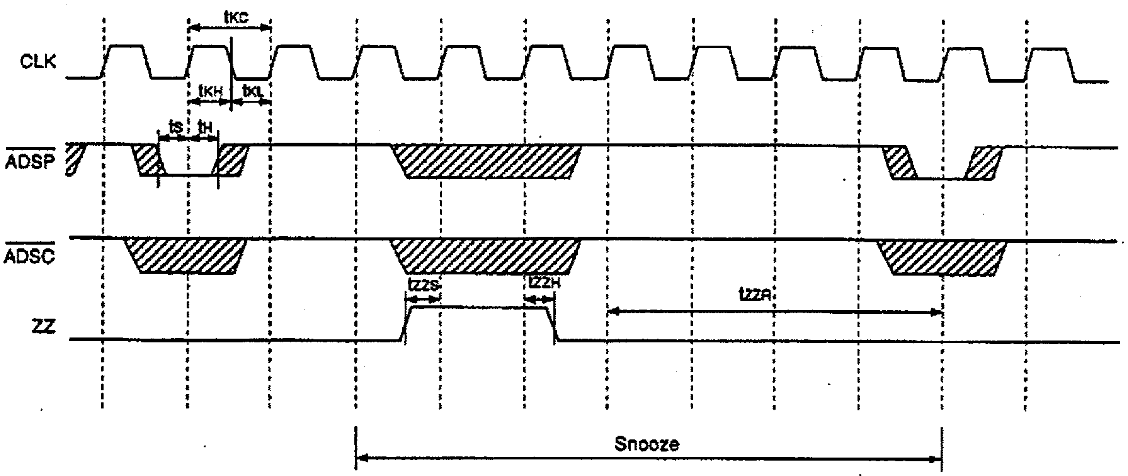
Read/Write Timing (Flow-Thru)



*1 Q (A3) refers to output from address A3. Q (A3 + 1) refers to output from the next internal burst address following A3.

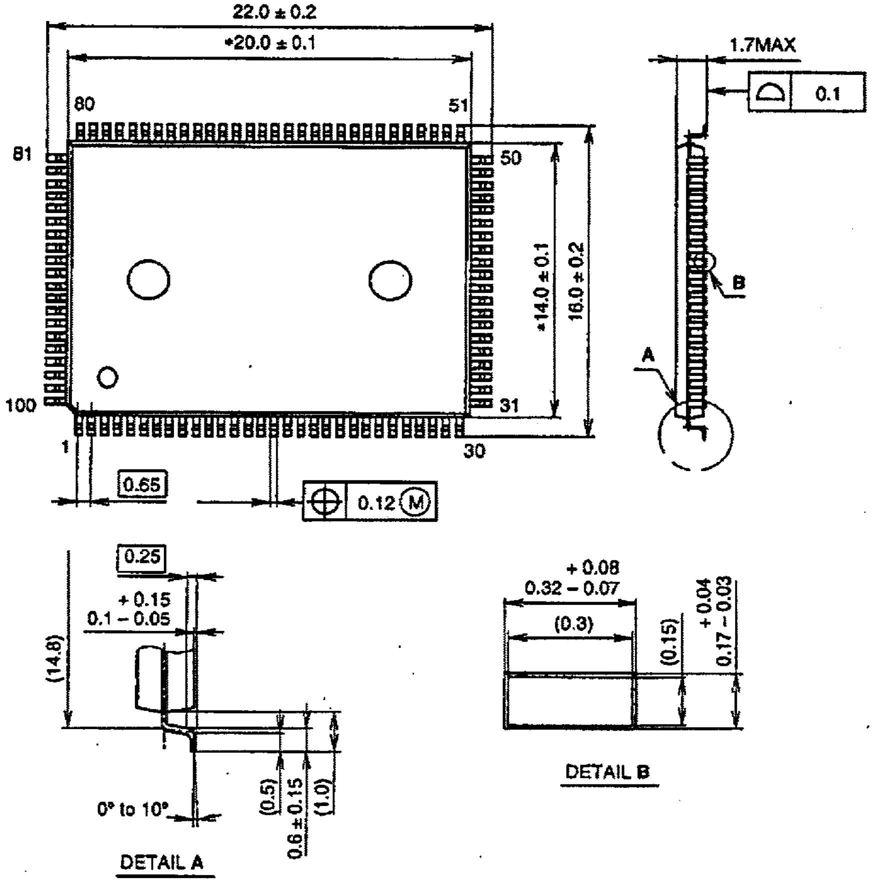
*2 $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

ZZ Timing


tKC
CLK
tKH
tKL
tS
tH
$\overline{ADSP}$
$\overline{ADSC}$
tZZS
tZZH
tZZR
ZZ
Snooze

Package Outline Unit : mm

100PIN LQFP(PLASTIC)1420



NOTE > "*" Dimensions do not include mold protruction.

SONY CODE	LQFP-100P-L141
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE WEIGHT	1.0g