Features

- Supports the multiplexing and demultiplexing of STS-48/STM-16 SONET/SDH signals into an STS-192/STM-64 SONET/SDH signal.

- SONET/SDH low speed side interfaces compatible with AMCC's STS-48/STM-16 devices.

- Supports the transfer of up to four STS-48/STM-16 data streams, carrying any valid combination of STS-48c/AU-4-16c, STS-12c/AU-4-4c, or STS-3c/AU-4 SONET/SDH payloads, to other AMCC SONET/SDH POS/ATM terminating products.

- Provisionable for performance monitoring & regeneration.

- Terminates & generates SONET/SDH transport/section overhead layers, with TOH/SOH interfaces in both mux and demux directions, on the high-speed side.

- Provides a 622.08 MHz 16-bit bus interface on the High Speed line side interface in both the MX and DX directions.

- Provides four 155.52 MHz 16-bit bus interfaces on the low speed line side in both the MX and DX directions.

- Selectable scrambling/descrambling (X^7+X^6+1) of SONET/SDH frame.

- 16-bit synchronous microprocessor interface for configuration, control, and status monitoring.

- Supports Automatic Protection Switching (APS).

- 192x192 Cross-connect with STS-1 Level granularity.

The S19201 is a highly-integrated VLSI device that provides for the multiplexing and demultiplexing of STS-48/STM-16 SONET/SDH signals into an STS-192/STM-64 SONET/SDH signal. When used in conjunction with AMCC's RHINE chip, the INDUS provides a channelized OC-192 solution down to STS-48/STS-12/STS-3 signal payloads. When used in conjunction with AMCC's MISSOURI and DANUBE chips, the INDUS provides a channelized OC-192 to STS-48/STS-12/ STS-3/STS-1 framer/pointer processor solution.

The S19201 provides full section and line overhead processing. It also provides SONET/SDH framing, scrambling/ descrambling, alarm signal insertion/detection, and bit interleaved parity (B1/B2) processing.

The S19201 is SONET/SDH standards compliant with Bellcore GR-253, ITU G.707, and ANSI T1.105 -1995.

A general purpose 16-bit microprocessor interface is provided for control, and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configurations.

Applications

- ATM switches and Packet over SONET Routers

- SONET/SDH Add Drop Multiplexers, Terminal Multiplexers and Digital Cross Connects

- WDM and DWDM

- Test equipment

Figure 1: Block Diagram

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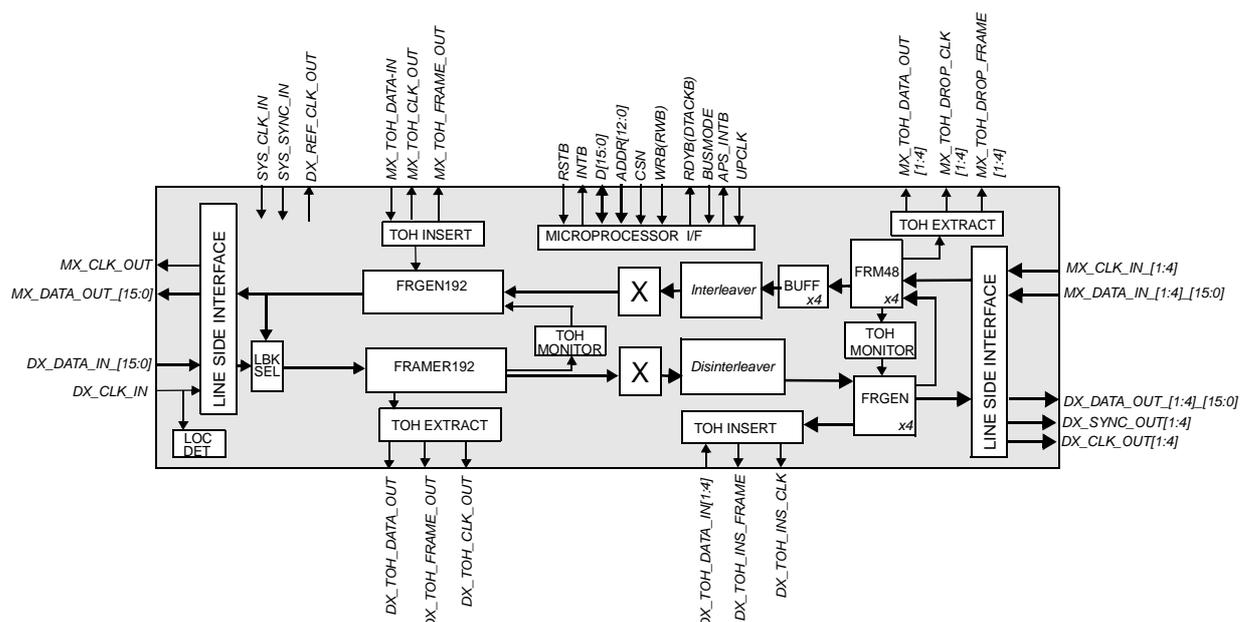
Overview and Applications

SONET Processing

The S19201 can be used in either SONET or SDH applications. On the high-speed side, it interfaces to a STS-192/STM-64 signal in each direction. On the low-speed side, it interfaces to four STS-48/STM-16 signals in each direction.

The S19201 can be used in conjunction with AMCC's RHINE, MISSOURI, or DANUBE chips for terminating STS-48/STM-16 payloads.

In the multiplex direction, the S19201 accepts four 16-bit parallel STS-48/STM-16 (155 Mb/s) signals. The S19201 locates the STS-48/STM-16 frames, descrambles the data, processes the TOH bytes (or SOH bytes in SDH mode), muxes the four STS-48/STM-16 tributaries.

This muxed signal, or the STS-192 from the demux input is then selected as the input to the FRGEN192. The S19201 then generates the TOH bytes (or SOH bytes in SDH mode), performs frame synchronous scrambling, and outputs the data onto a 16-bit bus.

In the demultiplex direction, the S19201 accepts a 16-bit wide STS-192/STM-64 signal. The S19201 locates frame in this signal, performs descrambling, and processes the TOH bytes. This signal is then selected for disinterleaving.

The four tributaries are then output on four 16-bit parallel interfaces.

A TOH/SOH interface provides direct add/drop capability for both Section and Line overhead.

On the multiplex side the S19201 generates section and line overhead. It performs framing pattern insertion (A1, A2), scrambling, alarm signal insertion, and generates section and line Bit Interleaved Parity (B1/B2) for far-end performance monitoring.

On the Demux side the S19201 processes section and line overhead. It performs framing (A1, A2), descrambling, alarm detection, bit interleaved parity monitoring (B1/B2), and error count accumulation for performance monitoring.

High-Speed Interface

On the high-speed side, the S19201 supports 16-bit parallel high-speed interfaces, operating at 622 MHz, on both the multiplex and demultiplex side.

Low-Speed Interface

On the low-speed side, the S19201 supports four 16-bit parallel high-speed interfaces operating at 155 MHz.

Figure 2: Typical Applications: S19201 in a STS-192/AU-4-64 Channelized System

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