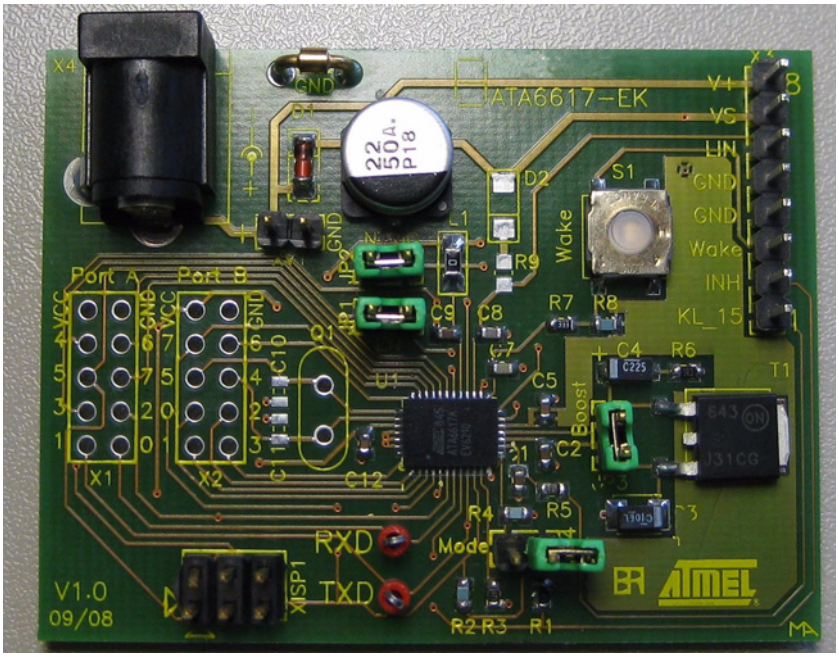
ATA6617 - EK
Development Board V1.1

Features

- All Necessary Components to Put the ATA6617 in to Operation Are Included
- Placeholders for Some Optional Components for Extended Functions Included
- All Pins Easily Accessible
- Easily Adaptable Watchdog Times by Replacing a Single Resistor
- Possibility to Activate an External NPN-transistor to Boost the Output Current of the Voltage Regulator (Jumper JP3)
- Possibility to Select between Master or Slave Operation (Mounting D2 and R1)
- Possibility to Mount an External Quartz to Handle Time-critical Applications (Not Necessary for LIN Communication)
- Push Button Included to Create a Local Wake-up after Entering Sleep or Silent Mode
- Ground Coulter Clip for Connecting Probes when Measuring with the Oscilloscope

Figure 0-1. ATA6617 - EK Development Board



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Application Note

9149A–AUTO–03/09

1. Introduction

The development board for the ATA6617 IC is designed to give designers a quick start with the ATA6617 IC and to enable prototyping and testing new LIN designs.

The ATA6617 is a dual-chip System-in-Package (SIP) product, which is particularly suited for complete LIN bus slave and master node applications. It supports highly integrated solutions for in-vehicle LIN networks. The first chip is the LIN-system-basis-chip (LIN SBC) ATA6624, which has an integrated 5V voltage regulator, a window watchdog, and a fully integrated LIN transceiver, in compliance with the LIN specification 2.1. The second chip is an automotive microcontroller from Atmel®'s series of AVR® 8-bit microcontrollers with advanced RISC architecture (ATtiny167 with 16K flash). All pins of both integrated chips are bonded out to provide customers the same flexibility for their applications as they have when using discrete parts.

The included AVR provides the following features:

- 16 Kbytes of in-system programmable flash with read-while-write capabilities
- 512 bytes EEPROM
- 512 bytes SRAM
- 16 general purpose I/O lines
- 32 general purpose working registers
- Internal 8 MHz RC Oscillator Calibrated at 5V at 25°C
- 2 flexible timer/counters with compare modes
- Internal and external interrupts
- LIN 2.1 and 1.3 controller or 8-Bit UART
- Byte-oriented 2-wire serial interface
- Master/Slave SPI serial interface
- 4-channel 10-bit ADC
- Four software-selectable power-saving modes:
  - Idle Mode stops the CPU while allowing the SRAM, timer/counters, ADC, Analog comparator, and interrupt system to continue functioning.
  - Power-down Mode saves the register contents but freezes the oscillator and disables all other chip functions until the next interrupt or hardware reset.
  - Power-save Mode: the asynchronous timer continues to run allowing the user to maintain a timer base while the rest of the device is sleeping.
  - ADC Noise Reduction Mode stops the CPU and all I/O modules except ADC, which minimize switching noise during ADC conversions.

The included LIN SBC ATA6624 provides the following features:

- Master and slave operation possible
- Supply voltage up to 40V
- Operating voltage VS = 5V to 27V
- Typically 10 µA supply current during Sleep Mode and VCC is switched off
- VCC-undervoltage detection (4 ms reset time) and watchdog reset logical combined at open drain output NRES
- Boosting the voltage regulator possible with an external NPN transistor
- LIN physical layer according to LIN 2.1 specification and SAEJ2602-2
- Wake-up capability via LIN-bus, wake pin, or KI_15 pin
- INH output to control an external voltage regulator or to switch off the master pull up resistor
- TXD time-out timer
- Bus pin is overtemperature and short circuit protected versus GND and battery
- Adjustable watchdog time via external resistor

The combination of the features included in ATA6617 make it possible to develop simple, yet powerful and low cost slave nodes in LIN bus systems.

The IC is designed to handle the low-speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud. Sleep Mode and Silent Mode included in the LIN SBC guarantee a very low current consumption.

As there is a standard AVR microcontroller with all pins available included in the ATA6617, the standard toolchain consisting of the AVR Studio®, front-end assembler and simulator, and in-circuit-emulator can be used for developing and debugging new applications. Using the software components and the development board, it is very easy and inexpensive to create and test a LIN network.

In the contrast to the standalone AVRs, the internal 8 MHz RC oscillator has been calibrated at 5V and therefore perfectly fits the output voltage of the integrated voltage regulator.

This document has been developed to provide the user with start-up information about the ATA6617's development board. For more detailed information about the use of the ATA6617, refer to the corresponding datasheet.

2. Start-up Information

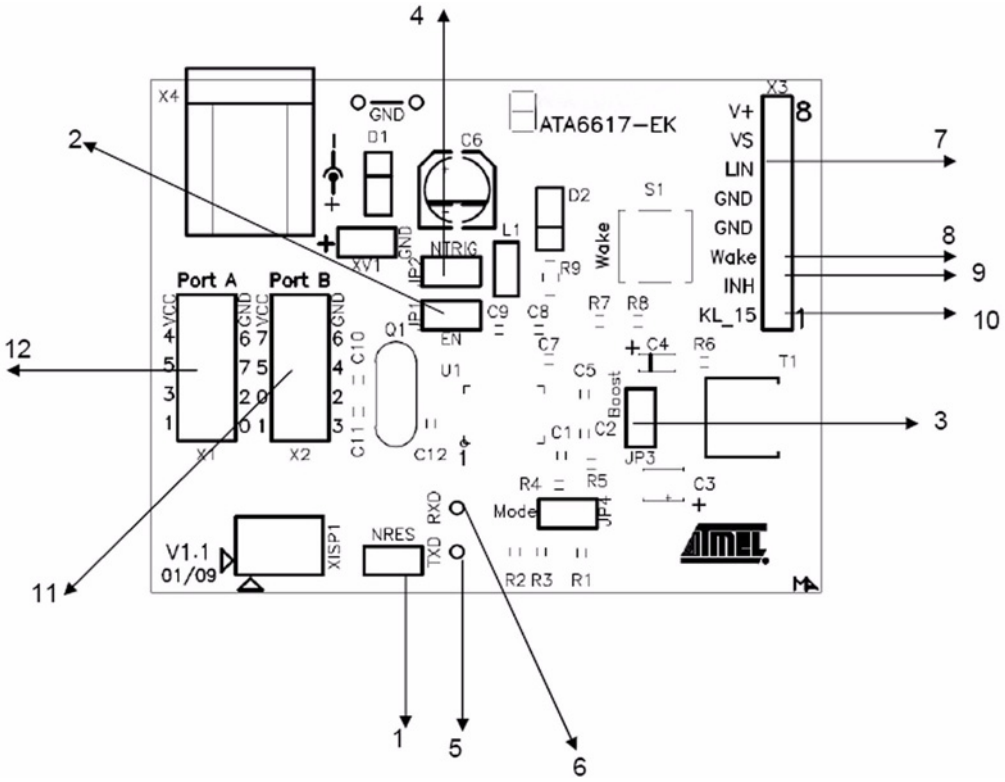
The development board for the ATA6617 is shipped with the default jumper settings and all accessories required for immediate use.

The IC mounted on the board is pre-programmed with a firmware in order to test and to understand the basic functions directly on the board. After correctly connecting an external 12V DC power supply between the terminals “+” and “-”, the LIN SBC is in Fail-safe Mode. A regulated 5V DC voltage, provided by the internal voltage regulator supplying the internal microcontroller, can be measured at the PVCC jumper. After the power is supplied to the microcontroller, the microcontroller switches the LIN SBC to Normal Mode by setting the EN pin to high (ENABLE jumper), and starts to trigger the integrated window watchdog. The system is now ready for data transmission via the LIN bus. Signals fed in at the TXD pin are visible on the LIN bus, and signals fed in on the LIN bus are visible at the RXD pin. In Normal Mode, the current consumption is approximately 3 mA and the following voltages and signals can be seen at the corresponding pins.

Table 2-1. Overview of Pin Status at Start-up of the Development Board

Test Point	Expected Behavior	Additional Information	Symbol
Jumper NRES	5V DC		1
Jumper EN	5V DC		2
Jumper Boost	5V DC		3
Jumper NTRIG	Frequency f ≈ 36.6 Hz	V_{pp} = 5V	4
TXD	Frequency f ≈ 36.6 Hz	V_{pp} = 5V	5
RXD	Frequency f ≈ 36.6 Hz	V_{pp} = 5V	6
LIN	Frequency f ≈ 36.6 Hz	$V_{pp} \cong$ 11V	7
WAKE	~11.2V DC		8
INH	~11.2V DC		9
KL15	0V DC		10
PB0 to PB6	Frequency f ≈ 36.6 Hz	V_{pp} = 5V	11
PB7	5V DC		11
PA0 to PA3, PA5 to PA7	Frequency f ≈ 36.6 Hz	V_{pp} = 5V	12
PA4	5V DC		12

Figure 2-1. ATA6617 Development Board with Reference Point



The board's pre-programmed firmware provides the window watchdog with a valid trigger signal so that the NRES pin is not forced to ground and the microcontroller does not receive any resets.

For testing purposes and to understanding the system, it can be helpful to see the behavior when the watchdog is not triggered correctly. This can be achieved in two different ways without changing the firmware of the IC:

- Remove NTRIG jumper
  No trigger signal reaches the watchdog and the watchdog generates a reset.
- Re-program the fuse bit
  Changing the fuse bit CKDIV8 to un-programmed, changes the microcontroller's internal clock from 1 MHz to 8 MHz. Because of this, the trigger signal generated from the microcontroller does not meet the open window from the window watchdog and a reset is generated.

Figure 2-2. ATA6617 - EK Schematic of the Development Board

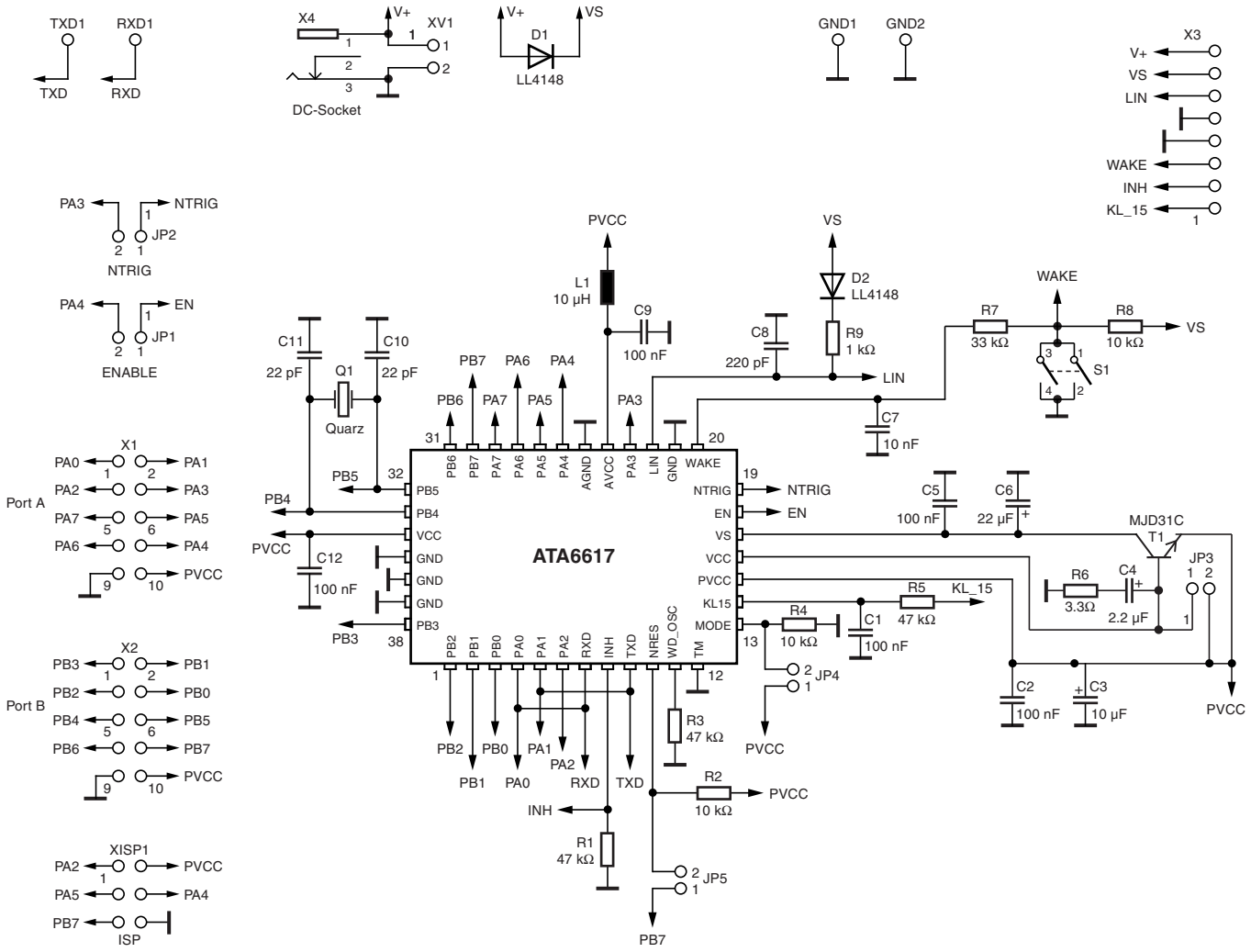
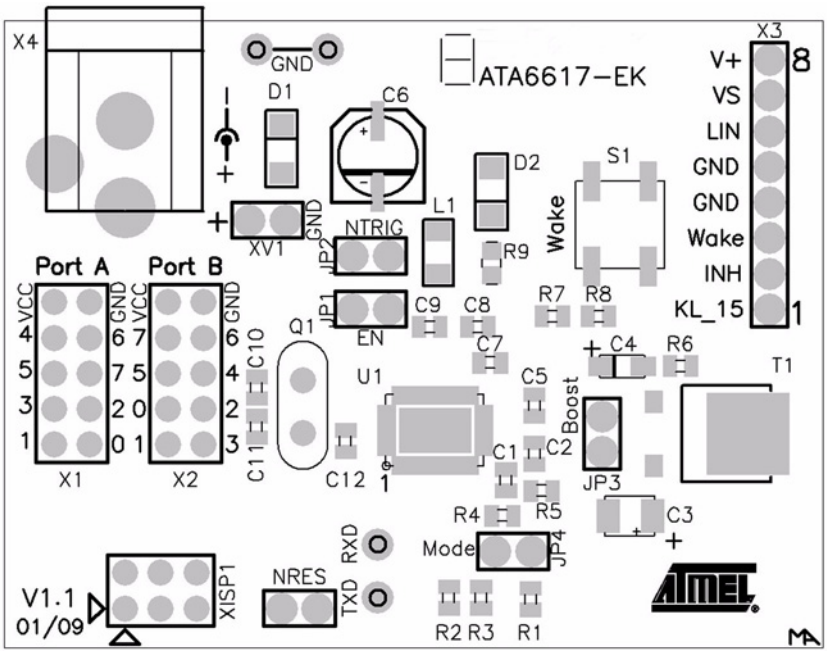


Figure 2-3. ATA6617 - EK Board Component Placement; Top side, Top View



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