Features

- **Low Power CMOS Operation**
  - **100 µA max. Standby**
  - **30 mA max. Active at 5 MHz**
- **Fast Read Access Time - 100 ns**
- **Wide Selection of JEDEC Standard Packages Including OTP**
  - **40-Lead 600-mil Cerdip and OTP Plastic DIP**
  - **44-Pad LCC and OTP PLCC**
- **5 V ± 10% Power Supply**
- **High Reliability CMOS Technology**
  - **2000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Rapid Programming - 100 µs/word (typical)**
- **Two-line Control**
- **CMOS and TTL Compatible Inputs and Outputs**
- **Integrated Product Identification Code**
- **Full Military, Commercial and Industrial Temperature Ranges**

1 Megabit (64K x 16) UV Erasable CMOS EPROM

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Description

The AT27C1024 is a low-power, high performance 1,048,576 bit Ultraviolet Erasable and Electrically Programmable Read Only Memory (EPROM) organized 64K x 16. It requires only one 5-V power supply in normal read mode operation. Any word can be accessed in less than 100 ns, eliminating the need for speed reducing WAIT states. The by-16 organization make this part ideal for high-performance 16 and 32 bit microprocessor systems.

In read mode, the AT27C1024 typically consumes 15 mA. Standby mode supply current is typically less than 10 µA.

The AT27C1024 come in a choice of industry standard JEDEC-approved packages including; 40-pin DIP in ceramic or one time programmable (OTP) plastic, and 44-pad ceramic leadless chip carrier (LCC), or OTP plastic J-leaded chip carrier (PLCC). All devices feature two line control ($\overline{CE}$, $\overline{OE}$) to give designers the flexibility to prevent bus contention.

With high density 64K word storage capability, the AT27C1024 allow firmware to be stored reliably and to be accessed by the system without the delays of mass storage media.

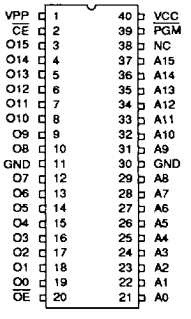
Atmel's 27C1024 have additional features to ensure high quality and efficient production use. The Rapid Programming Algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100 µs/word. The Integrated Product Identification Code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

Pin Configurations

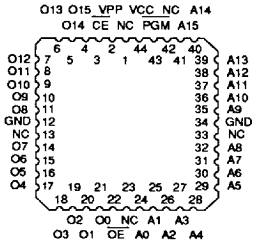
Pin Name	Function
A0-A15	Addresses
O0-O15	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{PGM}$	Program Strobe
NC	No Connect

Note: Both GND pins must be connected.

CDIP, PDIP Top View



LCC, JLCC, PLCC Top View

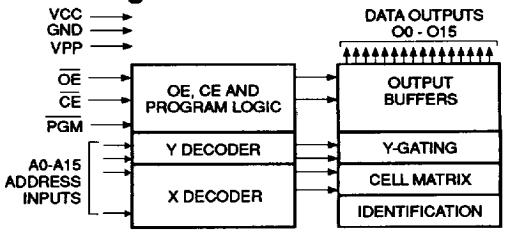


Note: PLCC Package Pins 1 and 23 are DON'T CONNECT.

Erasure Characteristics

The entire memory array of the AT27C1024 is erased (all outputs read as V_{OH}) after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15 W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable EPROM which will be subjected to continuous fluorescent indoor lighting or sunlight.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on A9 with Respect to Ground	-2.0 V to +14.0 V(1)
V_{PP} Supply Voltage with Respect to Ground	-2.0 V to +14.0 V(1)
Integrated UV Erase Dose	7258 W•sec/cm^2

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes:
1. Minimum voltage is -0.6 V dc which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC}+0.75 V dc which may overshoot to +7.0 V for pulses of less than 20 ns.

Operating Modes

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	Ai	V_{PP}	V_{CC}	Outputs
Read	V_{IL}	V_{IL}	X(1)	Ai	X	V_{CC}	D_{OUT}
Output Disable	X	V_{IH}	X	X	X	V_{CC}	High Z
Standby	V_{IH}	X	X	X	X(5)	V_{CC}	High Z
Rapid Program(2)	V_{IL}	V_{IH}	V_{IL}	Ai	V_{PP}	V_{CC}	D_{IN}
PGM Verify	V_{IL}	V_{IL}	V_{IH}	Ai	V_{PP}	V_{CC}	D_{OUT}
PGM Inhibit	V_{IH}	X	X	X	V_{PP}	V_{CC}	High Z
Product Identification(4)	V_{IL}	V_{IL}	X	A9=V_H (3) A0=V_{IH} or V_{IL} A1-A15=V_{IL}	V_{CC}	V_{CC}	Identification Code

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to Programming characteristics.
3. $V_H = 12.0 \pm 0.5$ V.
4. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.
5. Standby V_{CC} current (I_{SB}) is specified with V_{PP}=V_{CC}. V_{CC} > V_{PP} will cause a slight increase in I_{SB}.

D.C. and A.C. Operating Conditions for Read Operation

		AT27C1024			
		-10	-12	-15	-20
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.		-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 5%	5 V ± 10%	5 V ± 10%	5 V ± 10%

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D.C. and Operating Characteristics for Read Operation

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = -0.1 V to V_{CC}+1 V			5	µA
I_{LO}	Output Leakage Current	V_{OUT} = -0.1 V to V_{CC}+0.1 V			10	µA
I_{PP1} (2)	V_{PP} (1) Read/Standby Current	V_{PP} = 3.8 to V_{CC}+0.3 V			10	µA
I_{SB}	V_{CC} (1) Standby Current	I_{SB1} (CMOS) $\overline{CE}$ = V_{CC}-0.3 to V_{CC}+1.0 V			100	µA
		I_{SB2} (TTL) $\overline{CE}$ = 2.0 to V_{CC}+1.0 V			1	mA
I_{CC}	V_{CC} Active Current	f = 5 MHz, I_{OUT} = 0 mA, $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.,Mil.		40	mA
V_{IL}	Input Low Voltage			-0.6	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+ 0.75	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.45	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA		V_{CC}-0.3		V
		I_{OH} = -2.5 mA		3.5		V
		I_{OH} = -400 µA		2.4		V

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.

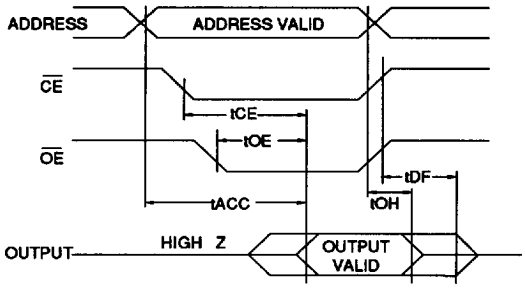
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}.

A.C. Characteristics for Read Operation

				AT27C1024								
				-10		-12		-15		-20		
Symbol	Parameter	Condition		Min	Max	Min	Max	Min	Max	Min	Max	Units
t_{ACC} (3)	Address to Output Delay	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	Com.		100		120		150		200	ns
			Ind.,Mil.				120		150		200	ns
t_{CE} (2)	$\overline{CE}$ to Output Delay	$\overline{OE}$ = V_{IL}			100		120		150		200	ns
t_{OE} (2,3)	$\overline{OE}$ to Output Delay	$\overline{CE}$ = V_{IL}			30		35		65		75	ns
t_{DF} (4,5)	$\overline{OE}$ High to Output Float	$\overline{CE}$ = V_{IL}			30		30		40		55	ns
t_{OH}	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, whichever occurred first	$\overline{CE}$ = $\overline{OE}$ = V_{IL}		0		0		0		0		ns

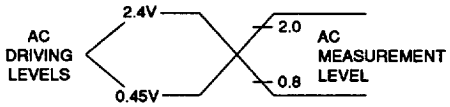
Notes: 2, 3, 4, 5. - see AC Waveforms for Read Operation.

A.C. Waveforms for Read Operation [1]



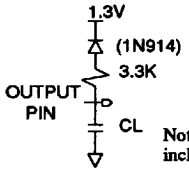
Notes:
1. Timing measurement references are 0.8 V and 2.0 V. Input AC driving levels are 0.45 V and 2.4 V, unless otherwise specified.
2. $\overline{OE}$ may be delayed up to t_{CE}-t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE}.
3. $\overline{OE}$ may be delayed up to t_{ACC}-t_{OE} after the address is valid without impact on t_{ACC}.
4. This parameter is only sampled and is not 100% tested.
5. Output float is defined as the point when data is no longer driven.

Input Test Waveforms and Measurement Levels



t_R, t_F < 20 ns (10% to 90%)

Output Test Load



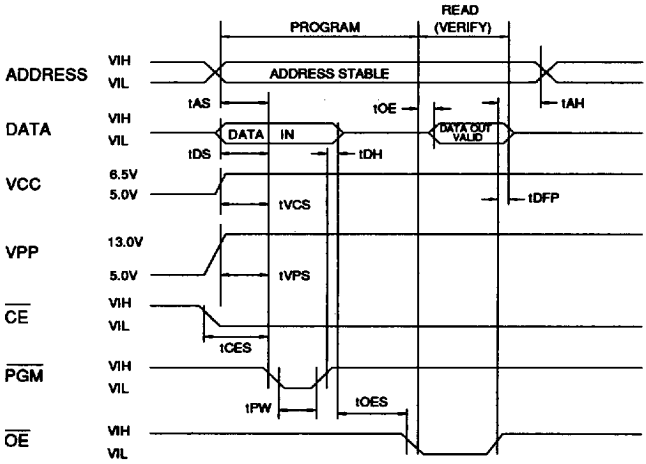
Note: C_L = 100 pF including jig capacitance.

Pin Capacitance (f = 1 MHz T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Notes: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Programming Waveforms [1]



Notes:
1. The Input Timing Reference is 0.8 V for V_{IL} and 2.0 V for V_{IH}.
2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
3. When programming the AT27C1024 a 0.1-µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

D.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions	Limits Min	Limits Max	Units
I_{LI}	Input Load Current	$V_{IN}=V_{IL},V_{IH}$		10	µA
V_{IL}	Input Low Level	(All Inputs)	-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC}+0.3$	V
V_{OL}	Output Low Volt.	$I_{OL}=2.1$ mA		.45	V
V_{OH}	Output High Volt.	$I_{OH}=-400$ µA	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			50	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE}=\overline{PGM}=V_{IL}$		30	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

A.C. Programming Characteristics

$T_A = 25 \pm 5°C$, $V_{CC} = 6.5 \pm 0.25$ V, $V_{PP} = 13.0 \pm 0.25$ V

Symbol	Parameter	Test Conditions* (see Note 1)	Limits Min	Limits Max	Units
t_{AS}	Address Setup Time		2		µs
t_{CES}	$\overline{CE}$ Setup Time		2		µs
t_{OES}	$\overline{OE}$ Setup Time		2		µs
t_{DS}	Data Setup Time		2		µs
t_{AH}	Address Hold Time		0		µs
t_{DH}	Data Hold Time		2		µs
t_{DFP}	$\overline{OE}$ High to Output Float Delay	(Note 2)	0	130	ns
t_{VPS}	V_{PP} Setup Time		2		µs
t_{VCS}	V_{CC} Setup Time		2		µs
t_{PW}	$\overline{PGM}$ Program Pulse Width	(Note 3)	95	105	µs
t_{OE}	Data Valid from $\overline{OE}$			150	ns

*A.C. Conditions of Test:

Input Rise and Fall Times (10% to 90%) ..... 20 ns
Input Pulse Levels ..... 0.45 V to 2.4 V
Input Timing Reference Level ..... 0.8 V to 2.0 V
Output Timing Reference Level ..... 0.8 V to 2.0 V

Notes:

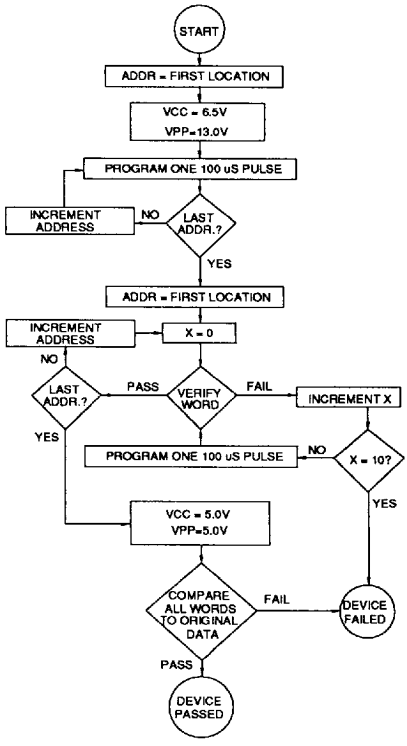
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven — see timing diagram.
3. Program Pulse width tolerance is 100 µsec ± 5%.

Atmel's 27C1024 Integrated Product Identification Code

Codes	Pins A0	015-08	O7	O6	O5	O4	O3	O2	O1	O0	Hex Data
Manufacturer	0	0	0	0	0	1	1	1	1	0	001E
Device Type	1	0	1	1	1	1	0	0	0	1	00F1

Rapid Programming Algorithm

A 100 µs $\overline{PGM}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5 V and V_{PP} is raised to 13.0 V. Each address is first programmed with one 100 µs $\overline{PGM}$ pulse without verification. Then a verification / reprogramming loop is executed for each address. In the event a word fails to pass verification, up to 10 successive 100 µs pulses are applied with a verification after each pulse. If the word fails to verify after 10 pulses have been applied, the part is considered failed. After the word verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0 V and V_{CC} to 5.0 V. All words are read again and compared with the original data to determine if the device passes or fails.



Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
100	30	0.1	AT27C1024-10DC AT27C1024-10KC AT27C1024-10LC	40DW6 44KW 44LW	Commercial (0°C to 70°C)
120	30	0.1	AT27C1024-12DC AT27C1024-12JC AT27C1024-12KC AT27C1024-12LC AT27C1024-12PC	40DW6 44J 44KW 44LW 44P6	Commercial (0°C to 70°C)
120	40	0.1	AT27C1024-12DI AT27C1024-12JI AT27C1024-12KI AT27C1024-12LI AT27C1024-12PI	40DW6 44J 44KW 44LW 44P6	Industrial (-40°C to 85°C)
			AT27C1024-12DM AT27C1024-12KM AT27C1024-12LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-12DM/883 AT27C1024-12KM/883 AT27C1024-12LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	30	0.1	AT27C1024-15DC AT27C1024-15JC AT27C1024-15KC AT27C1024-15LC AT27C1024-15PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
150	40	0.1	AT27C1024-15DI AT27C1024-15JI AT27C1024-15KI AT27C1024-15LI AT27C1024-15PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)
			AT27C1024-15DM AT27C1024-15KM AT27C1024-15LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-15DM/883 AT27C1024-15KM/883 AT27C1024-15LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT27C1024-20DC AT27C1024-20JC AT27C1024-20KC AT27C1024-20LC AT27C1024-20PC	40DW6 44J 44KW 44LW 40P6	Commercial (0°C to 70°C)
200	40	0.1	AT27C1024-20DI AT27C1024-20JI AT27C1024-20KI AT27C1024-20LI AT27C1024-20PI	40DW6 44J 44KW 44LW 40P6	Industrial (-40°C to 85°C)

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
200	40	0.1	AT27C1024-20DM AT27C1024-20KM AT27C1024-20LM	40DW6 44KW 44LW	Military (-55°C to 125°C)
			AT27C1024-20DM/883 AT27C1024-20KM/883 AT27C1024-20LM/883	40DW6 44KW 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
120	60	0.1	5962-86805 06 QX 5962-86805 06 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
150	60	0.1	5962-86805 05 QX 5962-86805 05 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
170	60	0.1	5962-86805 04 QX 5962-86805 04 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	60	0.1	5962-86805 03 QX 5962-86805 03 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	60	0.1	5962-86805 02 QX 5962-86805 02 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)
300	60	0.1	5962-86805 01 QX 5962-86805 01 XX	40DW6 44LW	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Package Type	
40DW6	40 Lead, 0.600" Wide, Windowed, Ceramic Dual Inline Package (Cerdip)
44J	44 Lead, Plastic J-Leaded Chip Carrier OTP (PLCC)
44KW	44 Lead, Windowed, Ceramic J-Leaded Chip Carrier (JLCC)
44LW	44 Pad, Windowed, Ceramic Leadless Chip Carrier (LCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline package OTP (PDIP)