T-46-23-08

GigaBit Logic **12G014**

# 256x4 Bit Registered, Self-Timed Static RAM 2.5 ns Cycle Time

# 12G NanoRAM™ Family

## FEATURES

- Nanosecond access and cycle times
- Fully registered architecture with 3 selectable output modes provides maximum usable speed
- Equal read and write cycle times
- Internally generated write pulse eliminates need for narrow write pulse
- Register mode output for fast access with minimum cycle time
- Latch mode output for fast access with extended cycle
- Single-ended or differential clock input
- ECL and 10G PicoLogic™ Family compatible
- Temperature & voltage compensated design
- Source follower outputs permit wire-or capability
- Available in C-leaded or leadless chip carriers or in die form

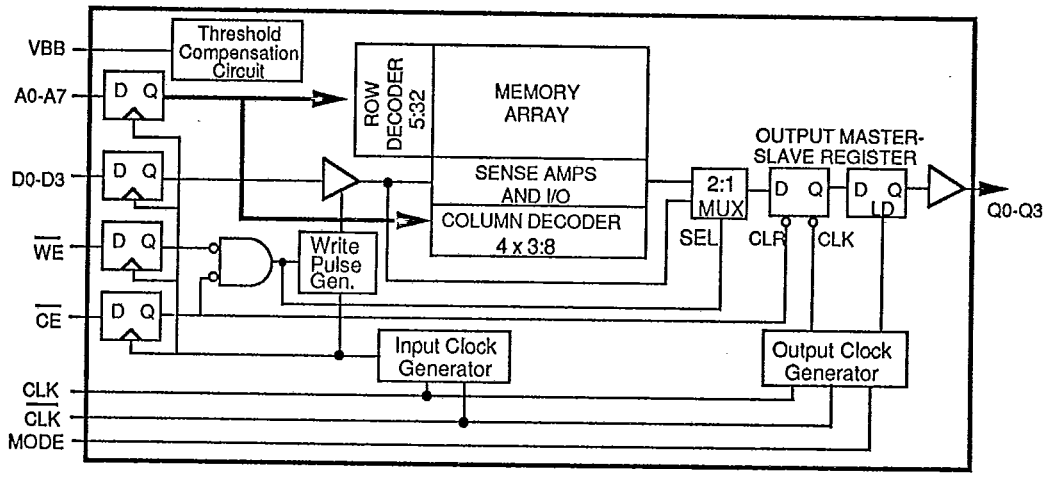
## FUNCTIONAL DESCRIPTION

The 12G014 is an ultra-high speed 1024 bit synchronous, registered Random Access Memory, organized as 256 words by 4 bits. The device is designed for ultra- high speed cache and buffer storage applications (See App. Note #5 for description of a 1Kx16-bit memory subsystem). The innovative architecture of the NanoRam™ Family incorporates the functions of a traditional static RAM along with on-chip, fully pipelined, latched inputs and outputs, an internally generated write pulse, and a single clock to deliver maximum usable device speed in system applications.

The 12G014 RAM input and output levels are ECL and 10G PicoLogic Family compatible. A VBB input pin is provided for direct voltage and/or temperature compensation tracking with ECL interface circuitry. The device has source follower outputs to allow simple wire-OR expansion.

The 12G014 is packaged in a JEDEC outline leadless or C-leaded chip carrier and is fabricated using GigaBit's high volume GaAs MESFET process technology.

## BLOCK DIAGRAM




| 12G014 ORDERING INFORMATION | | |
|---|---|---|
| PACKAGE TYPE | Register Mode R/W Cycle Time | |
| | 2.5 ns | 3.5 ns |
| 40 pin C-leaded CC<br>40 pin Leadless CC<br>Unpackaged dice | 12G014-2C<br>12G014-2L | 12G014-3C<br>12G014-3L<br>12G014-3X |

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| SYMBOL | PIN DESCRIPTIONS |
|---|---|
| A0 - A7 | Address Inputs: Lines A0 - A2 are column addresses. Lines A3 - A7 are row addresses. At the rising edge of Clock these lines determine the memory address state information. |
| $\overline{CE}$ | Chip Enable: At the rising edge of Clock this line determines the enable state of the device. Chip Enable LOW activates the function and output of the memory. Chip Enable HIGH deactivates the memory and its output. |
| $\overline{WE}$ | Write Enable: At the rising edge of CLOCK this line determines the read or write state of the device. Write Enable HIGH activates a read cycle. Write Enable LOW activates a self-timed write cycle. |
| CLK | Clock Input True: provides the basic timing of the memory device. All inputs are latched on the rising edge of Clock which defines the initiation of a new memory cycle. |
| $\overline{CLK}$ | Clock Input Complement: provides an optional differential input for systems with differential Clock distribution. For single ended Clock distribution, CLK is tied to the Vbb input pin (nom. -1.3V). |
| MODE | Mode: sets the output mode of the device. When the Mode pin is tied to Vss the output operates in the Register Mode. When the Mode pin is tied to Vddl the output operates in the Latch Mode. When the Mode Pin is tied to Vcc the output operates in the Transparent Mode. |
| D0 - D3 | Data In: at the rising edge of Clock during a Write Cycle these lines determine the data input state information to be written into the addressed memory location. |
| Q0 - Q3 | Data Out: these lines provide the valid data output from a Read Cycle and input data written from a Write Cycle. In the Register Mode, the pipelined Data Out is activated by the rising edge of Clock. In the Latch Mode, the non-pipelined Data Out is activated by the falling edge of Clock. |
| VCC | VCC: + 5.0 Volt power supply pin. |
| VDDL | VDDL: ground supply pin for the memory circuitry. |
| VDDO | VDDO: ground supply pin for the output drivers. |
| VSS | VSS: - 3.4 Volt power supply pin. |
| VEE | VEE: - 5.2 Volt power supply pin. |
| VTTC | VTTC: the AC return pin for the package internal Vddo decoupling capacitor. Vttc is not brought onto the 12G014 circuit, and is typically tied to Vtt (nominally -2.0V). |
| VBB | VBB: ECL Threshold Reference Voltage Input (Nominal - 1.3 V) provided to allow direct tracking of an ECL logic family's Vbb reference voltage. Must be tied to a nominal - 1.3 V when interfacing to 10G PicoLogic circuitry (or to the VBBS supply pin of a PicoLogic device). |
| DNC | DNC: Do Not Connect. Reserved for future use. |

## POWER SUPPLY SEQUENCING

Power to the device should be applied first to VEE and then to VSS and VCC. When powering down, power should first be removed from VSS and VCC, then from VEE. During power up and power down sequencing, absolute maximum ratings apply.

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## DEVICE DESCRIPTION

### NanoRam Architecture

The NanoRam architecture provides a fully registered, clocked, static memory operation. This architecture is optimized for ultra high speed memory applications requiring nanosecond access and cycle times. A single clock establishes the simple synchronous timing for the device. The rising edge of Clock determines the start of each memory cycle and controls the registered inputs and outputs.

### Registered Inputs

All input state information, including Addresses, Write Enable, Chip Enable, and Data In are latched into the on-chip pipeline registers at the rising edge of Clock to begin a new cycle. The setup times and hold times relative to the rising edge of Clock are the same for all inputs and controls. Once the input and control signals have been latched on-chip, they may begin transition to another state for the next cycle. This allows considerable time for address and control signals to propagate across an array of memory devices without slowing the memory cycle timing.

### Output Modes

The MODE pin determines the function of the 12G014's output register. When the MODE pin is strapped to Vss, the output operates in the fully pipelined REGISTER MODE. In this mode, the Data Out remains valid for the entire memory cycle and transitions only at the next rising edge of the Clock. This allows sufficient time for the data output signals to propagate across an array of memory devices without slowing memory cycle timing. Register Mode operation offers the fastest possible cycle time operation of the NanoRam memory in a system application.

When the Mode pin is strapped to Vddl, the output operates in the Latch Mode. In this mode, the non-pipelined Data Out is fed through on the falling edge of Clock in the current cycle and latched on the next rising edge of Clock. This allows the data output to appear without waiting for the next rising edge of Clock. Latch Mode operation offers the flexibility to achieve the fastest possible memory access time with output latches in system applications with extended cycle time.

When the Mode Pin is strapped to Vcc, the output operates in the Transparent Mode. In this mode, the data from the memory array appears at the output pins as soon as it is available from the memory array through the sense amplifiers. The input registers are unaffected by the state of the Mode Pin, with the rising edge of the clock loading them and starting the memory cycle.

For all modes of operation during write cycles, the data being written is also routed directly from the data input register to the output register where it appears as valid data out. This simplifies system design by eliminating the appearance of invalid or indeterminate states on the output pins. The Data Out drivers are source followers to allow wire-OR configurations.

### Output Master/Slave Register Operation

The output M/S register is controlled by the Clock and the Mode control and operates as follows:

| Mode C'ntl | Master Reg. | Slave Reg. |
|---|---|---|
| = Vss (Register) | Transparent when clock is low | Transparent when clock is high |
| = Vddl (Latch) | " " " | Always transparent |
| = Vcc (Transparent) | Always transparent | Always transparent |

### Clock Options

The Clock input is differential to provide optimum sensitivity and noise immunity. If it is driven from a single-ended clock source, the $\overline{CLK}$ input must be tied to a nom. -1.3V reference. This reference voltage is available on pin VBBS if a PicoLogic device is used to drive the Clock input. All specifications in this data sheet assume the rising edge of CLK as the active edge. If $\overline{CLK}$ is used instead (with CLK tied to a nom. -1.3V source), all timimg diagrams should be referenced to the clock edge opposite to that shown. The sum of Clock high and Clock low pulse widths is considerably less than total cycle time allowing ample time for clock transitions in practical systems. The Clock duty cycle may be asymmetrical within the limits allowed by the minimum clock pulse width specifications.

### ECL and PicoLogic Family Compatibility

All 12G014 inputs are ECL and PicoLogic I/O level compatible. The Vbb input pin allows the input logic threshold to be controlled by the driving logic family, thereby compensating for mismatches in threshold due to temperature and power supply variation, resulting in high system noise immunity. If PicoLogic is used to drive the 12G014, the Vbb pin should be connected to the VBBS pin of a driving PicoLogic device. If the 12G014 is driven from ECL logic, the Vbb pin should be connected to the VBB threshold reference voltage derived from the driving ECL logic family.

### Power Supply Sequencing

Power to the device should be applied first to Vee and then to Vss and Vcc. When powering down, power should first be removed from Vss and Vcc, then from Vee. During power up and power down sequencing, the absolute maximum ratings apply.

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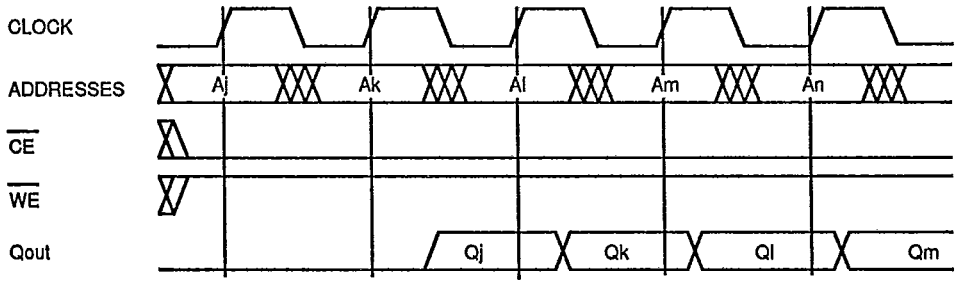
## DEVICE DESCRIPTION

### Register Mode Read Cycle

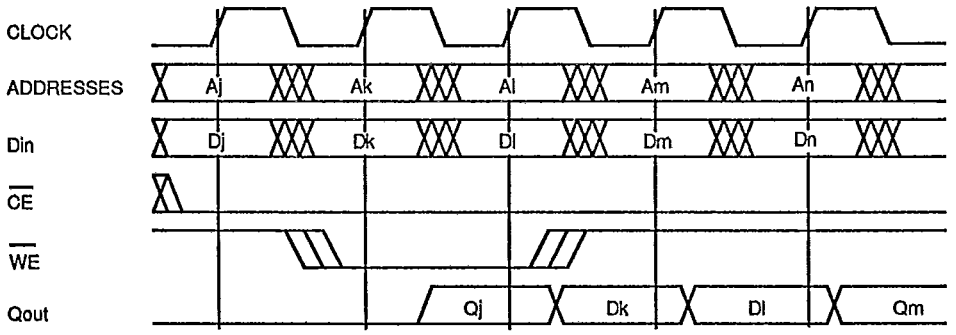
The MODE pin is strapped to Vss for all Register Mode operations. The Read Cycle in the Register Mode is performed by presenting a Write Enable ($\overline{WE}$) HIGH and valid Addresses to the input registers prior to the rising edge of Clock. The Jth memory access takes place during the present Clock cycle and valid Jth cycle read data is presented to the on-chip output registers. At the next rising edge of Clock the Kth memory cycle is started and the valid Jth cycle read data is loaded into the output registers, propagates through the output drivers and appears at Data Out where it is held for a full cycle. Successive Read Cycles proceed in a fully pipelined manner where each rising edge of Clock loads the input registers with the valid state for the present memory cycle while the output registers are loaded with read data from the previous cycle.




### Register Mode Write Cycle

The MODE pin is strapped to Vss for all Register Mode operations. The Jth Write Cycle in the Register Mode is performed by presenting a Write Enable ($\overline{WE}$) low and valid Addresses to the input registers prior to the rising edge of Clock. No write pulse is required. The Jth memory write takes place totally self-timed during the present Clock cycle and valid Jth cycle write data is presented to the on-chip output registers. At the next rising edge of clock, the Kth memory cycle is started and valid Jth cycle write data is loaded into the output registers and appears at the Data Out pins where it is held for a full cycle. Successive Write Cycles proceed in a fully pipelined manner with each successive rising edge of Clock.

Write Cycles have timing parameters identical to Read Cycles. Any combination of Read Cycles and Write Cycles can be performed in succession with identical pipelined timing.



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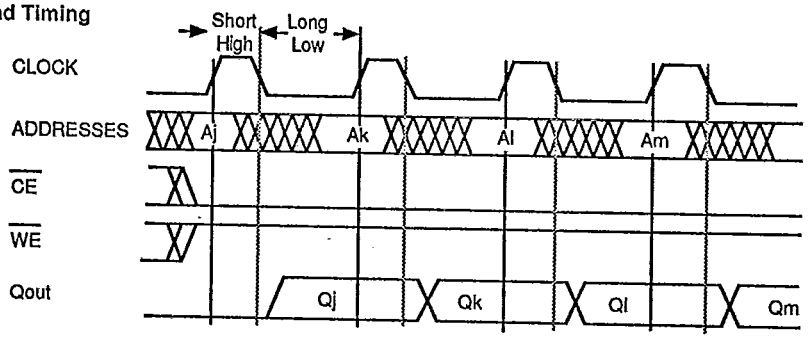
## DEVICE DESCRIPTION

### Latch Mode Read and Write Cycles

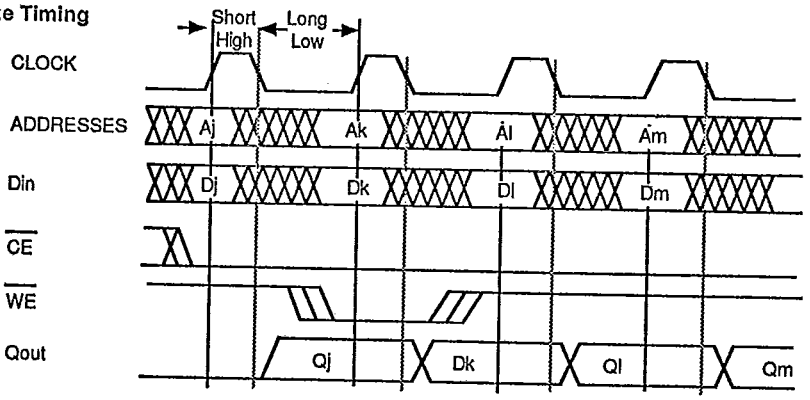
The MODE pin is strapped to Vddl for all Latch Mode operations. The Jth read cycle in Latch Mode is performed by presenting the same pipelined inputs prior to the rising edge of Clock as for the Register Mode read cycle. The Jth memory access takes place during the present clock cycle. At the falling edge of Clock within the cycle, the output latch becomes transparent and allows valid Jth cycle read data to appear at Data Out. At the next rising edge of Clock, the Kth memory cycle is started and valid Jth cycle read data is held until the next falling edge of Clock. Latch Mode operation is typically used to achieve a fast access time in applications with extended cycle times. To achieve the fastest possible access time in Latch Mode, the Clock is operated asymmetrically. The clock is held HIGH for a minimum time and brought LOW to allow valid read data from the present cycle to appear at Data Out as soon as possible. The Clock is then held LOW for the remainder of the extended cycle.

The Kth Write Cycle in Latch Mode is performed by presenting the same pipelined inputs prior to the rising edge of Clock as for the Register Mode Write Cycle. Valid Kth cycle write data appears at Data Out at the falling edge of Clock in the present cycle. At the next rising edge of Clock the Lth memory cycle is started and valid Kth cycle write data is held until the next falling edge of Clock. Latch Mode Write Cycles have timing parameters identical to Latch Mode Read Cycles. Any combination of Read Cycles and Write Cycles can be performed in succession with identical timing.

### Latch Mode Read Timing




### Latch Mode Write Timing



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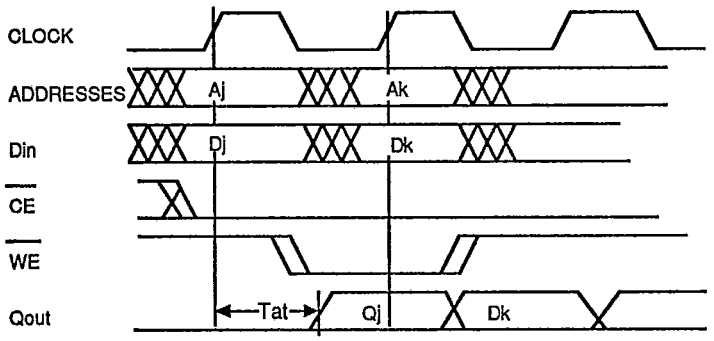
## DEVICE DESCRIPTION

**Transparent Mode Read and Write Cycles**

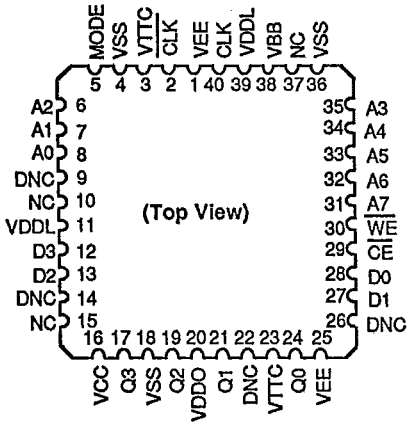
The MODE pin is strapped to Vcc for all transparent mode operations. The Jth read or write cycle is performed by presenting the appropriate Write Enable signal and valid addresses to the input registers prior to the rising edge of Clock. No write pulse is required during a write operation.

The Jth memory cycle takes place during the present Clock cycle and valid read or write data is presented to the output pins through the output registers which are held transparent in this mode. Successive cycles are initiated with each subsequent rising clock edge.



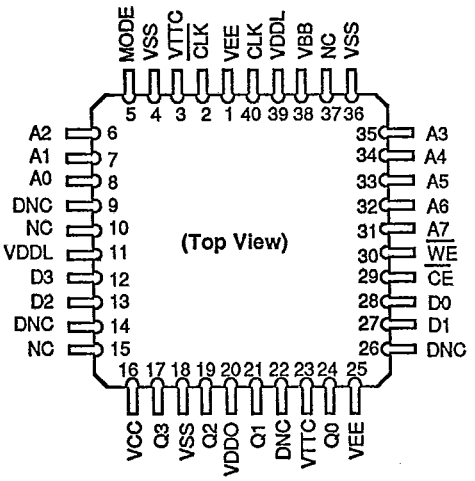

## PIN FUNCTION DIAGRAMS

**PACKAGE TYPE "L"**




NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = do not connect.

**PACKAGE TYPE "C"**




NOTES: Pin 1 is marked for orientation. N/C = No Connection. DNC = do not connect.

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## ABSOLUTE MAXIMUM RATINGS (Notes 1, 5)

(Beyond which useful life may be impaired)

| SYMBOL | PARAMETER | ABSOLUTE MAXIMUM RATINGS | NOTES |
|---|---|---|---|
| Tstor | Storage Temperature | -65 °C to +150 °C | |
| TJ | Junction Temperature | -55 °C to +150 °C | |
| Tc | Case Temperature Under Bias | -55 °C to + 125 °C | 2 |
| Vcc | Supply Voltage | - 0.5 V to + 6.0 V | |
| Vddo | Output Driver Supply Voltage | Vss to + 1.0 V | |
| Vbb | ECL Reference Voltage | -4.0 V to +0.5 V | |
| Ibb | Input current (from interfacing family) | -0.5 mA to +1.0 mA | |
| Vss | Supply Voltage | - 4.0 V to + 0.5 V | |
| Vee | Supply Voltage | - 7.0 V to Vss - 1.0 V | |
| Vin | Voltage Applied to Any Input; Continuous Vcc = 5.0, Vss = - 3.4 V, Vee = - 5.2 V | - 4.0 V to + 0.5 V | |
| I in | Current Into Any Input; Continuous | - 0.5 mA to 1.0 mA | |
| Vout | Voltage Applied to Any Output | - 4.0V to +7.0 V | 3 |
| Iout | Current From Any Output; Continuous | -100 mA | 3 |
| Pd | Total Power Dissipation Tc = 85° C | 3.9 W | 4 |
| Pout | Power Dissipation Per Output Pout = (Vddo-Vout) x Iout | 100 mW | |
| Vttc | Vddo Internal Decoupling Cap. Return | - 6.0 V to Vddo | |
| Vtt | Load Termination Supply | - 6.0 V to Vddo + 6.0 V | 3 |

NOTES:
1. All voltages specified with Vddl defined as 0 V. Positive current flows into the device.
2. Tc is measured at case top.
3. Subject to power dissipation limitations.
4. Total power dissipation is the limit of the package power dissipation. The operating power dissipation of the device is specified under DC Characteristics.
5. Sustained application of Vss or Vcc in the absence of Vee may result in excessive power dissipation and damage to the device.

## RECOMMENDED OPERATING CONDITIONS (Note 1)

| SYMBOL | PARAMETER | MIN | NOM | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Tc | Case Operating Temperature | 25 | | 85 | ℃ | 3 |
| Vcc | Supply Voltage | 4.75 | 5.0 | 5.25 | V | |
| Vddl | Logic Supply Voltage | | Gnd | | V | |
| Vddo | Output Driver Supply Voltage | -0.8 | Gnd | 1.0 | V | |
| Vbb | ECL Reference Voltage | | - 1.3 | | V | |
| Vss | Supply Voltage | - 3.6 | - 3.4 | - 3.2 | V | |
| Vee | Supply Voltage | - 5.5 | - 5.2 | - 4.9 | V | |
| Vttc | Vddo Internal Decoupling Return | Vss | Vtt | Vddo | V | |
| Vtt | Load Termination Supply Voltage | Vss | - 2.0 | - 1.8 | V | 2 |
| Rload | Output Termination Load Resistance | 25 | 50 | 100 | Ω | 2 |

NOTES:
1. All voltages are specified with respect to Vddl and Vddo, which are grounded.
2. The Rload and Vtt combination used is subject to maximum output current and output power restrictions.
3. This operating temperature can be maintained with a heat sink and air flow as determined by using Application Note 3. Tc measured at case top. ***HEATSINKING IS REQUIRED.***

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## DC CHARACTERISTICS (note 5)

TEST CONDITIONS: Tc =25 °C to 85 °C, VCC = 4.75 to 5.25V, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd, Output load = 50Ω to VTT = - 2.0 V, clock input edge rate ≤ 2 ns.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | TEST CONDITIONS | NOTES |
|---|---|---|---|---|---|---|---|
| Voh | Output Voltage High | - 0.7 | -0.4 | -0.3 | V | | |
| Vol | Output Voltage Low | Vtt | -1.9 | - 1.8 | V | | |
| Ioh | Output Current High | | -70 | -60 | mA | Voh = - 0.7 V | 1 |
| Iol | Output Current Low | | 0.01 | 10 | µA | Vol = -1.8V | |
| Vih | Input Voltage High | - 1.0 | | Vddl | V | Vbb = - 1.3 V | 2 |
| Vil | Input Voltage Low | -2.0 | | - 1.6 | V | Vbb = - 1.3 V | 2,3 |
| Iin | Logic Input Current | -100 | 10 | 100 | uA | -1.8 V ≤ Vin ≤ -0.7 V | |
| Imode | Mode Input Current | | | 1.0 | mA | Vss ≤ Vmode ≤ Vcc | |
| Ibb | Vbb Input Current | -500 | | 500 | uA | Vbb = -1.3 V | |
| Iss | Power Supply Current | -460 | -290 | | mA | | |
| Iee | Power Supply Current | -140 | -100 | | mA | | |
| Icc | Power Supply Current | | 160 | 200 | mA | | |
| Pd | Power Dissipation | | 2.3 | 3.3 | W | | 4 |

NOTES:

1. Ioh is the maximum current the output can source under any Rload and Vtt combination.
2. The input threshold is referenced to the Vbb input. Therefore Vih and Vil will track the Vbb input.
3. Inputs may be connected to Vss (-3.4V) to establish a logic low level.
4. Measured at nominal supply voltages and 50% output duty cycle. Excludes Vddo output source follower power (typically 10 mW per loaded output).
5. For proper operation, the clock input edge rate should be ≤ 2 ns.

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## 12G014 - 2 AC CHARACTERISTICS (Note 1)

Test Conds.: Tc = 25°C to 85°C, VCC = 4.75 to 5.25, VSS = -3.6V to -3.2V, VEE = -5.5V to -4.9V, VDDL=VDDO = Gnd.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **ALL MODES, READ AND WRITE CYCLES** | | | | | | |
| Tclkh | Clock High Pulse Width | 1000 | | | ps | |
| Tclkl | Clock Low Pulse Width | 1000 | | | ps | |
| Ts | Input Setup Time | -400 | | | ps | 2 |
| Th | Input Hold Time | 1500 | | | ps | 2 |
| Tr,Tf | Output rise and fall times | | 175 | 250 | ps | 3 |
| **REGISTER MODE, READ AND WRITE CYCLES** | | | | | | |
| Trc | Read/Write Cycle Time | 2500 | | | ps | |
| Tar | Clock Rising Edge to Output Delay | 800 | 1000 | 1200 | ps | |
| **LATCH MODE, READ AND WRITE CYCLES** | | | | | | |
| Tlc | Read/Write Cycle Time | 3800 | | | ps | |
| Tarl | Clock Rising Edge to Output Delay | 2600 | | 3800 | ps | |
| Tafl | Clock Falling Edge to Output Delay | 1200 | 1500 | 1700 | ps | |
| **TRANSPARENT MODE READ AND WRITE CYCLES** | | | | | | |
| Ttc | Read/Write CycleTime | 3800 | | | ps | |
| Tat | Clock Rising Edge to Output Delay | 2600 | | 3800 | ps | |

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| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **ALL MODES, READ AND WRITE CYCLES** | | | | | | |
| Tclkh | Clock High Pulse Width | 1250 | | | ps | |
| Tclkl | Clock Low Pulse Width | 1250 | | | ps | |
| Ts | Input Setup Time | -100 | | | ps | 2 |
| Th | Input Hold Time | 1800 | | | ps | 2 |
| Tr,Tf | Output Rise and Fall Times | | 200 | 300 | ps | 3 |
| **REGISTER MODE, READ AND WRITE CYCLES** | | | | | | |
| Trc | Read/Write Cycle Time | 3500 | | | ps | |
| Tar | Clock Rising Edge to Output Delay | 800 | 1400 | 1700 | ps | |
| **LATCH MODE, READ AND WRITE CYCLES** | | | | | | |
| Tlc | Read/Write Cycle Time | 4500 | | | ps | |
| Tarl | Clock Rising Edge to Output Delay | 3300 | | 4500 | ps | |
| Tafl | Clock Falling Edge to Output Delay | 1300 | 1600 | 2000 | ps | |
| **TRANSPARENT MODE READ AND WRITE CYCLES** | | | | | | |
| Ttc | Read/Write CycleTime | 4500 | | | ps | |
| Tat | Clock Rising Edge to Output Delay | 3300 | | 4500 | ps | |

NOTES:

1. AC test conditions, unless otherwise stated:
   VBB = -1.3V, Rload = 50Ω to VTT = -2.0V, VIH = -0.8V, VIL = -1.8V, edge rate (all inputs) = 400 ps measured between 20% and 80% points. All delays measured between 50% points of signal transitions.
2. Measured from the rising edge of the clock input between 50% points.
3. Output rise and fall times are measured at the 20% and 80% points of the transition from VOL max. to VOH min.

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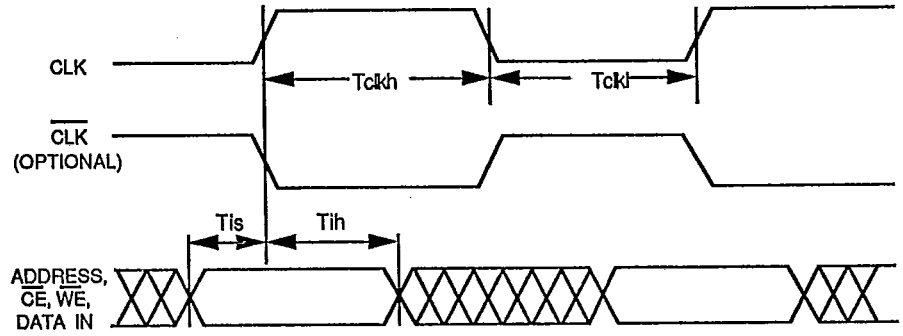
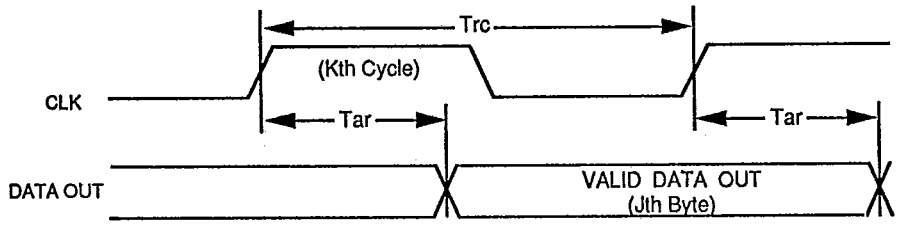
## SWITCHING WAVEFORMS

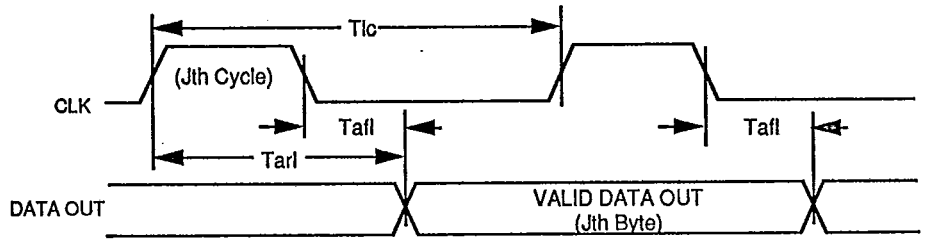
### ALL MODES, READ AND WRITE CYCLES



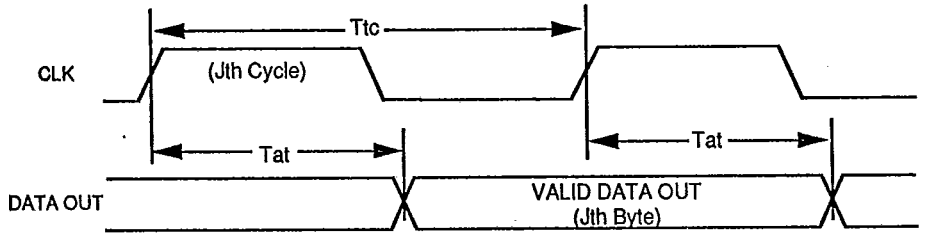

### REGISTER MODE, READ AND WRITE CYCLES




### LATCH MODE, READ AND WRITE CYCLES




### TRANSPARENT MODE, READ AND WRITE CYCLES



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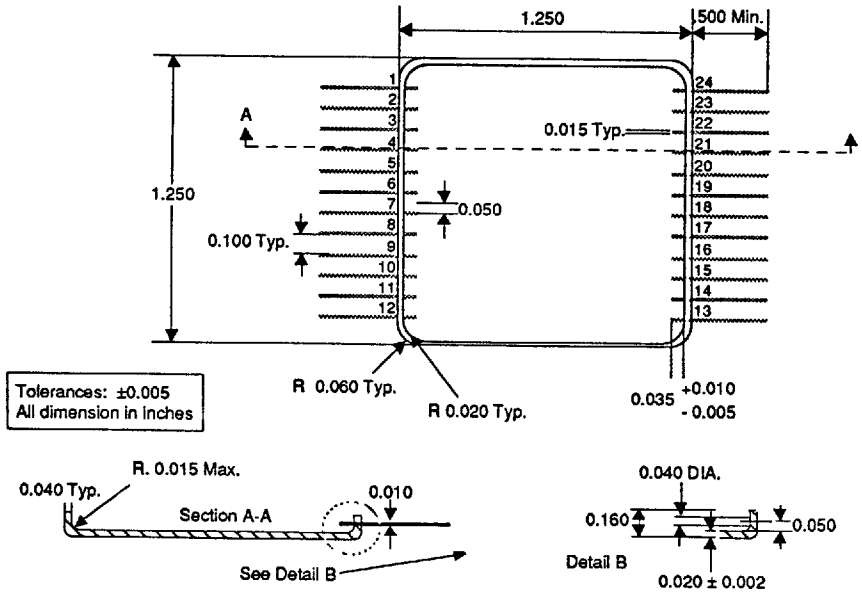
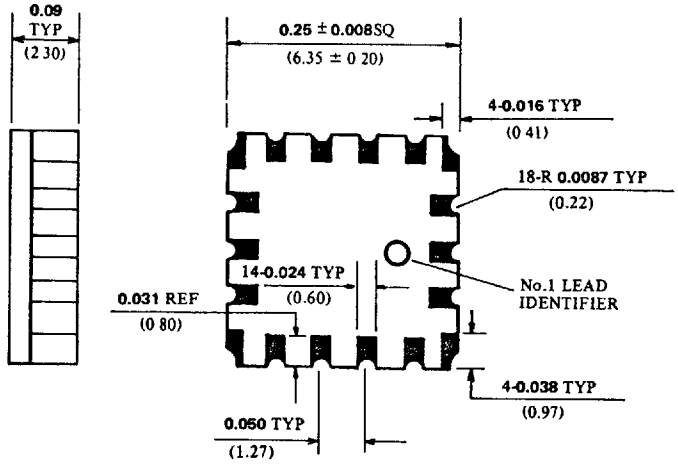
# 24 PIN METAL FLATPACK
# 18 PIN PACKAGE

## 24 PIN METAL FLATPACK
Type H




## 18 PIN LEADLESS CHIP CARRIER
TYPE L1




All dimensions shown in inches and (millimeters)

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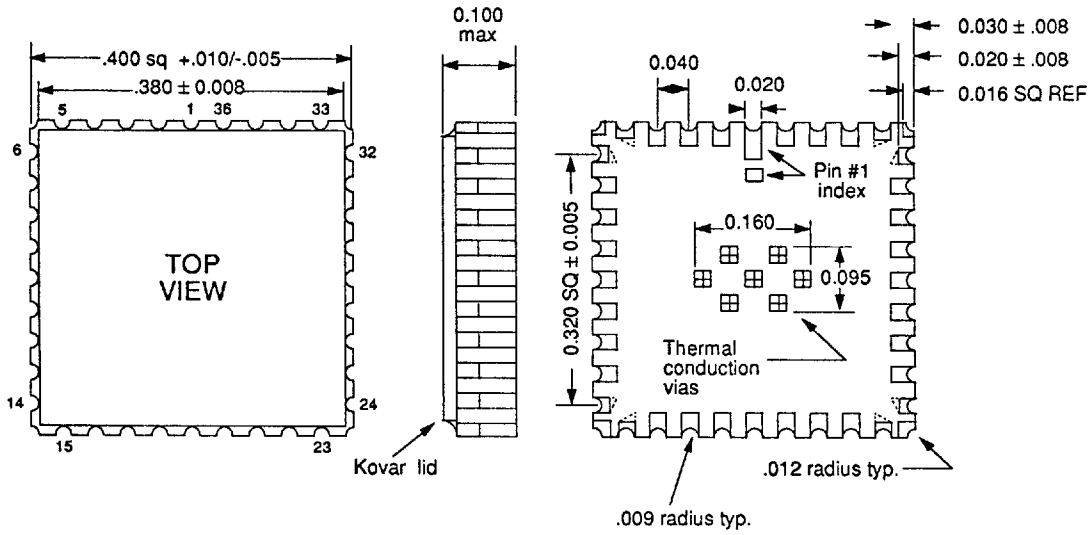
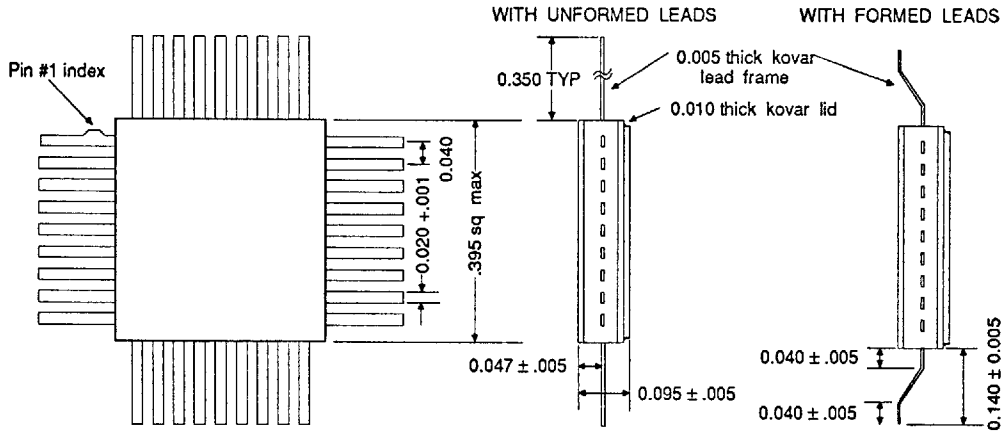
# 36 PIN PACKAGES

## 36 PIN LEADLESS CHIP CARRIER
TYPE L36




NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

## 36 I/O LEAD FLATPACK
TYPE F



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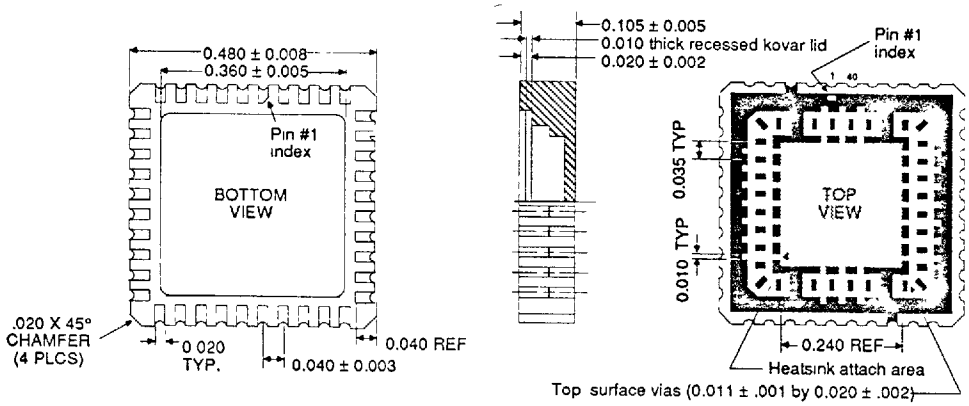
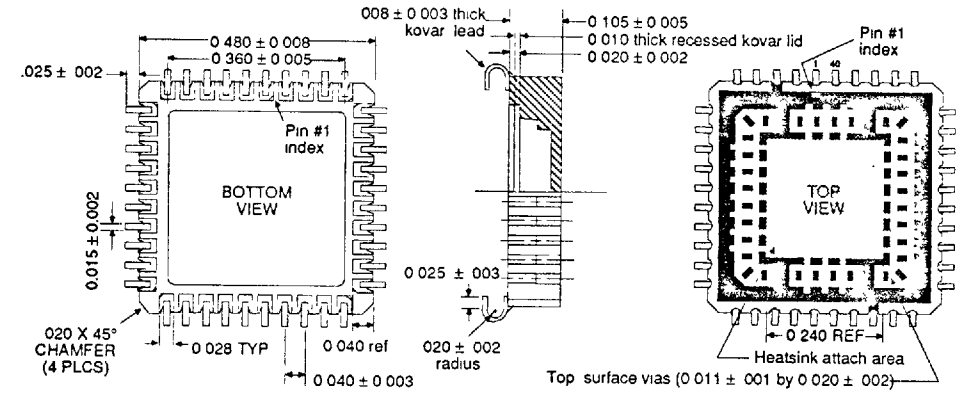
# 40 PIN PACKAGES

## 40 PIN LEADLESS CHIP CARRIER
TYPE L

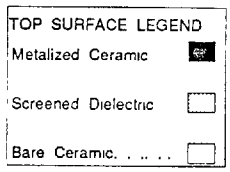



## 40 PIN LEADED CHIP CARRIER
TYPE C

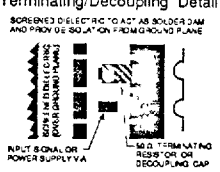



NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width




Top Surface Terminating/Decoupling Detail



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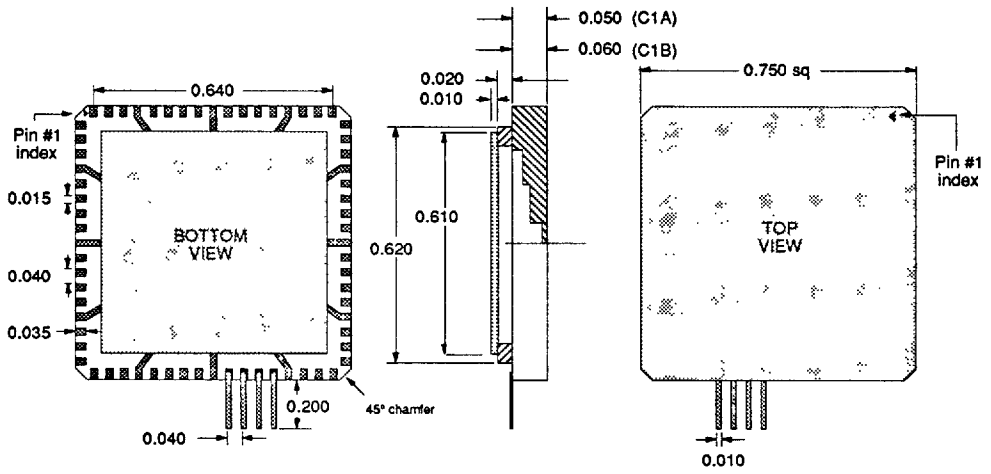
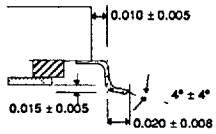
# 68 & 132 PIN PACKAGES

## 68 PIN LEADED CHIP CARRIER
### TYPE C1




1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS




## 132 PIN LEADED CHIP CARRIER
### TYPE C3