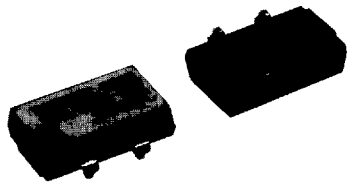
SaRonix

Crystal Clock Oscillator — ACMOS, TTL, Tri-State, SMD

Technical Data — STA / STT Series, Type F



ACTUAL SIZE

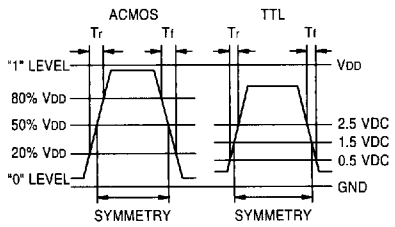
Description

A crystal controlled oscillator to drive HCMOS and NMOS microprocessors. This ACMOS device is capable of driving both HCMOS and TTL loads at high frequencies. The tri-state function enables the output to go high impedance. The surface mountable J-leaded plastic package is ideal for automated assembly.

Applications & Features

- Ideally suited for high speed graphics, CISC and RISC processors, and custom ASIC's
- Compact Surface Mountable package
- Matches EIA standard SO-J-20 footprint
- High frequency up to 135 MHz
- ACMOS, HCMOS and TTL compatible
- Tri-state output
- Output is short-circuit protected
- Also available as 3.3V version, see separate data sheet

Output Waveform



Frequency Range:	70 MHz to 135 MHz		
Frequency Stability:	±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.		
Temperature Range:			
Operating:	0°C to +70°C		
Storage:	-55°C to +125°C		
Supply Voltage:			
Operating:	+5 VDC ±10%		
Absolute Maximum:	+7 VDC		
Supply Current at 5V:	typ mA	max @ 25°C mA	max over temp mA
70 - 80 MHz:	45	55	60
80 - 135 MHz:	55	65	70
Output Drive:			
ACMOS			
Symmetry:	@ 0.5 VDD, see Part Numbering Guide on Page 2		
Rise & Fall Times:	20% to 80% VDD, see Part Numbering Guide		
Logic 0:	10% VDD max		
Logic 1:	90% VDD min		
Output Load:	50Ω AC load		
TTL			
Symmetry:	@ 1.5V level, see Part Numbering Guide on Page 2		
Rise & Fall Times:	0.5 to 2.5V, see Part Numbering Guide		
Logic 0:	0.5V max		
Logic 1:	2.5V min		
Sink & Source Current:	50mA max		
Mechanical:			
Shock:	MIL-STD-883, Method 2002, Condition B		
Solderability:	MIL-STD-883, Method 2003		
Terminal Strength:	MIL-STD-202, Method 211, Conditions A and C		
Vibration:	MIL-STD-883, Method 2007, Condition A		
Solvent Resistance:	MIL-STD-202, Method 215		
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition B		
Environmental:			
Thermal Shock:	MIL-STD-883, Method 1011, Condition A		
Moisture Resistance:	MIL-STD-883, Method 1004		

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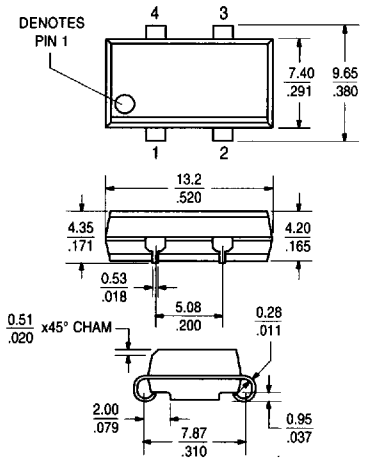
Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic "1" or NC	Oscillation
Logic "0" or GND	High Impedance

Required Input Levels on Pin 1:
Logic "1" = 2.5V min
Logic "0" = 0.6V max

Package Details

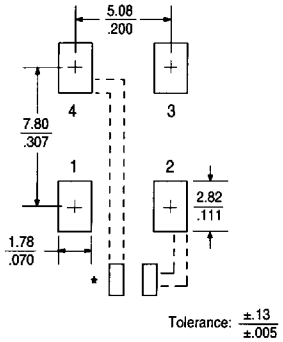


Pin Function:

Pin 1: Tri-State Control **Pin 3:** Output
Pin 2: GND **Pin 4:** +5 VDC

Standard Marking Format

Recommended Land Pattern



Tolerance: $\frac{\pm.13}{\pm.005}$

* External high frequency power supply decoupling recommended.

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

STA 0 8 F C - 100.0000

Series
STA = ACMOS
STT = TTL - compatible

Symmetry
0 = Symmetry 50% ±10%
A = Symmetry 50% ±5%
(available at some frequencies, consult factory)

Frequency Range
2 = TTL 1.0 nsec Rise/fall, 2.0 nsec max (consult factory)
3 = TTL 0.5 nsec Rise/fall, 1.0 nsec max (Standard for TTL)
8 = ACMOS 2.5 nsec Rise/fall, 3.5 nsec max (consult factory)
9 = ACMOS 1.8 nsec Rise/fall, 2.0 nsec max (Standard for ACMOS)

Package Style
F = J - Lead

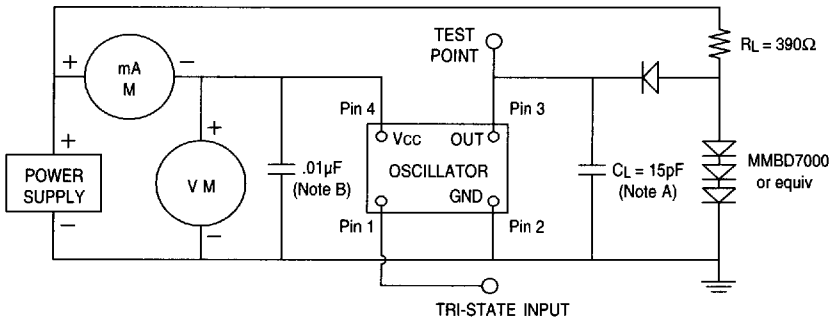
Stability Tolerance
B = ±50 ppm (0.005%)
C = ±100 ppm (0.010%)

Logic
R = Reverse Logic Tri-state Address Option (up to 120 MHz)

Frequency

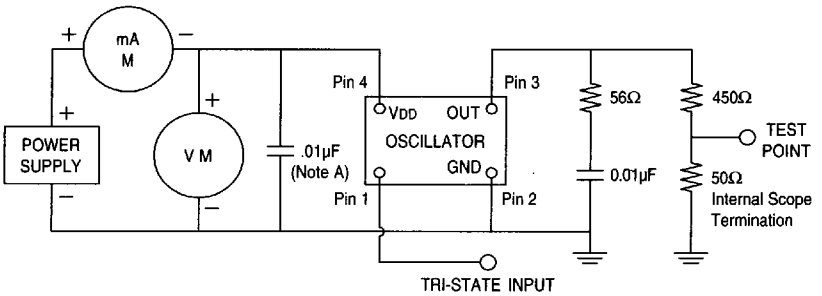
Example P/N: STA08FC - 80.0000

Test Circuits



NOTE: A. CL includes probe and fixture capacitance.
NOTE: B. An external .01µF bypass capacitor close to package ground and Vcc pin is recommended.

FIGURE 1 - TTL TEST CIRCUIT (STT)



NOTE: A. An external .01µF bypass capacitor close to package ground and Vcc pin is recommended.

FIGURE 2 - ACMOS TEST CIRCUIT (STA)

All specifications are subject to change without notice.

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