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A TDK Group Company

SSI 32F8011/8012
Programmable Electronic Filter

T-64-05

November 1991

3

DESCRIPTION

The SSI 32F8011/8012 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, Bessel–type, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programmability, combined with low group delay variation makes the SSI 32F8011/8012 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

The SSI 32F8011/8012 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

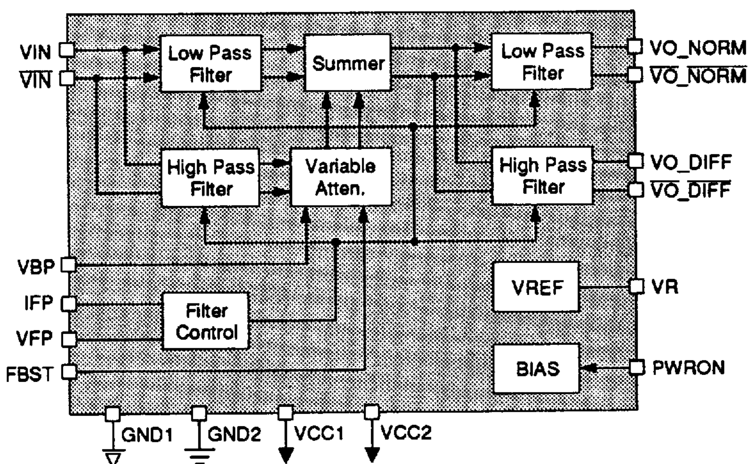
The SSI 32F8011/8012 requires only a +5V supply and is available in 16-pin DIP, SON, and SOL packages.

Note: SSI 32F8011 is in full production; SSI 32F8012 is in preliminary status. Samples of both are available.

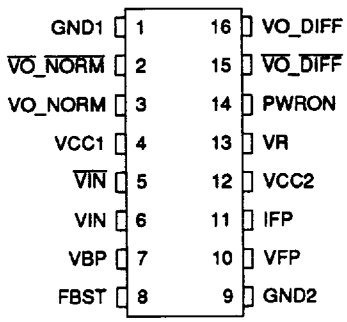
FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **cellular telephone applications**
  - **radio**
  - **data acquisition**
  - **LAN**
- **Programmable filter cutoff frequency (SSI 32F8011 f_c = 5 to 13 MHz) (SSI 32F8012 f_c = 6 to 15 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±0.75 ns group delay variation from 0.2 f_c to f_c = 13 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-pin DIP, SON, and SOL package**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8011/8012 Programmable Electronic Filter

T-64-05

FUNCTIONAL DESCRIPTION

The SSI 32F8011/8012, a high performance programmable electronic filter, provides a low pass Bessel-type seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4622 Combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The programmable electronic filter can be set to a filter cutoff frequency from 5 to 13 MHz (with no boost) for SSI 32F8011 and 6 to 15 MHz for SSI 32F8012.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8011/8012 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8011/8012. This reference voltage is an internally generated bandgap reference, which typically varies less than 1% over supply voltage and temperature variation.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•IVFP•2.2/VR

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•IVFP•2.2/VR
where IFP and IVFP are in mA, $0.31 < IFP < 0.8$ mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8011/8012 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•2.2/(3•Rx)

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•2.2/(3•Rx)
where Rx is in ohms, $0.917 < Rx < 2.366$ kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where $0 < VBP < VR$.

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T-64-05

3

PIN DESCRIPTION

NAME	DESCRIPTION
VIN, $\overline{VIN}$	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM, $\overline{VO\_NORM}$	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF, $\overline{VO\_DIFF}$	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level or open circuit enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature, Tj	+130	°C
Supply Voltage, VCC1, VCC2	-0.5 to 7	V
Voltage Applied to Inputs	-0.5 to VCC + 0.5	V
IFP, VFP Inputs Maximum Current*	≤1.2	mA

* Exceeding this current may cause frequency programming lockup.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS	UNIT
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50	V
Ambient Temperature	0 < Ta < 70	°C

SSI 32F8011/8012 Programmable Electronic Filter

ELECTRICAL CHARACTERISTICS

Power Supply Characteristics (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
ICC Power Supply Current	PWRON ≤ 0.8V	VBP = VR		14	17	mA
		VBP = 0V		12	15	mA
ICC Power Supply Current	PWRON ≥ 2.0V			67	80	mA

DC Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VIH High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL Low Level Input Voltage		-0.3		0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			−1.5	mA

Filter Characteristics

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
FCA Filter *fc* Accuracy	using VFP pin Rx = 0.917 kΩ	32F8011	11.7		14.3	MHz
		32F8012	13.5		16.5	MHz
AO VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8		1.20	V/V
AD VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8AO		1.0AO	V/V
FBA Frequency Boost Accuracy	VBP = VR @ *fc* = 5 MHz		8.5	9.5	10.5	dB
TGD0 Group Delay Variation Without Boost*	*fc* = Max *fc*, VBP = 0V F = 0.2 *fc* to *fc*		−0.75		+0.75	ns
TGDB Group Delay Variation With Boost*	*fc* = Max *fc*, VBP = VR F = 0.2 *fc* to *fc*		−0.75		+0.75	ns
VIF Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc* (no boost)		1.5			Vpp
VOF Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*		1.5			Vpp
RIN Filter Diff Input Resistance			3.0			kΩ
CIN Filter Diff Input Capacitance*					7	pF
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, I*fp* = 0.8 mA, VBP = 0.0V			5.5	6.8	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = 0.0V			2.5	3.6	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			6.0	8.1	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			3.25	4.4	mVRms

* Not directly testable in production, design characteristic.

T-64-05

ELECTRICAL CHARACTERISTICS (continued)

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IO−	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance Single ended	Source Current (IO+) = 1 mA			60	Ω

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VR	Reference Voltage Output		2.0		2.40	V
I_{VR}	Reference Output Source Current				2.0	mA

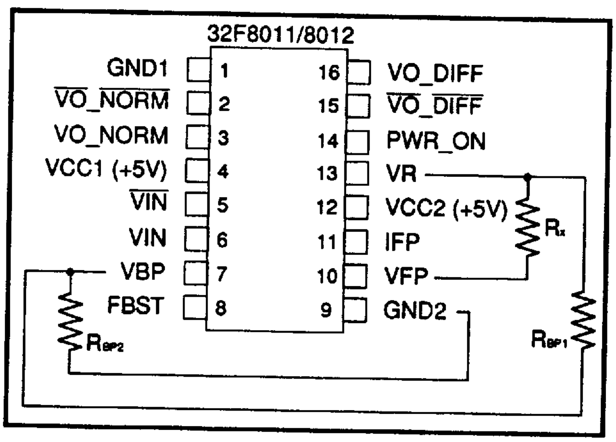


FIGURE 1: 32F8011/8012 Applications Setup, 16-Pin SO or DIP

VR = 2.2V
VFP = 0.667 VR

IVfp = 0.33VR/Rx
IVfp range: 0.31 mA to 0.8 mA
(5 MHz to 13 MHz for SSI 32F8011)
(6 MHz to 15 MHz for SSI 32F8012)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

SSI 32F8011/8012 Programmable Electronic Filter

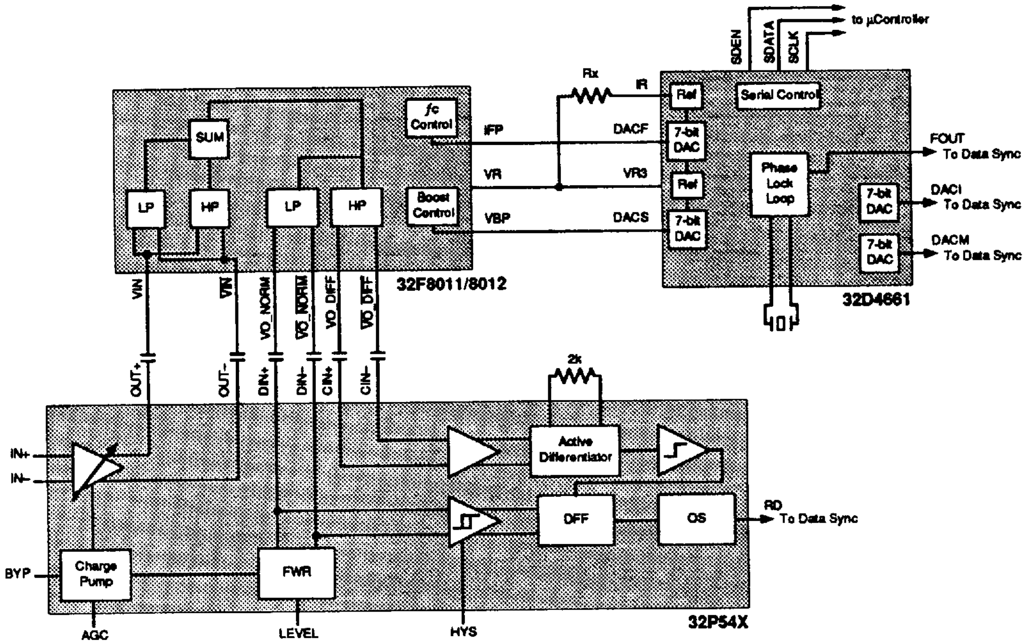


FIGURE 2: Applications Setup, Constant Density Recording 32F8011/8012, 32P54X, 32D4661

IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

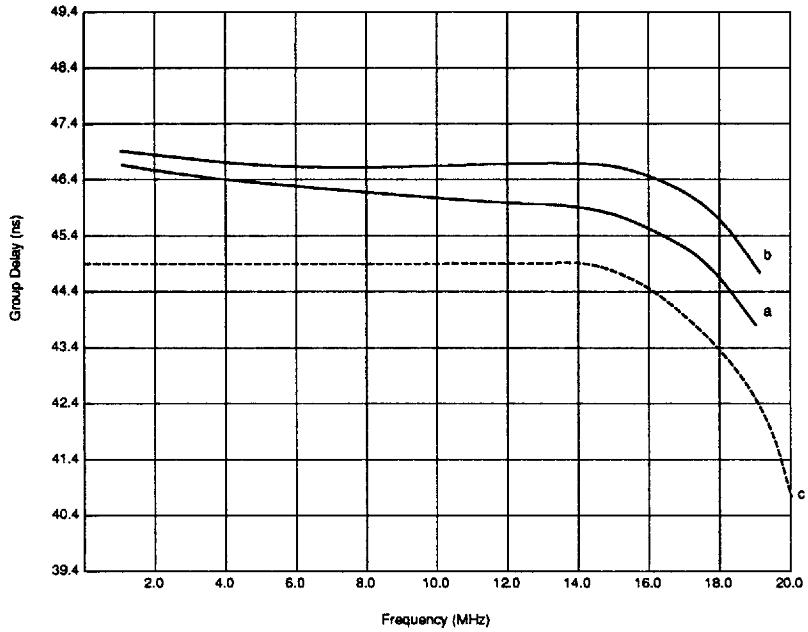
For range of Max *fc* then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

T-64-05



fc = 10.4 MHz

a) No Boost
b) Max Boost
c) Ideal Bessel Filter

3

FIGURE 3: 32F8011/8012 Typical Group Delay Variation (Differentiated Output)

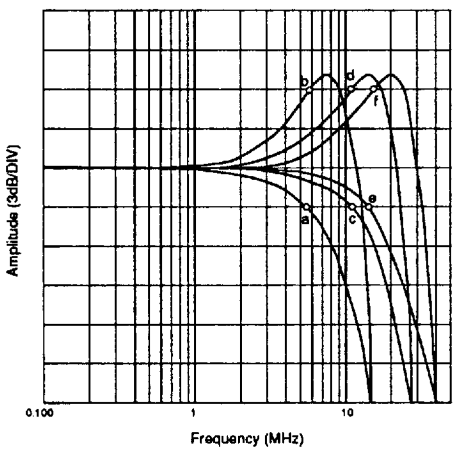


FIGURE 4: 32F8011/8012 Normal Low Pass Output Response (VO_NORM)

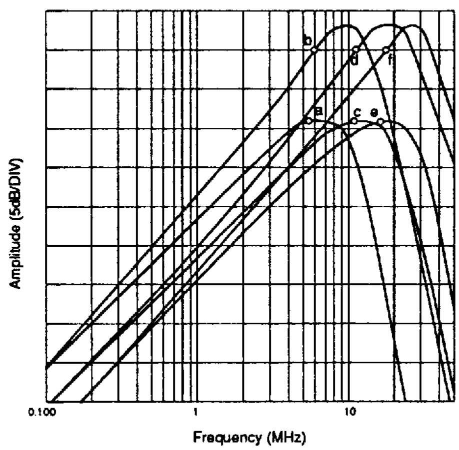
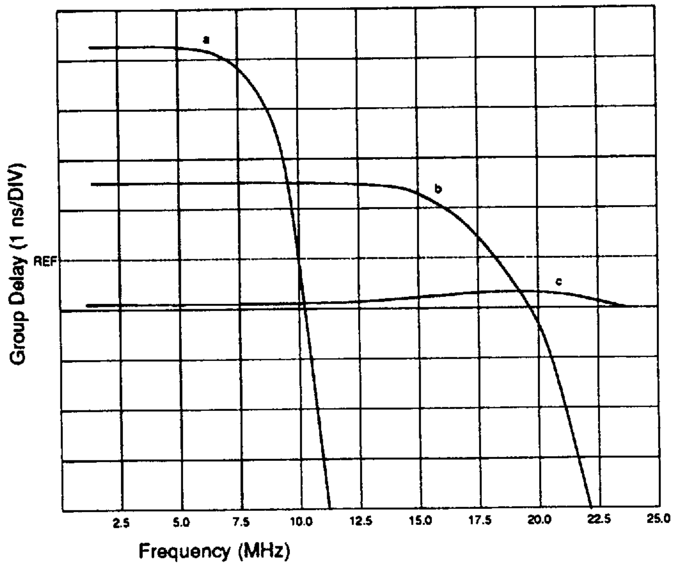


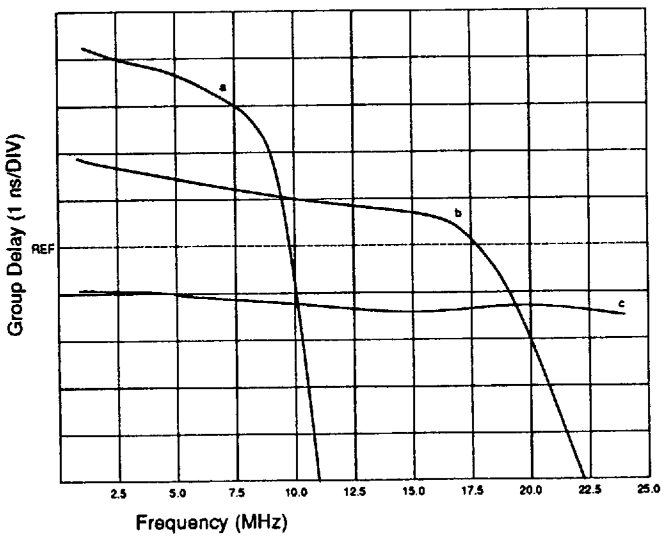
FIGURE 5: 32F8011/8012 Differented Low Pass Output Response (VO_DIFF)

a) *fc* = 5 MHz No Boost
b) *fc* = 5 MHz Max Boost
c) *fc* = 10 MHz No Boost
d) *fc* = 10 MHz Max Boost
e) *fc* = 15 MHz No Boost
f) *fc* = 15 MHz Max Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

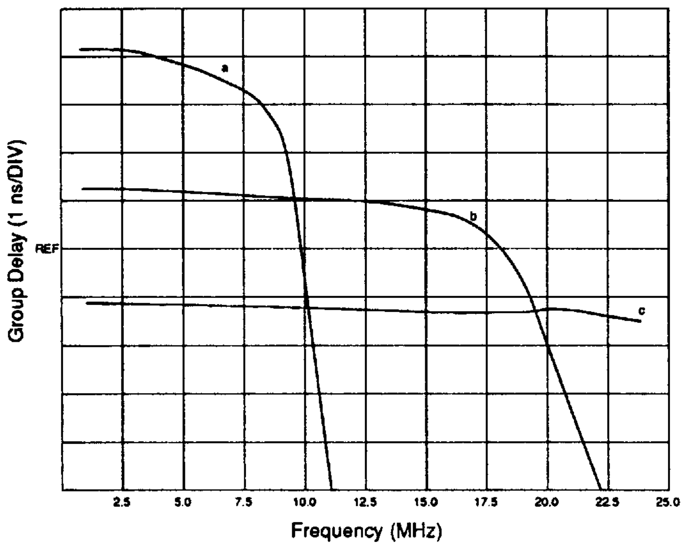
FIGURE 6: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) Maximum Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

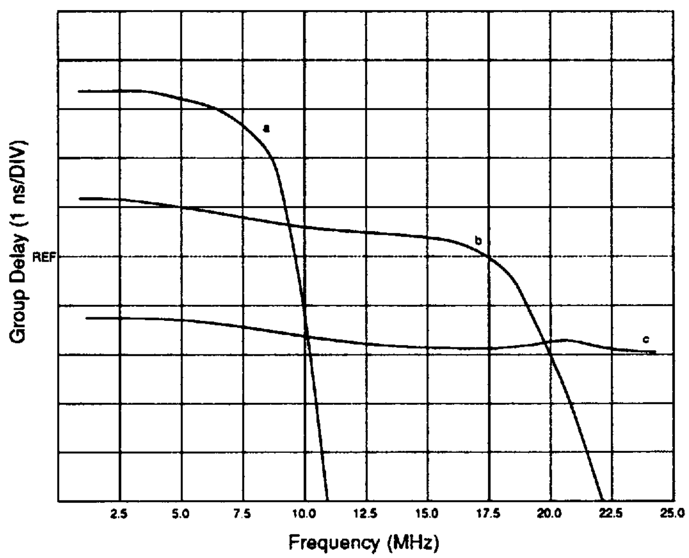
FIGURE 7: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) No Boost

T-64-05



a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

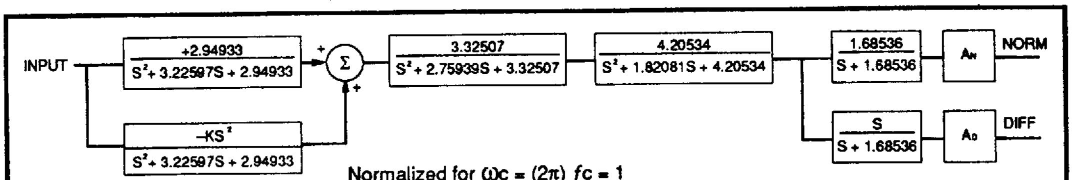
FIGURE 8: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) Maximum Boost



a) *fc* = 5 MHz (Ref = 80 ns)
b) *fc* = 10 MHz (Ref = 45 ns)
c) *fc* = 15 MHz (Ref = 35 ns)

FIGURE 9: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) No Boost

SSI 32F8011/8012 Programmable Electronic Filter



Normalized for $\omega c = (2\pi)\, fc = 1$

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc

Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$

Eq for fc = 13 MHz, $S = S / [(2\pi)(13 \cdot 10^6)] = S / 8.16814^7$

FIGURE 12: 32F8011/8012 Normalized Block Diagram

TABLE 1: 32F8011/8012 Frequency Boost Calculations

Assuming 9.2 dB boost for VBP = VR	Boost	VBP/VR	Boost	VBP/VR
$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right) - 1}{1.884}$	1 dB	0.065	6 dB	0.528
	2 dB	0.137	7 dB	0.658
	3 dB	0.219	8 dB	0.802
	4 dB	0.310	9 dB	0.965
	5 dB	0.413		
or,	**VBP/VR**	**Boost**	**VBP/VR**	**Boost**
boost in dB $\cong 20 \log \left[1.884 \left(\frac{VBP}{VR}\right) + 1\right]$	0.1	1.499 dB	0.6	6.569 dB
	0.2	2.777 dB	0.7	7.305 dB
	0.3	3.891 dB	0.8	7.984 dB
	0.4	4.879 dB	0.9	8.613 dB
	0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost	Boost at fc	f-3 dB/fc	Boost at fc	f-3 dB/fc
	0 dB	1.0	5 dB	2.13
	1	1.2	6	2.28
	2	1.47	7	2.41
	3	1.74	8	2.53
	4	1.95	9	2.65

Notes: 1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented

i.e., fc = 5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 10.65 MHz

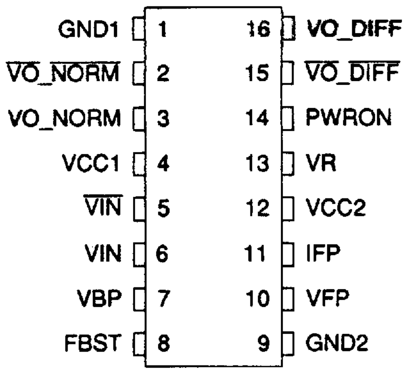
SSI 32F8011/8012 Programmable Electronic Filter

T-64-05

3

PIN DIAGRAM

(Top View)



16-pin DIP, SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W
16-lead PDIP	170° C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8011		
16-lead SON (150 mil)	32F8011-CN	32F8011-CN
16-lead SOL (300 mil)	32F8011-CL	32F8011-CL
16-pin PDIP	32F8011-CP	32F8011-CP
SSI 32F8012		
16-lead SON (150 mil)	32F8012-CN	32F8012-CN
16-lead SOL (300 mil)	32F8012-CL	32F8012-CL
16-pin PDIP	32F8012-CP	32F8012-CP

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Patent Nos. (497,863) (500,778) (516,717)