FOUR PORT BYPASS AND REPEATER FOR FC-AL S2072

FEATURES

- Micropower Bipolar Technology
- ANSI X3T11 Fibre Channel Compliant
- Monolithic Clock Recovery Unit
  - – Retimes & Buffers Received Data
  - – Jitter Peaking < 0.1 dB
- Lock Detect Function
  - – Frequency Detection
- Four Port Bypass Circuits
- Suitable for both Coaxial and Optical Link
- Low Power Operation 0.93 W Typical
- 106.25 or 53.125 MHz Reference Clock
- Compact 10 mm x 10 mm 64 Pin PQFP Package
- 3.3 V Supply

APPLICATIONS

- FC-AL Nodes
- RAID
- JBOD
- SAN

GENERAL DESCRIPTION

The Four Port Bypass and Repeater for FC-AL Circuit is used in full-speed (1.0625 Gb/s) Disk Arrays. It contains a monolithic Clock Recovery Unit (CRU), a lock detect feature and four port bypass circuits. The S2072 may be used to implement a single chip Arbitrated Loop Port Bypass Retiming Node. The S2072 performs the function of four port bypass circuits followed by a Clock and Data Retimer (CDR). The CDR retimes incoming serial data, detects whether a valid signal is present and outputs a low jitter serial data stream.

FUNCTIONAL DESCRIPTION

The S2072 functional block diagram is shown in Figure 1. The S2072 performs two functions. The first function is a Quad Port Bypass Circuit (PBC) for nodes in a FC-AL system. The low jitter accumulation of the port bypass path is essential in these systems. The second function is to restore signal quality in RAID drives using the FC-AL link configuration. The S2072 clock and data recovery PLL provides low jitter transfer peaking and high jitter tolerance. In addition, the lock detect circuit monitors the incoming signals for frequency, which is useful for link performance monitoring and detection of channel present.

Jitter Performance

Input jitter tolerance is defined as the amplitude of frequency dependent, random and deterministic jitter that causes the clock recovery PLL to violate the BER specifications.

The S2072 complies with the minimum jitter tolerance requirements proposed by the Fibre Channel jitter working group when used with differential inputs and outputs as shown in Figure 2. In addition, the S2072 is designed for minimum jitter generation and jitter transfer specifications. This allows the optimum system design for arbitrated loop architectures.

Figure 1. S2072 Functional Block Diagram

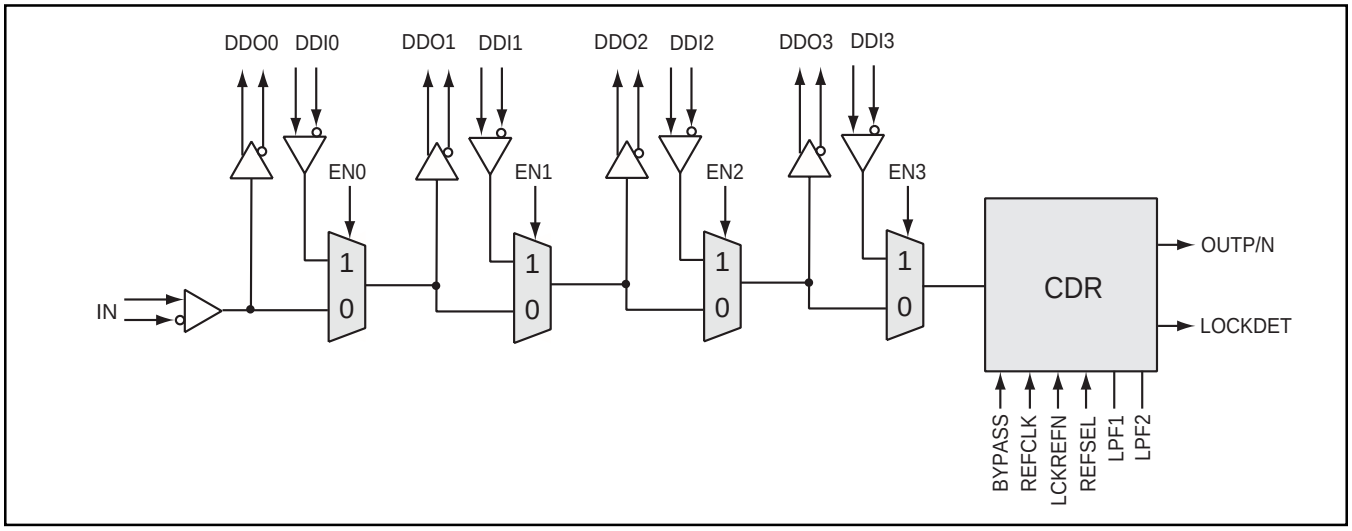
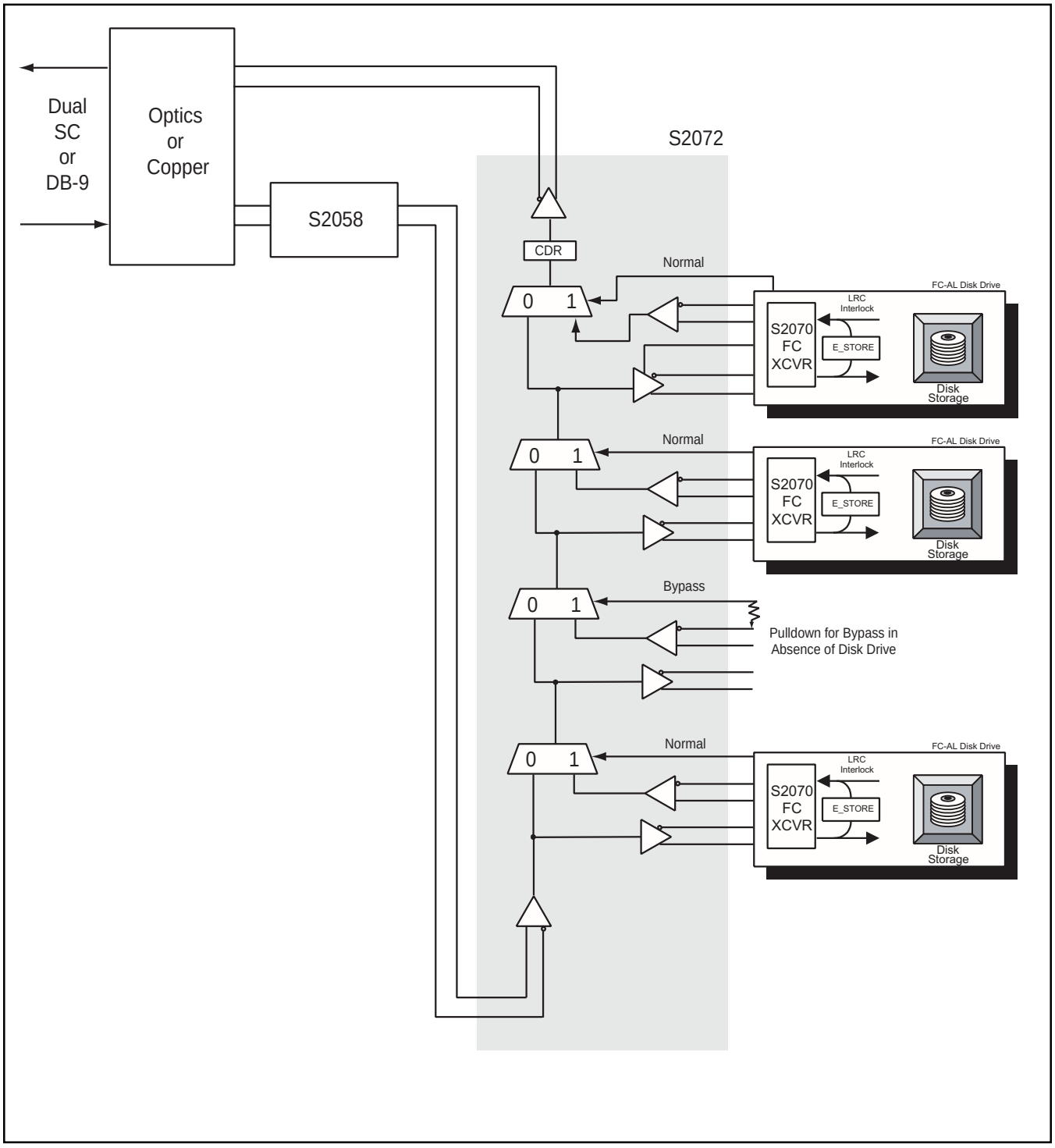


Figure 2. FC-AL JBOD Application for Repeaters



DEVICE DESCRIPTION

The S2072 provides a port bypass function for up to 4 nodes in an FC-AL circuit, with low jitter accumulation. An integrated repeater reduces jitter and restores signal amplitude levels for optimal signal integrity. Jitter performance of the PLL is specified by jitter tolerance and jitter transfer. In accordance with ANSI X3T11, jitter tolerance is divided into random, deterministic, and frequency dependent jitter. Figure 3 illustrates the components of random, deterministic, and frequency dependent jitter that must be tolerated to be ANSI X3T11 compliant.

Frequency Dependent Jitter Tolerance

Frequency Dependent Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes the clock recovery to violate BER specifications. See Figure 4.

Random Jitter Tolerance

Random Jitter Tolerance is the amount of jitter with a gaussian distribution that the clock recovery PLL must tolerate.

Deterministic Jitter Tolerance

Deterministic Jitter Tolerance is the amount of Deterministic jitter that the clock recovery PLL must tolerate.

Jitter transfer

Jitter transfer is defined as the ratio of jitter on the output signal to the jitter applied on the input signal versus frequency. Jitter transfer requirements are shown in Figures 4 and 5. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 4 is applied and the output jitter is measured for compliance to the mask of Figure 5. The jitter transfer mask includes specifications for both jitter peaking and bandwidth.

Lock detect

The S2072 lock detect circuit monitors the selected input signal to detect the presence of the channel. This is done by monitoring the frequency content of the incoming data. The frequency monitor circuit checks the difference between the divided down recovered clock and the externally supplied reference clock (REFCLK). If the frequency difference between the recovered clock and the reference clock varies by more than ± 100 ppm the part will be declared out of lock. In the out of lock state, the PLL will lock to the local reference clock and periodically poll the serial data inputs looking for data with valid frequency content.

Figure 3. Input Jitter Tolerance

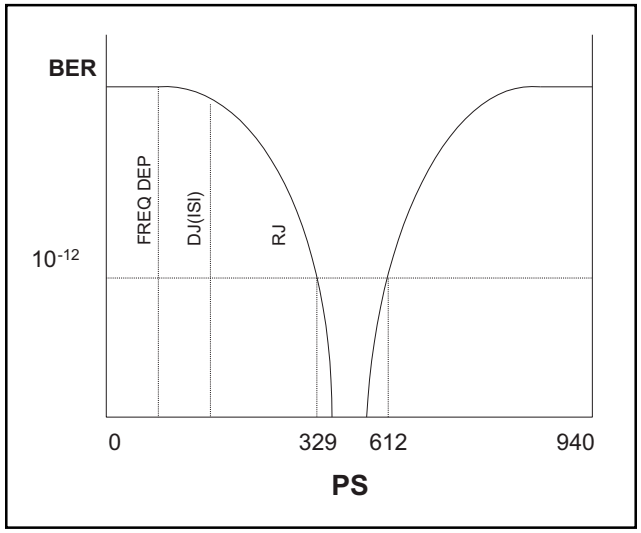


Figure 4. Frequency Dependent Jitter Tolerance Mask

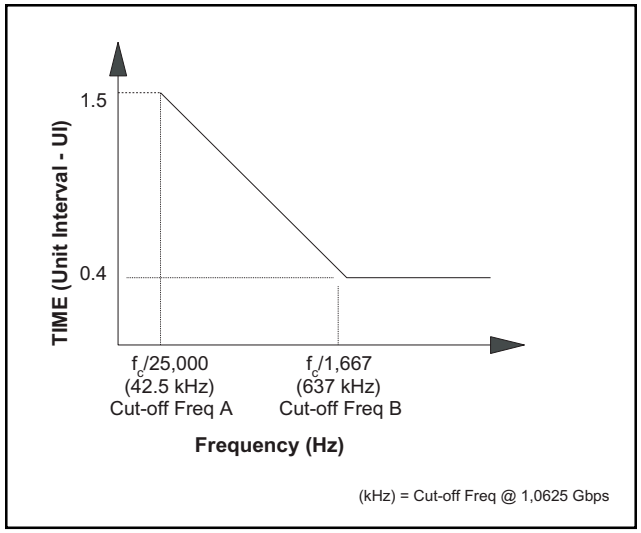


Figure 5. Jitter Transfer Specification

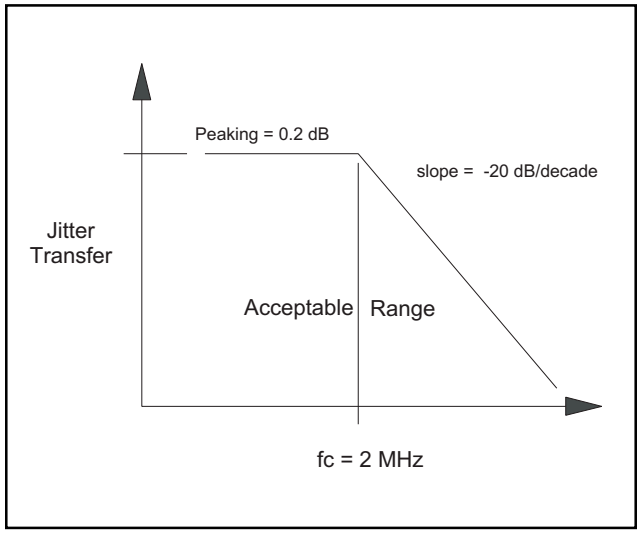


Table 1. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
OUTP OUTN	Diff. LVPECL	O	38 39	Serial output to be connected to the next PBC in the loop. (See Figure 2.) This output has been retimed by the clock and data recovery PLL.
INP INN	Diff. LVPECL	I	16 15	Serial input from the previous Port Bypass Circuit.
DDI0P DDI0N DDI1P DDI1N DDI2P DDI2N DDI3P DDI3N	Diff. LVPECL	I	4 3 61 60 50 49 43 42	Serial input to the port bypass. This input should be driven by the FC-AL disk drive connected to the port bypass. Any one of these input pairs may be routed to the CDR block if its PBC is in Normal Mode and the other PBCs are in Port Bypass Mode.
REFCLK	TTL	I	29	Reference clock for the PLL, rising edge active.
LPF1 LPF2	Analog		32 33	Loop Filter pins. The external loop filter capacitor and resistors are connected to these pins.
LCKREFN	3 State TTL	I	35	Active Low. When active, the PLL will be forced to lock to the local reference clock (REFCLK).
LOCKDET	TTL	O	34	Active High. When active, LOCKDET indicates the PLL is locked to the serial data stream. When inactive, the PLL will lock to the local reference clock indicating a loss of data condition.
DDO0P DDO0N DDO1P DDO1N DDO2P DDO2N DDO3P DDO3N	Diff. LVPECL	O	13 12 64 63 58 57 46 45	Port bypass output pairs. These outputs should drive the input ports of the FC-AL disk drive.
EN0 EN1 EN2 EN3	TTL	I	22 23 25 26	Port bypass control. Active High. When EN is inactive, the port bypass will be in bypass mode. When EN is active, port bypass will be in normal mode.

Table 1. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
GND	Ground		1, 14, 20, 30, 37, 48, 59	Ground pins are physically mounted to the die surface and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane using multiple vias if possible.
VCC			2, 11, 40, 41, 44, 47, 62	+3.3 V Power supply.
VCCA	Analog		19 28	+3.3 V Power supply for the CDR.
GNDA	Analog		18 27	Ground for the CDR.
BYPASS	3 Level TTL	I	17	Active High. Used for manufacturing test. Normal chip operation when inactive. When active, S2072 is put in Test Mode and the PLL will be bypassed for factory testing.
REFSEL	TTL	I	36	Active Low. When REFSEL is active, allows 106.25 MHz reference clock. When REFSEL is inactive, allows 53.125 MHz clock.
DNC			5, 6, 7, 8, 9, 10, 21, 24, 31, 51, 52, 53, 54, 55, 56	Do not connect.

Figure 6. S2072 Pinout

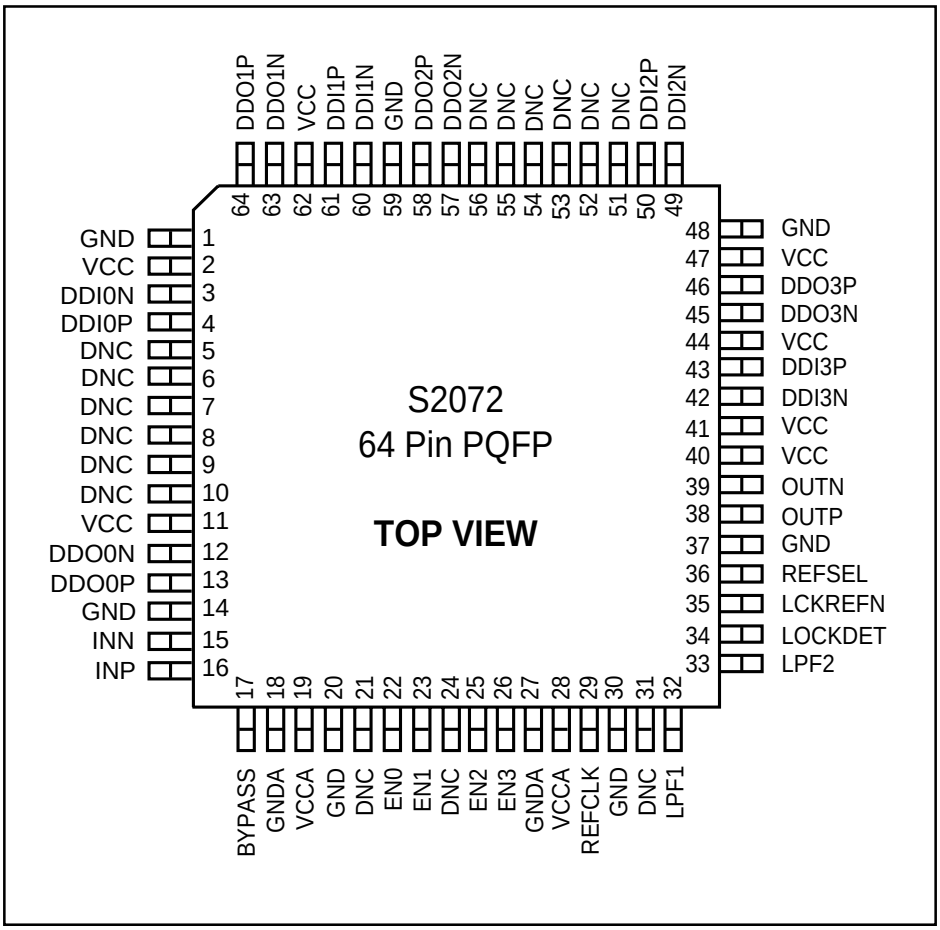
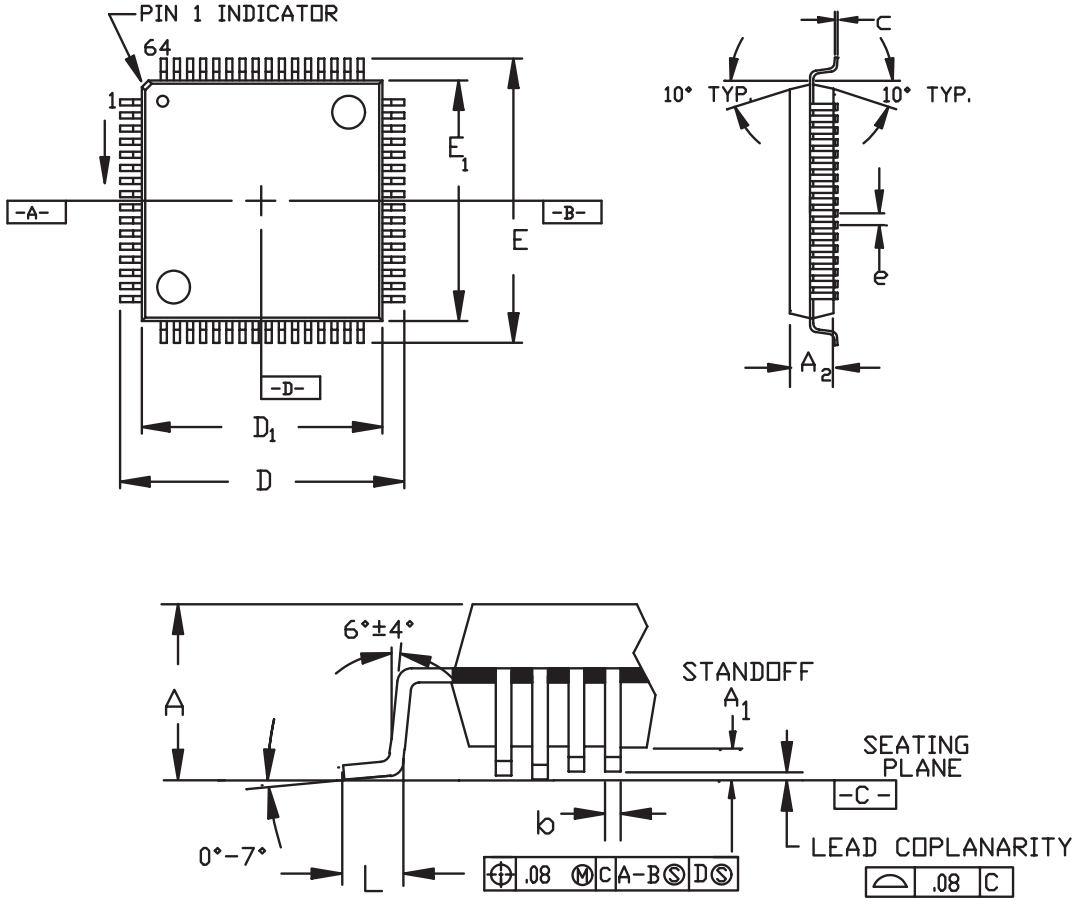


Figure 7. S2072 64 Pin PQFP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	13.00	9.90	13.00	9.90	0.78	0.50 BSC.	0.17	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.22	
MAX	2.45	0.50	2.10	13.40	10.10	13.40	10.10	1.03		0.27	0.17

Thermal Management

Device	Max Package Power[1]	Θ_{JA}
S2072	1.18 W	50° C/W

1. Power is measured with outputs terminated.

Table 2. AC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
T_R, T_F	Required REFCLK Rise and Fall time			3.0	ns	10% to 90%.
FT	Required REFCLK Frequency Tolerance	–100		+100	ppm	Difference between REFCLK and RX data frequency.
DC	Required REFCLK Duty Cycle	40		60	%	
T_{DD}	Any input to DDO[3:0] output propagation delay			4	ns	See Figure 8.
T_{RDDO} T_{FDDO}	Serial Data Rise and Fall time DDO[3:0] to OUT		185	350	ps	20% to 80%, tested on a sample basis.
Jitter Specifications						
RJOUT	Random Jitter (RMS) OUT P/N			14	ps	RMS, tested on a sample basis with worst case FC jitter input signal.
DJOUT	Deterministic Jitter (p-p) OUT P/N			50	ps	Peak-to Peak, tested on a sample basis with worst case FC jitter input signal.
FREQJT	Frequency dependent jitter tolerance IN P/N	0.1			UI	Jitter tolerance mask per Fibre Channel Jitter specification.
RANJT	Random Jitter Tolerance IN P/N			0.22	UI	Peak-to-Peak.
DJT	Deterministic Jitter Tolerance IN P/N			0.38	UI	Peak-to-Peak @ >53.125 MHz.
JXFR (Input to Output)	Jitter transfer peaking from IN P/N to OUT P/N			0.1	dB	
ΔV_{OUT}	LVPECL Output differential peak-to-peak voltage swing	1000		2200	mVp-p	50 Ω to V_{CC} - 2.0 V. See Figure 9.
ΔV_{IN}	Receiver differential peak-to-peak input sensitivity	200		2600	mVp-p	V_{CC} = 3.3 V, AC coupled. Internally DC biased to V_{CC}- 0.65 V. See Figure 9.
T_{JITTER} RMS	Random Jitter Accumulation, any input to DDO[3:0]		3	5	ps	RMS jitter accumulated with K28.7 data pattern. Tested on sample basis.
T_{JITTER} DJ	Deterministic Jitter Accumulation, any input to DDO[3:0]		±10	±40	ps	Deterministic jitter accumulated with ± K28.5 data pattern. Tested on sample basis.

Table 3. LVTTL DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage (TTL)	2.2			V	I_{OH} = –0.1 mA
V_{OL}	Output Low Voltage (TTL)			0.5	V	I_{OL} = +1.2 mA
V_{IH}	Input High Voltage (TTL)	2.0			V	
V_{IL}	Input Low Voltage (TTL)			0.8	V	
I_{IH}	Input High Current (TTL)			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current (TTL)	-600		-5	µA	V_{IN} = 0.5 V

Table 4. LVPECL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output High Voltage	V_{CC} -1.15			V	
V_{OL}	Output Low Voltage			V_{CC} -1.65	V	
V_{IH}	Input High Voltage	V_{CC} -1.2		V_{CC} -0.5	V	
V_{IL}	Input Low Voltage	V_{CC} -2.0		V_{CC} -1.4	V	
I_{IH}	Input High Current	-250		200	µA	
I_{IL}	Input Low Current	-250		200	µA	

The following are absolute maximum S2072 device stress ratings. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions beyond those indicated in the electrical characteristics section of this document is not implied.

Table 5. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
TTL Power Supply Voltage (V_{CC})	0.5		+4	V
PECL DC Input Voltage (V_{INP})	0		V_{CC}	V
TTL DC Input Voltage (V_{INP})	-0.5		5.0	V
DC Voltage applied to outputs for High output state ($V_{IN\ TTL}$)	-0.5		V_{CC} +0.5	V
TTL Output Current (I_{OUT}) (DC, Output High)			5	mA
PECL Output Current (I_{OUT}) (DC, Output High)			24	mA
Storage Temperature (T_{STG})	-65		150	˚C

Electrostatic Discharge (ESD) Ratings

The S2072 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1000 V, except pin 32 and pin 33.

Table 6. Recommended Operating Conditions [1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	+3.13		+3.47	V
Junction Temperature Under Bias			130	˚C
Ambient Operating Temperature Range	0		70	˚C
ICC Current Supply[2]		250	295	mA
Voltage on any LVPECL input pin	V_{CC}–2		V_{CC}	V
Voltage on any TTL input pin	0		V_{CC}	V

1. AMCC guarantees the functional and parametric operation of the part under "Recommended Operating Conditions," except where specifically noted in the AC and DC Parametric Tables.
2. ICC is measured with outputs not terminated.

POWER SUPPLY SEQUENCING

When the S2072 is operated with a 5 volt controller, it is recommended that power be applied to the S2072 before or simultaneously (time difference less than 1 ms) with the application of power to the 5 volt controller. If this condition cannot be met, series resistance of at least 33 Ohms is required on all TTL inputs driven from the 5 volt environment.

Please note that 33 Ohms is already recommended on dynamically switching input signals such as REFCLK and LCKREFN to limit overshoot and ringing. Static control lines such as EN[3:0], BYPASS, and REFSEL should also be provided with series resistors of at least 33 Ohms (100 Ohms recommended) to limit input current if the 5 volt environment is powered while the 3.3 volt VCC of the S2072 is off.

Figure 8. Timing Waveforms

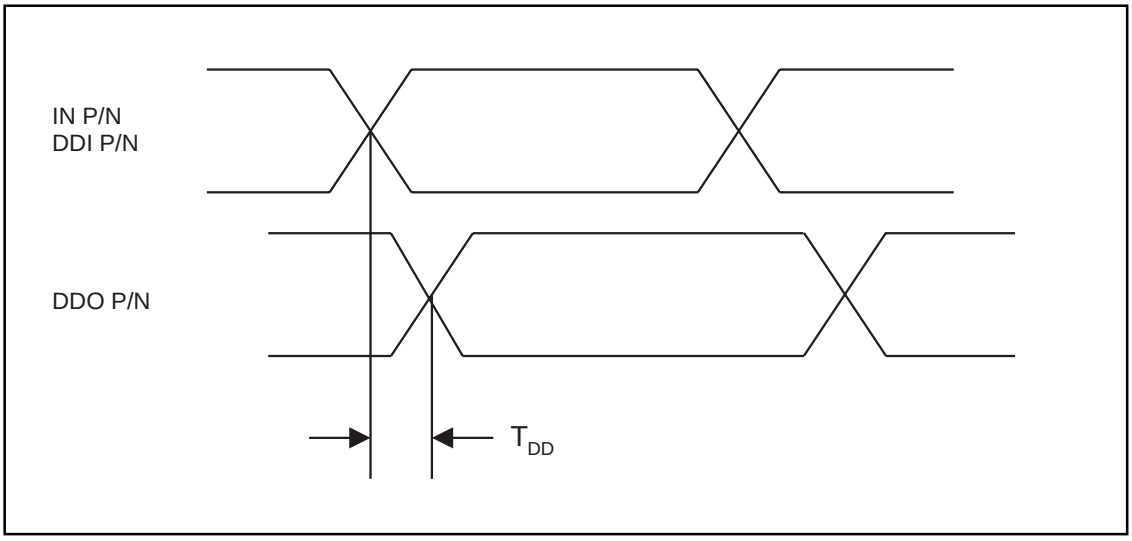
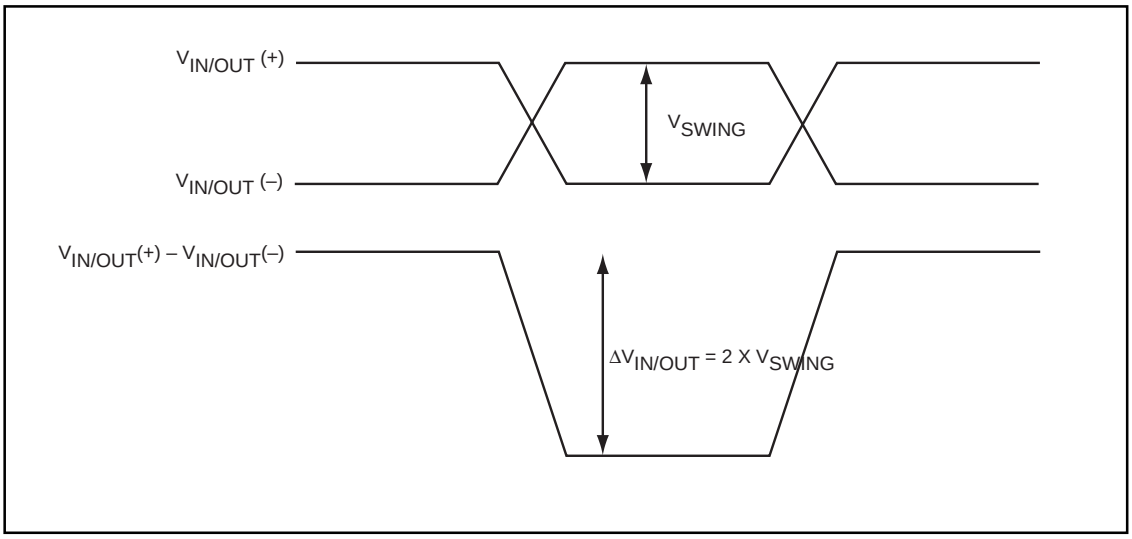


Figure 9. Differential Input/Output Voltage



Note: $V_{IN/OUT}(+) - V_{IN/OUT}(-)$ is the algebraic difference of the input/output signals.

Figure 10. High Speed Differential LVPECL Outputs

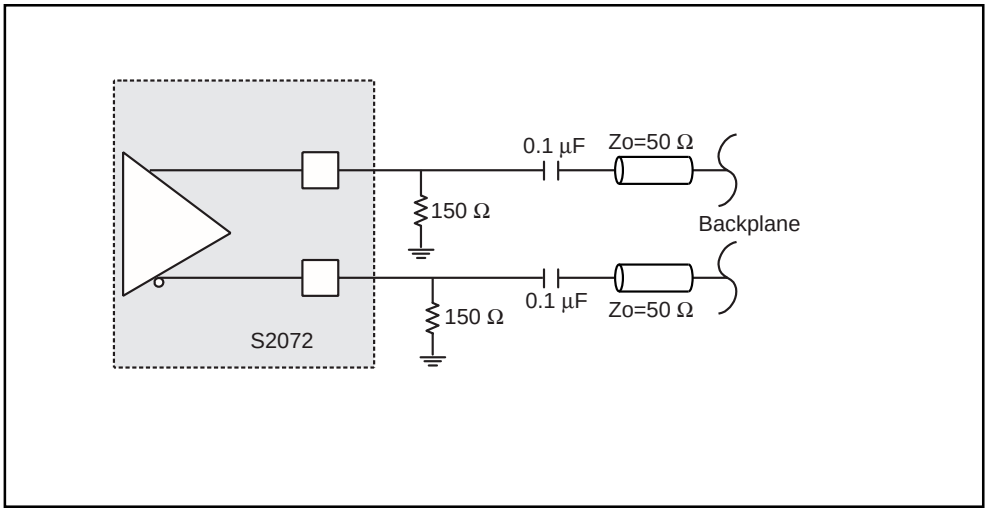


Figure 11. High Speed Differential LVPECL Inputs

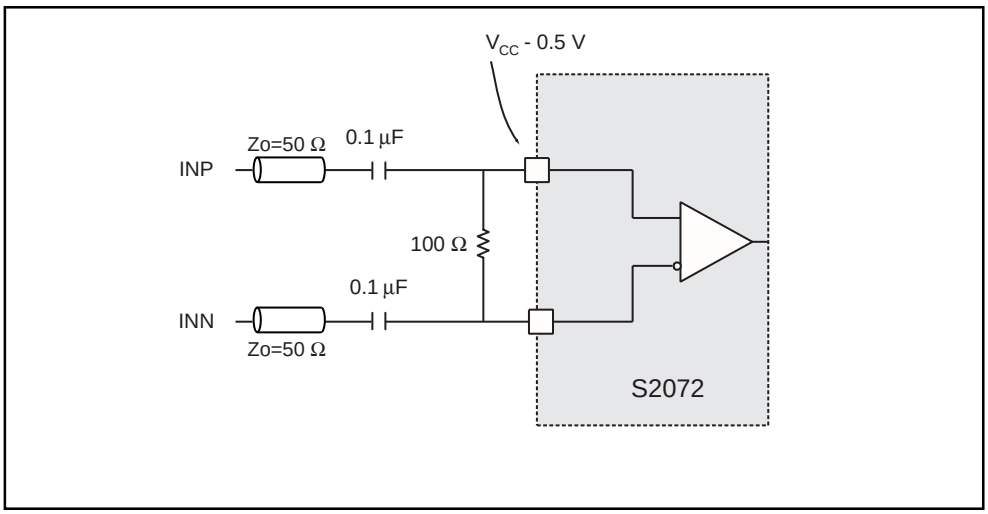
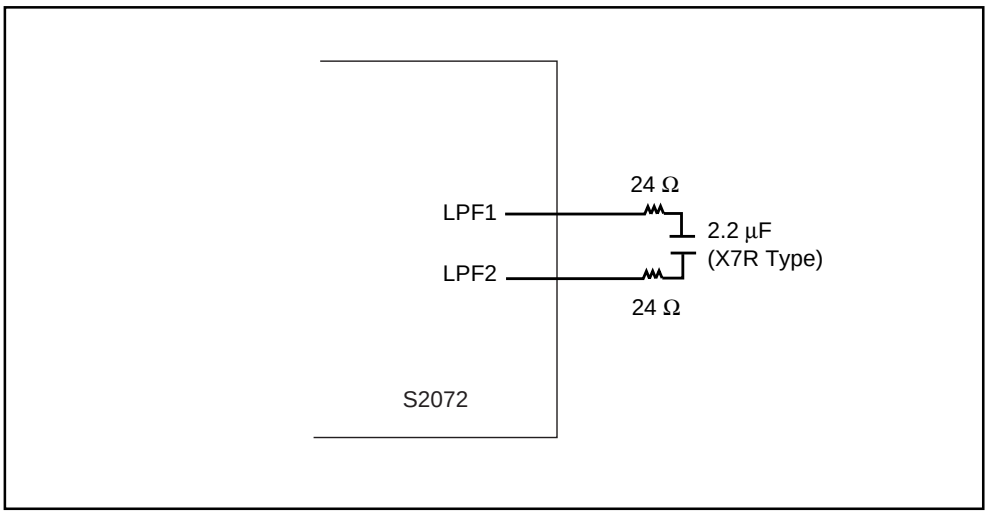
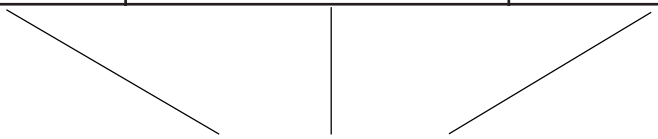


Figure 12. Loop Filter Circuit



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2072	QF – 64 Pin PQFP



X Prefix XXXX Part No. XX Package

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885
http://www.amcc.com