



MU9C9760, 9760V, 9760A SYNDAC™

PRELIMINARY SPECIFICATION

DISTINCTIVE CHARACTERISTICS

- o Combination Look-up Table, Triple Video DAC, and Dual Clock Synthesizer
- o Directly drives single- or double-terminated 75-ohm transmission line
- o VGA, Super-VGA, VESA, TIGA™, and 8514/A compatible
- o Displays 256 colors from a palette of 256K colors
- o Single external crystal or TTL-compatible input reference clock (typically 14.31818 MHz)
- o Eight Pixel Clock frequencies (CLK0)
- o Two Controller Clock frequencies (CLK1)
- o All frequencies may be re-programmed by the user
- o On-chip Loop filters reduce external components
- o Internal/external voltage reference (MU9C9760V/A) or external current reference (MU9C9760)
- o Precision internal reference (MU9C9760A)
- o Monitor sense comparators to detect monitor connections
- o Asynchronous Microprocessor Interface
- o Pixel Replicate™ prevents display noise caused by Look-up Table or Mask Register access during active display time
- o 44-pin PLDCC package
- o Available in 80-MHz, 66-MHz and 50-MHz Pixel Rates
- o High-performance CMOS for low power with TTL-compatible inputs

GENERAL DESCRIPTION

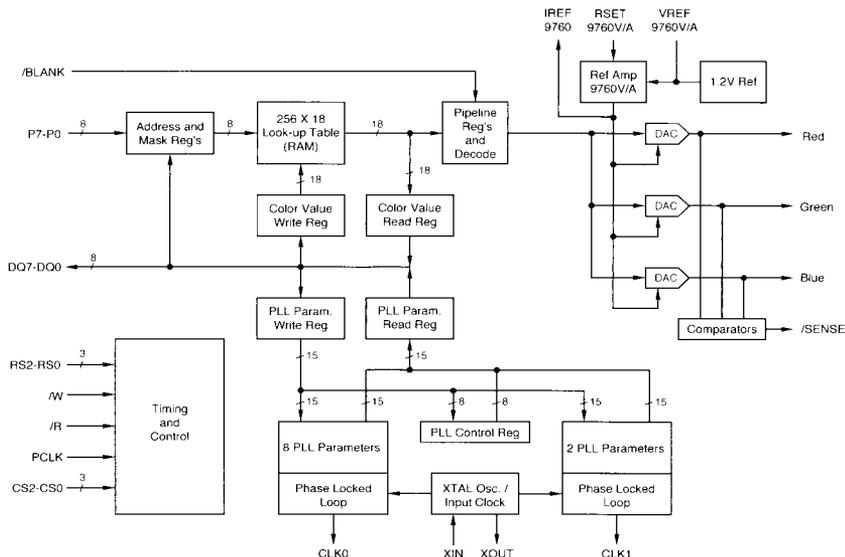
The MU9C9760, MU9C9760V, and MU9C9760A combine a 256-word by 18-bit Look-up table and three six-bit Video DACs with two programmable, 80-MHz clock synthesizers; and Monitor Sense comparators. The Look-up table accepts up to eight bits per pixel from a frame buffer and performs a translation into three six-bit values for conversion into Red, Green, and Blue analog signals. Each of the Video DACs can directly drive a double-terminated 75-ohm transmission line. The MU9C9760 sets the DAC output current with an external current reference. The MU9C9760V/A set the DAC output current by using an internal or external voltage reference.

The MU9C9760, MU9C9760V, and MU9C9760A are fully compatible with VGA, Super-VGA, VESA, TIGA™, and 8514/A industry standards while providing many enhanced features. One clock synthesizer has

eight programmable clock rates for use as a video dot clock. A second synthesizer has two programmable clock rates for use as a controller or frame buffer refresh clock. All of the pre-set frequency values may be re-programmed by the user after power-on. Monitor Sense comparators permit the detection of color, monochrome, or no monitor connection. These devices also incorporate a proprietary Pixel Replicate™ feature that allows Look-up table read and write operations to occur during the active portion of the display.

The MU9C9760, MU9C9760V, and MU9C9760A are available in a standard 44-pin PLDCC package and support the screen resolution, power requirements, and color capability necessary for high-performance Desktop Personal Computers.

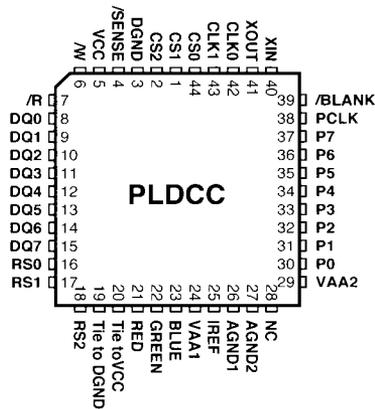
BLOCK DIAGRAM



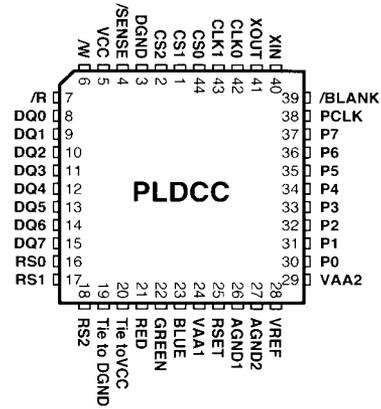
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MU9C9760V/A

PINOUT DIAGRAMS



MU9C9760



MU9C9760V/A

PIN DESCRIPTIONS

Red, Green, Blue (Video Signals, Outputs, Analog)

These signals are the outputs of the three Video DACs and are capable of driving a double- or single-terminated 75-Ω transmission line directly connected to a suitable monitor or video amplifier.

IREF (Reference Current, Input, Analog, 9760 only)

The IREF pin current sets the full scale output of the Video DACs. The IREF pin must be driven by an external current sink providing a regulated current. The value for IREF is determined by Equation [1], where VFS is the desired full scale DAC output voltage and Ro is the DAC load resistance with a monitor attached.

$$I_{REF} [mA] = \frac{V_{FS} [mV]}{R_o [\Omega] * 2.1} \quad [1]$$

VREF (Reference Voltage, Input, Analog, 9760V/A only)

The voltage on the VREF pin helps set the Video DAC full scale output (see Equation [2]). A voltage in the range of 1.0 to 1.5 volts applied to the VREF pin will override the internal 1.235-volt reference. VREF should be capacitively bypassed to AGND2 when using the internal voltage reference, but otherwise should not drive any external circuitry.

RSET (Reference Current, Input, Analog, 9760V/A only)

For the 9760V and 9760A, the DACs' full scale outputs are determined by a resistor from RSET to AGND2. The value of the resistor, RSET, is determined from Equation [2], where VREF is the reference voltage, VFS is the desired full scale DAC output voltage, and Ro is the DAC load resistance with a monitor attached.

$$R_{SET} [\Omega] = \frac{V_{REF} [V] * R_o [\Omega] * 2.1}{V_{FS} [V]} \quad [2]$$

P7-P0 (Pixel Address, Input, TTL)

P7-P0 provide the addresses that reference a color value stored in the Look-up Table for conversion to analog video signals. Individual Pixel Address bits are ANDed with the corresponding Mask Register bits. P7-P0 are registered on the rising edge of PCLK.

PCLK (Pixel Clock, Rising-edge-active Input, TTL)

The rising edge of PCLK registers the Pixel address (P7-P0) and /BLANK pins, transfers data in the internal pipeline, and internally synchronizes the Microprocessor Port signals. One pixel is displayed on the monitor for each Pixel Clock period.

/BLANK (Blank Control, Active-LOW Input, TTL)

The state of the /BLANK input is registered on the rising edge of PCLK. The /BLANK signal blanks the display during retrace. When /BLANK is HIGH, the DAC outputs reflect their digital input values. When /BLANK is LOW, the DAC outputs are forced to the Black Reference level. /BLANK has the same pipeline delay as P7-P0.

/SENSE (Monitor Sense, Active-LOW Output, TTL)

The /SENSE pin is LOW if one or more of the Red, Green or Blue outputs is higher than the internal 335-mV sense threshold.

MU9C9760/V/A

PIN DESCRIPTIONS (CONT'D)

XIN (Synthesizer Reference Clock, Input, Crystal/TTL)

The XIN pin is the reference clock for the two phase-locked loop synthesizers. The reference clock must come from a stable frequency source. XIN may be used either as a TTL input or as an internal oscillator by connecting a series-resonant crystal from XOUT to XIN.

XOUT (Crystal Oscillator, Output, Crystal)

The XOUT pin drives a series-resonant crystal from the internal oscillator to generate the synthesizer reference clock. XOUT is left open if an external TTL reference clock signal is used.

CLK0, CLK1 (Synthesizer Clocks, Output, TTL)

CLK0 is the output of the eight-frequency clock synthesizer, typically used for driving the pixel clock input of the video controller. CLK1 is the output of the two-frequency clock synthesizer, typically used as a controller or frame buffer refresh clock.

CS2-CS0 (CLK0 Frequency Select, Input, TTL)

An external controller may select the CLK0 frequency directly via CS2-CS0. These three pins select a set of PLL parameters that correspond to one of the eight CLK0 output frequencies. These pins are active at power-on, and remain active unless disabled by setting D5 in the PLL Control register to a logical one, allowing the PLL Control register to select the CLK0 frequency. Data changes on these pins are passed immediately to the CLK0 phase-locked loop control circuitry, i.e., these pins are not registered, and valid data must always be present unless disabled by D5.

/R (Read, Active-LOW Input, TTL)

A negative-going pulse on /R controls the DQ7-DQ0 Read cycle. RS2-RS0, registered on the falling edge of /R, determine the source of the Read Cycle data. The DQ7-DQ0 outputs become valid after the specified access time from the falling edge of /R. The DQ7-DQ0 outputs become high-impedance after the rising edge of /R.

/W (Write, Active-LOW Input, TTL)

A negative-going pulse on /W controls the DQ7-DQ0 Write cycle. RS2-RS0, registered on the falling edge of /W, determine the destination of the Write Cycle data. The DQ7-DQ0 data must meet set-up and hold times referenced to the rising edge of /W.

DQ7-DQ0 (Data Bus, I/O, Three-state TTL)

DQ7-DQ0 transfer all data to and from the Microprocessor port. The Color Value registers use only the six low-order bits (DQ5-DQ0); all other registers use all eight bits.

RS2-RS0 (Register Select, Input, TTL)

The states of RS2-RS0 at the beginning of a Microprocessor Port cycle determine the register to be read or written during that cycle as shown in Table 1. The beginning of the cycle is initiated by the falling edge of either /R or /W, depending on the type of cycle.

VAA1 (Analog Power Supply) □

AGND1 (Analog Ground)

The VAA1 and AGND1 pins provide the positive power supply and ground, respectively, for the analog portions of the device. They are separated from the VAA2 and AGND2 reference pins and the VCC and DGND digital supply pins to enhance noise margins. VAA1, VAA2, and VCC should all be tied to the same power plane, and AGND1, AGND2, and DGND should all be tied to the same ground plane, with appropriate care taken to minimize noise.

VAA2 (Power Reference)

AGND2 (Ground Reference)

The VAA2 and AGND2 pins provide reference voltages for the internal voltage reference, phase-locked-loop filters and VCO. To lower noise in these critical portions of the device, no high-speed switching currents are internally connected to the VAA2 and AGND2 pins. VAA1, VAA2, and VCC should all be tied to the same power plane, and AGND1, AGND2, and DGND should all be tied to the same ground plane, with appropriate care taken to minimize noise.

VCC (Digital Power Supply)

DGND (Digital Ground)

The VCC and DGND pins provide the positive power supply and ground, respectively, for the digital portion of the device. They are separated from the VAA1 and AGND1 analog supply pins and the VAA2 and AGND2 reference pins to enhance noise margins. VAA1, VAA2, and VCC should all be tied to the same power plane, and AGND1, AGND2, and DGND should all be tied to the same ground plane, with appropriate care taken to minimize noise.

RS2	RS1	RS0	Register
0	0	0	Address Register (RAM Write)
0	0	1	RAM Color Values
0	1	0	Pixel Mask Register
0	1	1	Address Register (RAM Read)
1	0	0	Address Register (PLL Write)
1	0	1	PLL Parameters
1	1	0	Reserved
1	1	1	Address Register (PLL Read)

Table 1: Register Access

MU9C9760V/A

FUNCTIONAL DESCRIPTION

Operational Characteristics

The MU9C9760V/A include a Video port, Address logic, a 256-word by 18-bit Look-up table (RAM), three six-bit Video DACs, two clock synthesizers, internal voltage reference (9760V/A only), output sense comparators, and the logic needed for a Microprocessor interface to access the Mask register, Look-up table, PLL parameters, and control functions providing the full operating capabilities of a graphics color palette plus a programmable dual clock synthesizer with access to eight CLK0 frequencies and two CLK1 frequencies.

Video Port Operation

The Look-up table and Video DACs display VGA-compatible pseudo-colors. P7-P0 and /BLANK are registered on the rising edge of PCLK. Look-up Table addresses from the Pixel register are logically ANDed with the Mask register to permit bit plane masking, and are then sent to the eight-bit Address register where one of 256 words in the Look-up table is selected. The 18-bit content of this address is transferred to the Video DACs.

The Triple Video DAC consists of three six-bit DACs capable of directly driving a double-terminated 75-ohm transmission line (75-ohm termination at both ends of the line). Each DAC consists of 63 identical current sources (set by the IREF or RSET pin current) which are selected through a six-bit binary decoder resulting in 64 levels per DAC.

The /BLANK (active LOW) input blanks the display during retrace. A LOW level on /BLANK forces the analog outputs to the Black Reference level without reference to the data at the DAC inputs. A HIGH level on /BLANK allows the DAC inputs to be converted into analog levels. The pipeline delay for /BLANK is identical to the delay for the P7-P0 path through the Look-up table (four registers in the pipeline, three clock delays).

Clock Synthesizers

Each phase-locked loop (PLL) frequency synthesizer provides programmable clock frequencies for use in the graphics subsystem. As shown in the PLL Block Diagram, Figure 1, both PLLs use the same reference frequency, f_{REF} , which may be generated by the internal clock oscillator with a 5-32 MHz series-resonant crystal connected between the XIN and XOUT pins, or by a TTL-compatible reference clock signal connected to XIN. Each PLL independently scales the reference frequency.

		PLL Ratio	Frequency (MHz)
CLK0	f0	1.75	25.172
	f1	1.98	28.332
	f2	2.27	32.514
	f3	2.48	35.500
	f4	2.51	36.000
	f5	2.79	40.000
	f6	3.14	44.900
	f7	4.54	65.000
CLK1	fA	2.79	40.000
	fB	3.49	50.000

$f_{ref} = 14.31818 \text{ MHz}$

Table 2: Pre-set Frequencies

Each clock output has its own frequency list. The CLK0 list contains eight frequencies (f0-f7) and the CLK1 list contains two (fA, fB). The frequency ratios in the CLK0 list are pre-set at power-on to commonly used Pixel Clock frequencies if the reference frequency, f_{REF} , is 14.31818 MHz. The CLK1 frequency ratios are also pre-set at power-on. The initialized frequency ratios are shown in Table 2, along with the corresponding clock frequencies. Other reference frequencies require the PLL parameters to be programmed during an initialization sequence after power-on.

At power-on, the CLK0 output frequency is selected from f0-f7 by the CS2-CS0 pins. The CLK0 frequency may be selected by D2-D0 in the PLL Control register by setting D5 in the PLL Control register to a logical one. The CLK1 output frequency is selected from fA or fB by D4 in the PLL Control register. When a frequency is selected, the values of M, N1, and N2 stored in the corresponding PLL Parameter word are sent to the PLL counters. The frequency selection may change at any time, but there will be a short period that the output frequency is uncertain while the PLL is locking to the new frequency (Switching parameter 17).

Monitor Sense Comparators

The Monitor Sense comparators test the output voltage level against an internal 335-mV threshold. The /SENSE output goes LOW if any output exceeds the threshold voltage. The /SENSE output may be read by the host processor, typically through a controller pin dedicated to this purpose. Monitor Sense may be used to detect the presence or absence of color

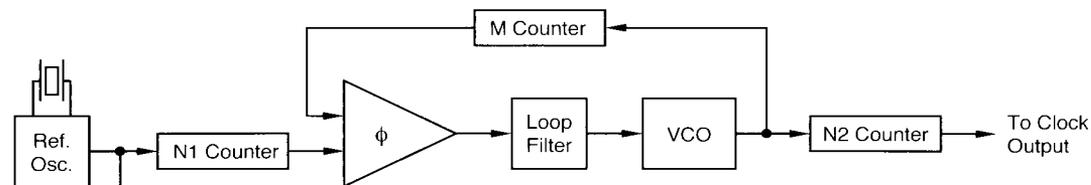


Figure 1: PLL Block Diagram

Rev. 1

MU9C9760/V/A

FUNCTIONAL DESCRIPTION (CONT'D)

or monochrome monitors or to perform diagnostics. The /SENSE pin should only be read when the DAC outputs are in a predictable state.

Microprocessor Port Operation

The Microprocessor port provides read and write access to the Look-up table's RAM array (256 words of 18 bits), the Mask register, and PLL Parameter and Control registers. Although the external operations of the Video port and Microprocessor port are asynchronous, Microprocessor port transactions destined for the Look-up Table RAM or the Mask register are internally synchronized by PCLK such that only one video cycle is interrupted for each 18-bit read or write of the Look-up table. To avoid noise on the display during this operation, the color data from the previous pixel is repeated (replicated) at the DAC outputs. This Pixel Replicate™ feature allows Look-up Table access during the active portion of the display.

INTERNAL REGISTERS

Any internal register listed in Table 1 or Table 3 may be read or written through the Microprocessor port. Table 1 registers are a single byte (and therefore read or written in a single Microprocessor Port cycle), except for the RAM Color Value and PLL Parameter addresses which are ports to the Table 3 registers.

For a Microprocessor Port Write cycle, the states of RS2-RS0 are first set to the desired value. The falling edge of /W captures the state of RS2-RS0. The signals on the Microprocessor Data bus (DQ7-DQ0) are captured on the rising

edge of /W for transfer to the proper byte of the selected register.

When writing to Table 3 registers, the Address register is first initialized by a Write cycle to RS2-0 = 0H or 4H, as appropriate. After the proper number of bytes have been written to the Color Value or PLL Parameter Write register, data is transferred to the indicated register. The Address register is then incremented in anticipation of writing to the next register, allowing sequential blocks of registers to be written.

For a Microprocessor Port Read cycle, RS2-RS0 are set to the desired value and captured on the falling edge of /R. The data to be output is placed on DQ7-DQ0 until after the rising edge of /R, at which time the data bus resumes a high-impedance state.

When reading Table 3 registers, the Address register is initialized with a Write cycle to RS = 3H or 7H, as appropriate. At this point, data is transferred from the selected register to the Color Value or PLL Parameter Read register, and then the Address register is incremented. After the indicated number of bytes have been read from the Color Value or PLL Parameter Read register, data is again transferred from the register selected by the Address register (now pointing to the next location), and the address register is again incremented in anticipation of the next read, allowing sequential blocks of registers to be read.

(Note: The Bit Assignment tables indicate the function or value of each bit when programmed to the state indicated at the left-hand edge of the table. D7 is read and written on DQ7; D0 is read and written on DQ0.)

RS2	RS1	RS0	Address Register	Accessed Register	Bytes
0	0	1	00H	Look-up Table Address 0	3
:	:	:	:	:	:
0	0	1	FFH	Look-up Table Address 255	3
1	0	1	00H	CLK0 f0 PLL Parameters	2
1	0	1	01H	CLK0 f1 PLL Parameters	2
1	0	1	02H	CLK0 f2 PLL Parameters	2
1	0	1	03H	CLK0 f3 PLL Parameters	2
1	0	1	04H	CLK0 f4 PLL Parameters	2
1	0	1	05H	CLK0 f5 PLL Parameters	2
1	0	1	06H	CLK0 f6 PLL Parameters	2
1	0	1	07H	CLK0 f7 PLL Parameters	2
1	0	1	08H	Reserved	2
1	0	1	09H	Reserved	2
1	0	1	0AH	CLK1 fA PLL Parameters	2
1	0	1	0BH	CLK1 fB PLL Parameters	2
1	0	1	0CH	Reserved	2
1	0	1	0DH	Reserved	2
1	0	1	0EH	PLL Control Register	1
1	0	1	0FH	Reserved	1

Table 3: Internal Register Map

MU9C9760N/A

FUNCTIONAL DESCRIPTION (CONT'D)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	M-Divider Value						
		MSB						LSB
0	X	0	0	0	0	0	0	0
1	X	1	1	1	1	1	1	1

Table 4: PLL Parameter Register M-Byte Bit Assignments

Mask Register

The eight-bit Mask register allows manipulation of the Pixel addresses. P7-P0 are bit-wise logically ANDed with the contents of this register before being sent to the Look-up table as an address. If the Mask register contains the byte value FFH, then the state of P7-P0 is unaltered. If the Mask register contains 00H, then the Look-up table will be passed 00H. The masking of individual bits may be used to create animation effects on the screen. Mask register operations are internally synchronized to PCLK, allowing unlimited read and write access during any portion of the display.

Address Register

The eight-bit Address register is accessed through one of four register select addresses depending upon the desired action. Separate addresses are provided for reading and writing either color values or PLL parameters. The Address register auto-increments to allow sequential block transfers of color values or PLL parameters without re-programming the Address register.

RAM Color Value

The RAM color values are written through the Write Color Value register (18 bits) and read through the Read Color Value register (18 bits) in three Read or Write cycles. The address of the accessed color value is determined by the Address register. The DQ5-DQ0 pins transfer the six-bit Red field on the first Microprocessor port cycle, the six-bit Green field on the second cycle and the six-bit Blue field on the third. DQ5 corresponds to the DAC MSB, and DQ0 to the LSB. Sequential blocks of color values may be transferred without re-programming the Address register.

PLL Parameters

All of the PLL parameters are initialized at power-on to provide an initial set of available frequencies. Any PLL parameter may be re-programmed through the Microprocessor port to customize the frequency list for a particular application. Both

the initialized and re-programmed PLL parameters may be read back through the Microprocessor port.

PLL parameters are written through the PLL Parameter Write register (15 bits) and read through the PLL Parameter Read register (15 bits) in two Read or Write cycles. The address of the accessed PLL parameter is determined by the Address register. The M-Byte is transferred on the first Microprocessor port cycle, followed by the N-Byte on the next cycle. Sequential blocks of PLL parameters may be transferred without re-programming the Address register.

M-Byte

The M-Byte (Table 4) contains the value used in the feedback divider of the PLL. The M-Byte data is transferred via DQ6-DQ0. Reserved bits are initialized to logical zeroes at power-on and are read back as logical zeroes; they should normally be programmed to logical zeroes.

D6-D0 M-Divider Value

D6-D0 of the M-Byte for the currently selected frequency provide the value used by the M-Divider. The M-Divider value may be set to any integer from 0 to 127. The M-Divider is in the feedback loop of the PLL.

N-Byte

The N-Byte (Table 5) contains the values for the PLL pre- and post-scalers. The N-Byte data is transferred via DQ7-DQ0. Reserved bits are initialized to logical zeroes at power-on and are read back as logical zeroes; they should normally be programmed to logical zeroes.

D3-D0 N1-Divider Value

D3-D0 of the N-Byte for the currently selected frequency provide the value used by the N1-Divider. The N1-Divider value may be set to any integer from 0 to 15. The N1-Divider pre-scales the reference frequency for the PLL.

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved		N2-Divider Code		N1-Divider Value			
			MSB	LSB	MSB		LSB	
0	X	X	0	0	0	0	0	0
1	X	X	1	1	1	1	1	1

Table 5: PLL Parameter Register N-Byte Bit Assignments

MU9C9760V/A

FUNCTIONAL DESCRIPTION (CONT'D)

D5-D4 N2-Divider Code

The value used by the N2-Divider is decoded from D5-D4 of the N-Byte for the currently selected frequency. The N2-Divider code may be set to any integer from 0 to 3, which sets the N2-Divider value to 1, 2, 4, or 8. The N2-Divider divides the PLL output by the selected amount.

PLL Control Register

The eight-bit PLL Control register controls the clock synthesizer phase-locked-loops using the bit assignments shown in Table 6. The PLL Control register is read or written in one Microprocessor Port cycle with the Address register set to 0EH. The Address register is auto-incremented when reading or writing the PLL Control register, so the Address register must be initialized before each access. Reserved bits are initialized to logical zeroes at power-on and are read back as logical zeroes; they should normally be programmed to logical zeroes.

D2-D0 CLK0 Select

These three bits select the CLK0 output frequency if D5 is a logical one. D2-D0 are interpreted as an octal number, n, that selects fn. D2, D1, and D0 are initialized to a logical zero at power-on, although the initial CLK0 PLL parameters are determined by the CS2-CS0 pins.

D4 CLK1 Select

This bit selects the CLK1 output frequency. If D4 is a logical zero, fA is selected. If D4 is a logical one, fB is selected. D4 is initialized to a logical zero at power-on, setting the CLK1 output frequency to the reference frequency.

D5 CLK0 External Select Enable

If D5 is a logical zero, the CLK0 output frequency is selected by the external CLK0 Frequency Select pins, CS2-CS0. If D5 is a logical one, the CLK0 output frequency is determined by D2-D0 in the PLL Control register. D5 is initialized to a logical zero at power-on, selecting the external pins.

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved		CLK0 External Select Enable	CLK1 Select	Reserved	CLK0 Select		
						MSB		LSB
0	0	0	External	A	X	0	0	0
1	X	X	Internal	B	X	1	1	1

Power-on initialized state in **Bold-Italic**

Table 6: PLL Control Register Bit Assignments

APPLICATIONS

DAC REFERENCE

The MU9C9760 requires an external current sink to set the DAC output levels. Such a reference can easily be built from a minimum of low-cost components, as shown in Figure 2. Shunt-type current regulators are not recommended, since this type of regulator requires a second current path from VCC to ground that bypasses the IREF pin for proper operation, increasing the current consumption. Current regulators connected to a negative supply should also be avoided. Better results are obtained if IREF is not capacitively bypassed to VAA; in fact a ferrite bead (L2 in Figure 2) between the IREF pin and the current regulator can reduce high-frequency current variations, and is recommended in noisy environments.

The MU9C9760V/A may be configured to use the internal voltage reference or an external voltage reference. When using the internal 1.235-volt reference, only an external resistor and capacitor are required (Figure 3). The internal reference should be accurate enough for most applications. If more accuracy is desired, an external voltage reference may be used. The wide operating range of the reference amplifier allows the user to choose a standard 1.235-volt two-terminal reference or a lower-cost 1.25-volt regulator (Figure 4).

PROGRAMMING AND USING THE PLLs

Upon power-up, all PLL parameter ratios are initialized, the CLK0 synthesizer operates at the frequency selected by the CS2-CS0 pins, and CLK1 initially runs at the reference frequency. The initialized ratios in Table 3 correspond to some common graphics dot clock frequencies when a reference frequency of 14.31818 MHz is used. If different PLL output frequencies are desired, or if a different reference frequency is used, the initialized ratios may be replaced with user-programmed values. A single PLL parameter may be replaced without affecting any others, or the entire list may be reprogrammed using the auto-increment feature of the Address register.

An output frequency is changed by programming the M-Byte and N-Byte of the corresponding PLL parameter. These two bytes contain the three PLL parameters, M, N1, and N2, plus two mode control bits. M is an integer between 0 and 127, N1 is an integer between 0 and 15, and N2 is an integer between 0 and 3. The output frequency, fOUT, is then calculated from the reference frequency, fREF, by Equation [3].

MU9C9760/V/A

APPLICATIONS (CONT'D)

$$f_{OUT} = \frac{(M+1)}{(N1+1) \cdot 2^{(N2)}} \cdot f_{REF} \quad [3]$$

For proper operation, f_{REF} , M , and $N1$ should be selected within the constraints of Equation [4], Equation [5], and Equation [6].

$$5 \text{ MHz} \leq f_{REF} \leq 32 \text{ MHz} \quad [4]$$

$$2 \text{ MHz} \leq \frac{f_{REF}}{(N1+1)} \leq 16 \text{ MHz} \quad [5]$$

$$40 \text{ MHz} \leq \frac{(M+1) \cdot f_{REF}}{(N1+1)} \leq 80 \text{ MHz} \quad [6]$$

CRYSTAL OSCILLATORS

When using a series resonant crystal to generate the reference frequency for the MU9C9760/V/A, it is recommended that the standard configuration of two resonance capacitors be used, shown as C5 and C6 in Figure 5. The recommended value for C5 and C6 is 220 pF, but this value should be checked in the actual operating circuit to confirm the performance.

SYSTEM APPLICATIONS

The Look-up table of the MU9C9760/V/A can display up to 256 colors at a time. Each of these colors can be any combination of the 64 levels available from each of the three DACs—Red, Green and Blue.

When driving analog monochrome (gray-scale) displays, only one DAC output is connected to the single video input of the monitor. The other DAC outputs must be terminated with the equivalent of a single- or double-terminated 75- Ω transmission line (37.5- to 75- Ω resistive load to ground) or tied directly to AGND. If the video frame buffer information is intended to be displayed on a color monitor, the Look-up table can be reprogrammed to provide only the intensity portion of the color information. This technique allows the display of a digitized color frame in monochrome.

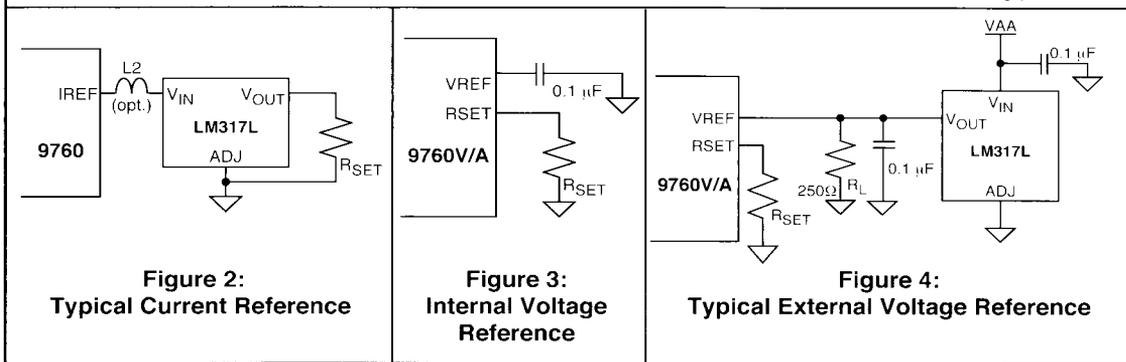
The Look-up table also allows pseudo-color image processing techniques, such as density slicing, to be easily implemented

on monochrome digitized images. Density slicing is a technique that assigns each gray-scale level in a monochrome image a unique color for display. Small differences in intensity (one bit of the grey scale) are difficult for the eye to differentiate in monochrome, but become readily apparent when assigned unique colors. By changing only the contents of the Look-up table, the displayed image can be transformed from monochrome into color.

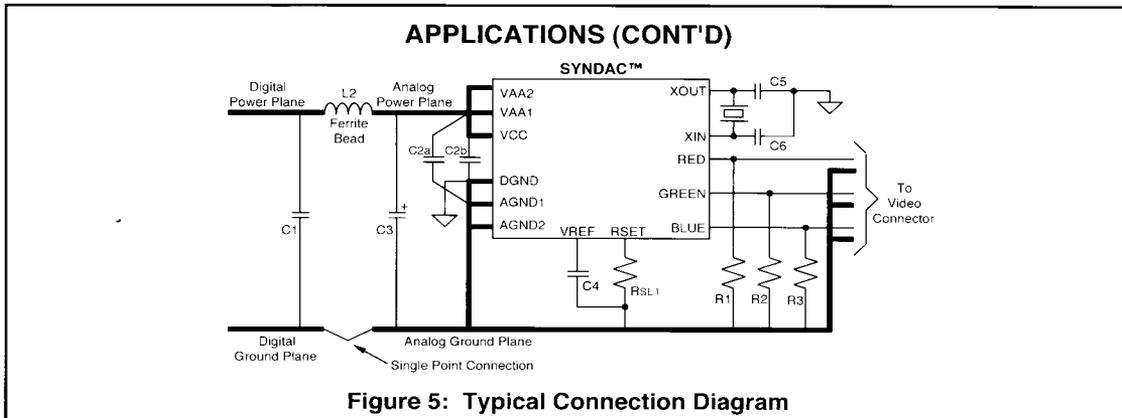
PC LAYOUT GUIDELINES

The MU9C9760/V/A must receive power from a noise-free, low-impedance power distribution system. The use of VCC and ground planes is highly recommended. Since one side of the package has the digital supplies (VCC and DGND) and opposite side has the analog supplies (VAA and AGND), high quality 0.01- μ F and 100-pF high-frequency ceramic bypass capacitors should be placed on both sides of the package. For maximum PCLK frequencies lower than 30 MHz, 0.1- μ F and 1000-pF capacitors should be used instead. In addition, a 4.7- μ F tantalum electrolytic capacitor should be placed nearby to help filter low frequency noise. The other TTL and CMOS devices on the PCB should also be capacitively bypassed.

A separate power distribution network is recommended for the MU9C9760/V/A color palettes to ensure a noise-free power supply. One approach is to provide separate power and ground planes for the color palette and its associated analog circuitry, as shown in Figure 5. The separate analog power plane is isolated from the PCB's digital logic supplies by a ferrite bead (L1) and is connected to the VCC and VAA pins on the color palette. A 4.7- μ F tantalum electrolytic capacitor to ground (C3) filters low-frequency noise. C2a consists of a pair of ceramic capacitors, as described above, located near VAA and AGND to bypass the analog power and ground pins. C2b is similarly constructed and placed near VCC and DGND to bypass the digital power and ground pins. The analog ground plane isolates digital ground currents from the analog components, and should be separated from the digital ground plane by at least a 1/8-inch (3-mm) gap. The two ground planes should be connected together at a single point (preferably near the PCB's ground connection) by a wide, low-impedance path. The signal lines connected to the P7-P0, /BLANK and PCLK inputs must be either very short or terminated to eliminate the possibility of ringing or undershoot that might affect critical timing parameters. The traces for these signals should be led over the digital ground plane and avoid the analog power and



Rev. 1



ground planes. This device is fabricated in CMOS technology with high-impedance inputs that may not clamp to ground.

To reduce noise, traces connecting external IREF, VREF, and DAC output circuitry should only be run over the analog ground plane, and should be kept as short as possible. If the distance from the DAC outputs to the Video connector cannot be kept extremely short, the connecting traces should be constructed as 75-Ω microstrip transmission lines. In general, this constraint implies wider traces, but the exact dimensions must be calculated from the board material and construction.

DEVICE HANDLING AND PROTECTION

CMOS devices are subject to a condition known as latch-up. Latch-up can occur when parasitic four-layer devices similar to SCRs are turned on, typically leading to excessive current flow from VCC to ground. If left to continue, this current may cause the bond wires to open and the device to fail catastrophically. Although steps are taken during design to minimize a product's

sensitivity to latch-up, additional precautions should be taken by the user. Digital signals that go directly off the board should be terminated with either a 47-Ω series resistor or a 1-KΩ resistor to DGND. If a 1-KΩ resistor to DGND is used, be sure that the output driver connected to that node can pull the inputs above $V_{IH(min)}$ (typically 2.4 mA source current per 1-KΩ pull-down resistor). Either method will greatly increase the latch-up threshold, as well as reduce EMI radiation (which will aid in meeting FCC standards for radiated noise) and improve Electro-static Discharge (ESD) damage protection.

CMOS devices are subject to damage from ESD. To avoid permanent damage from high-energy electrostatic fields, always follow proper handling procedures. Store unused devices in conductive foam, carriers, or tubes. Devices should be handled only at ESD protected workstations (grounded floor mat and work surface) while wearing a grounded wrist strap and anti-static smock. Never insert devices into a powered socket, and never insert circuit boards into a powered edge-connector.

Figure 6: DAC Switching Test Load

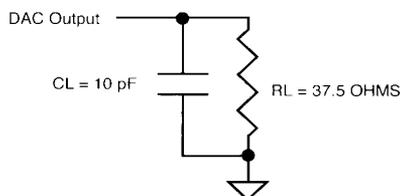


Figure 7: TTL Switching Test Load

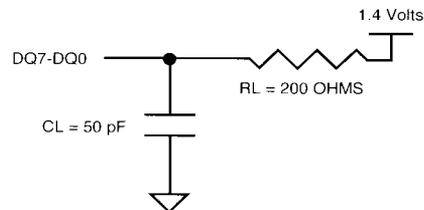


Figure 8: TTL Three-state Test Load

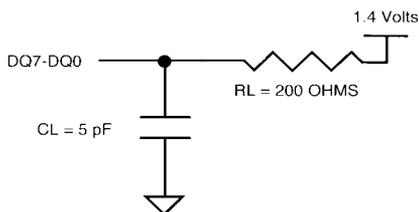
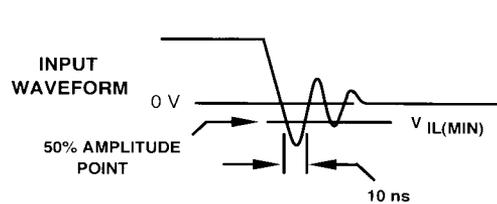


Figure 9: V_{IL} Waveform



MU9C9760/V/A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns at the 50% point; see Figure 9)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
Maximum Reference Current Magnitude	15 mA
Maximum DAC Output Current Magnitude	45 mA (per Output)
Maximum DC TTL Output Current Magnitude	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to DGND, except the Internal Voltage Reference and Monitor Sense Comparator Threshold voltages, which are referenced to AGND2.

OPERATING CONDITIONS (voltages referenced to DGND at the device pins)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V _{CC}	Operating Supply Voltage	4.5	5.0	5.5	Volts	
V _{IH}	Input Voltage Logic "1"	2.0		V _{CC} +0.5	Volts	
V _{IL}	Input Voltage Logic "0"	-0.5		0.8	Volts	-1.0 Volts for 10 ns measured @ 50% amplitude (Fig. 9)
V _{REF}	External Voltage Reference	1.0	1.235 1.25	1.5	Volts	16 Precision Reference Voltage Regulator
I _{REF}	Reference Current Magnitude	3.5	8.89	10	mA	12
f _{REF}	Reference Frequency					
	MU9C9760/9760V	12	14.31818	16	MHz	
	MU9C9760A	5	14.31818	32	MHz	
T _A	Ambient Operating Temperature	0		70	°C	Still Air

ELECTRICAL CHARACTERISTICS (over the Operating Temperature and Voltage ranges)

Symbol	Parameter	Min	Typ	Max	Units	Notes
I _{CC}	Avg. Power Supply Current		150 155	170 180	mA mA	PCLK, CLK0=50, 66MHz: 1 PCLK, CLK0=80 MHz: 1
V _{REF(INT)}	Internal Voltage Reference					I _{VREF} = 0 μA: 16
	MU9C9760A	1.200	1.235	1.270	Volts	
	MU9C9760V	1.110	1.235	1.360	Volts	
I _{VREF}	Voltage Ref. Input Current	-15		15	μA	1.2 V ≤ VREF ≤ 1.3 V; 15
V _{TH}	Monitor Sense Comparator Threshold	300	335	370	mV	
V _{OH}	Output Voltage Logic "1"	2.4			Volts	I _{OH} =-5.0 mA
V _{OL1}	Output Voltage Logic "0" (all outputs and I/O pins except CLK0, CLK1)			0.4	Volts	I _{OL} =5.0 mA
V _{OL2}	Output Voltage Logic "0" (CLK0, CLK1 only)			0.4	Volts	I _{OL} =8.0 mA
I _{ILK}	Input Leakage Current	-2		2	μA	V _{DGND} ≤ V _{IN} ≤ V _{CC}
I _{OLK}	Leakage Current (DQ7-DQ0)	-10		10	μA	V _{DGND} ≤ V _{IN} ≤ V _{CC} ; R ≥ V _{IH} (min)

Rev. 1

MU9C9760/V/A

ELECTRICAL CHARACTERISTICS (CONT'D)						
DAC Parameter Specifications						
Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{IREF}	Voltage on IREF	V _{CC} -3.0		V _{CC}	Volts	11,16; 3.5 mA ≤ I _{IREF} ≤ 10.0 mA
V _O MAX	Max. Output Voltage			1.5	Volts	10,11; I _O ≤ 10 mA
I _O MAX	Max. Output Current	21			mA	11; V _O ≤ 1.0 Volts
	Resolution	6			bits	
	DAC Full Scale Error			±5	%	2, 11
	DAC Output Matching			0.5	%	3; at I _O = Black & White levels
	Integral Nonlinearity			±0.5	LSB	4
	Rise Time (DAC Output)			4	ns	6; 10% to 90%; Load as shown in Fig. 6
	Full Scale Settling Time			12.5	ns	5,6; Load as shown in Fig. 6
	Glitch Energy			40	pV-sec	6; Load as shown in Fig. 6

NOTES	
1.	ICC is measured with VCC=VCC (max) and tCHCH=tCHCH (min). fREF = 14.31818 MHz TTL clock, CLK1 = 14.31818 MHz unless otherwise noted. The DAC test load is as shown in Figure 6. DQ7-DQ0, CLK0, and CLK1 are unloaded. IREF = 8.89 mA or Ext. VREF = 1.235 Volts and RSET = 139Ω.
2.	Full Scale Error is measured from the value given by the design equation. IREF = 8.89 mA or Ext. VREF = 1.235 Volts and RSET = 139Ω.
3.	Measured from the center value of the DAC outputs. IREF = 8.89 mA or Ext. VREF = 1.235 Volts and RSET = 139Ω.
4.	Measured from a straight line between the endpoints. Monotonicity is guaranteed.
5.	Full Scale Settling Time is measured from a 2% change in output voltage until the output voltage has settled to within ±2% of final value.
6.	Guaranteed but not 100% tested.
7.	Measured at the 50% point between the starting and ending DAC values.
8.	Measured from a ±200 mV change from the steady-state voltage using Test Load as shown in Figure 8.
9.	/BLANK ≤ VIL(MAX) to disable RED, GREEN, and BLUE Analog outputs.
10.	All DAC outputs must be terminated with the equivalent of a single- or double-terminated 75-Ω transmission line (75-Ω or 37.5-Ω resistive load to ground), independent of the number of DAC outputs used. Unused DAC outputs may also be tied directly to AGND1.
11.	The IREF pin, RSET pin, and analog output pins always source current. This specification shows a current magnitude and ignores the algebraic sign. Measured with IREF = -8.89 mA for IREF devices, or Ext. VREF = 1.235 Volts and RSET = 139Ω ±0.5% for VREF devices. These typical reference values give an output voltage of 700 mV into a 37.5-Ω load (75-Ω local termination in parallel with 75-Ω monitor).
12.	Measured from the PCLK transition that causes the DAC to change. The internal pipeline delay of four registers (three clock delays) from P0-P7 to the DAC output is not included.
13.	Rise and Fall times are measured at 0.8 Volt and 2.0 Volt levels. The clock output load capacitance for Rise and Fall time measurements is 15 pF.
14.	Duty Cycle is computed as (Output Clock HIGH/Output Clock Period) * 100%.
15.	MU9C9760V and MU9C9760A only.
16.	MU9C9760 only.
17.	PLL Parameters must meet the criteria of equations [4], [5], and [6].

MU9C9760/V/A

SWITCHING CHARACTERISTICS

AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 Volts
Video Port Signal Rise and Fall Times	≤ 2 ns
Microprocessor Port Signal Rise and Fall Times	≤ 3 ns
Digital Input Timing Reference Level	1.5 Volts
Digital Output Timing Reference Levels	0.8 V and 2.4 V
DAC Switching Test Load	Figure 6
TTL Switching Test Load	Figure 7

VIDEO PORT

No.	Symbol	Parameter	-80		-66		-50		Units	Notes
			Min	Max	Min	Max	Min	Max		
	f _{MAX}	PCLK Frequency		80		66		50	MHz	
1	t _{CHCH}	PCLK Period	12.5		15		20		ns	
2	t _{CLCH}	PCLK LOW	4		5		6		ns	
3	t _{CHCL}	PCLK HIGH	4		5		6		ns	
4	t _{PVCH}	P7-P0 and /BLANK Setup to PCLK HIGH	3		3		3		ns	
5	t _{CHPX}	P7-P0 and /BLANK Hold from PCLK HIGH	3		3		3		ns	
6	t _{CHAV}	PCLK to DAC Valid	0	20	0	20	0	20	ns	7, 12
6a	Δt _{CHAV}	DAC to DAC Skew		1		1		1	ns	6, 7
7	t _{AVQV}	DAC Valid to /SENSE Valid		1.0		1.0		1.0	μs	

CLOCK SYNTHESIZER

No.	Symbol	Parameter	All Speed Grades		Units	Notes
			Min	Max		
		XIN Frequency Range		5	32	MHz
8	t _{KHKH}	XIN Period		31.25	200	ns
9	t _{KLKH}	XIN LOW		5		ns
10	t _{KHKL}	XIN HIGH		5		ns
11	t _{r1}	XIN Rise Time			20	ns
12	t _{f1}	XIN Fall Time			20	ns
	f _{VCO}	Internal VCO Frequency Range		40	80	MHz
13	t _{KQHKQH}	CLK0, CLK1 Period	-50 -66 -80	20 15 12.5		ns ns ns
14	t _{r2}	CLK0, CLK1 Rise Time			4	ns
15	t _{f2}	CLK0, CLK1 Fall Time			4	ns
		CLK0, CLK1 Duty Cycle		40	60	%
16	t _{DXQV}	CLK0, CLK1 frequency hold after change		0		ns
17	t _{DVKQV}	CLK0, CLK1 stable after frequency change			5	ms
		Clock Stability		-200	+200	pS

Rev. 1

MU9C9760/V/A

SWITCHING CHARACTERISTICS (CONT'D)

MICROPROCESSOR PORT READ CYCLE

No.	Symbol	Parameter	All Speed Grades		Units	Notes
			Min	Max		
18	t _{RLRH}	Read Pulse Width	50		ns	
19	t _{RHRL1}	Successive Read Interval	3 X t _{CHCH}		ns	
20	t _{RHWL1}	Read to Write	3 X t _{CHCH}		ns	
21	t _{RHRL2}	Color Read to Read	6 X t _{CHCH}		ns	
22	t _{RHWL2}	Color Read to Write	6 X t _{CHCH}		ns	
23	t _{SVRL}	Register Select Setup to /R LOW	10		ns	
24	t _{RLSX}	Register Select Hold from /R LOW	3		ns	
25	t _{RLQV}	Data Access from /R LOW		40	ns	
26	t _{RLQX}	Output Turn-on from /R LOW	3		ns	8
27	t _{RHOX}	Data Hold from /R HIGH	3		ns	
28	t _{RHOZ}	Data Three-state Delay from /R HIGH		20	ns	8

MICROPROCESSOR PORT WRITE CYCLE

No.	Symbol	Parameter	All Speed Grades		Units	Notes
			Min	Max		
29	t _{WLWH}	Write Pulse Width	50		ns	
30	t _{WHWL1}	Successive Write Interval	3 X t _{CHCH}		ns	
31	t _{WHWL2}	Write after Color Write	3 X t _{CHCH}		ns	
32	t _{WHRL1}	Write to Read	3 X t _{CHCH}		ns	
33	t _{WHRL2}	Color Write to Read	3 X t _{CHCH}		ns	
34	t _{WHRL3}	Read after Read Address Write	6 X t _{CHCH}		ns	
35	t _{SVWL}	Register Select Setup to /W LOW	10		ns	
36	t _{WLSX}	Register Select Hold from /W LOW	3		ns	
37	t _{DVWH}	Data Setup to /W HIGH	10		ns	
38	t _{WHDX}	Data Hold from /W HIGH	3		ns	

CAPACITANCE

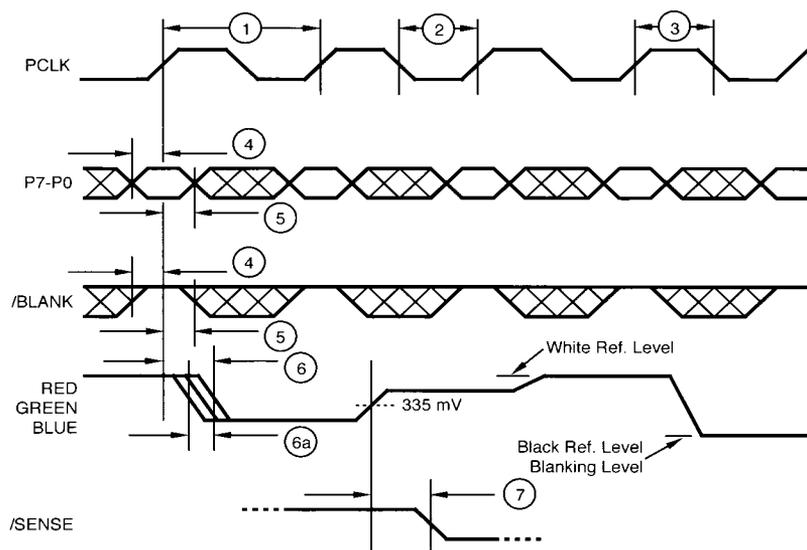
T_A = 0 to 70 °C; V_{CC} = 5.0 V ± 10%; f = 1.0 MHz

Symbol	Parameter	Max	Notes
C _I	Digital Input	7 pF	6, Pins 1, 2, 6, 7, 16-18, 30-40, 44
C _O	Digital Output	7 pF	6, Pins 4, 8-15, 41-43
COA	Analog Output	TBD pF	6, 9; Pins 21-23

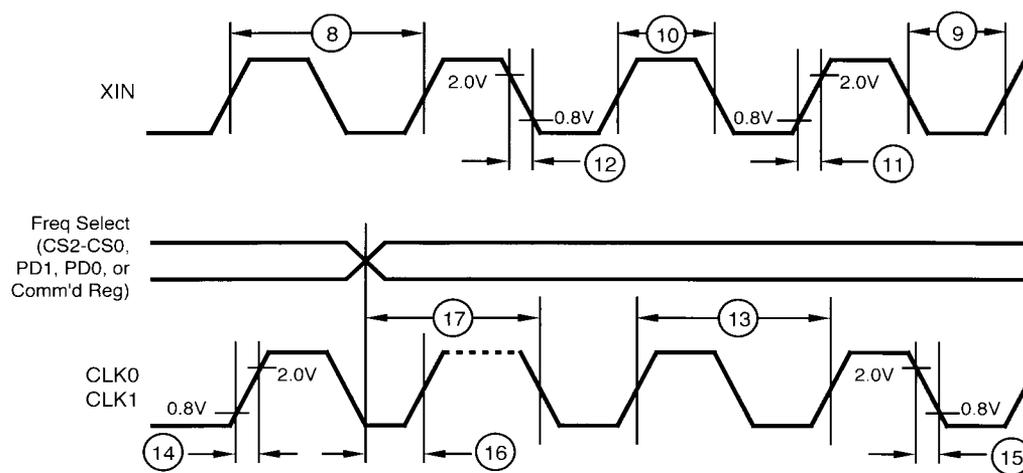
MU9C9760/V/A

TIMING DIAGRAMS

VIDEO PORT TIMING



CLOCK SYNTHESIZER TIMING

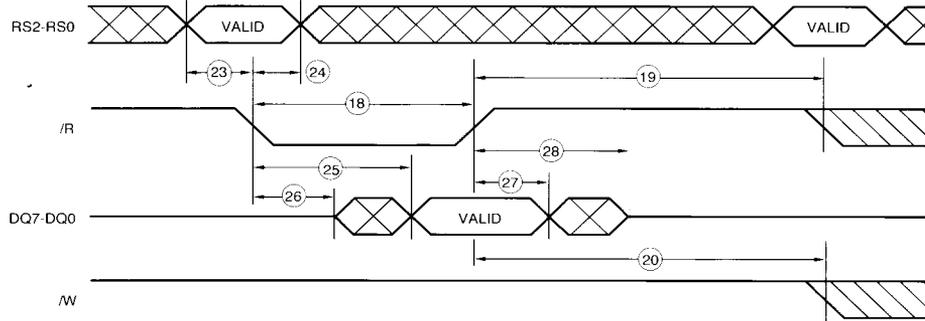


Rev. 1

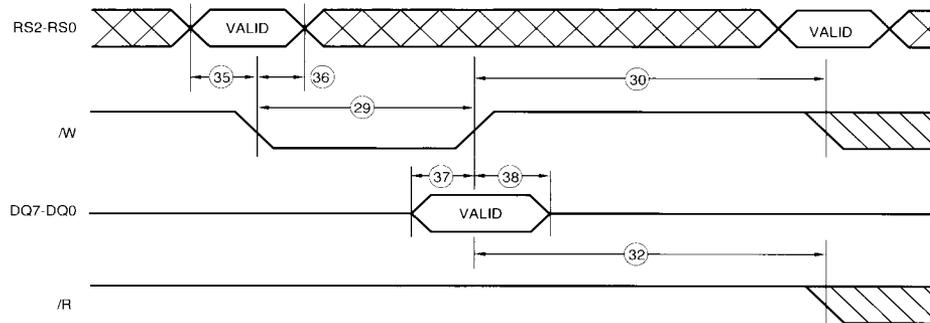
MU9C9760/V/A

TIMING DIAGRAMS (CONT'D)

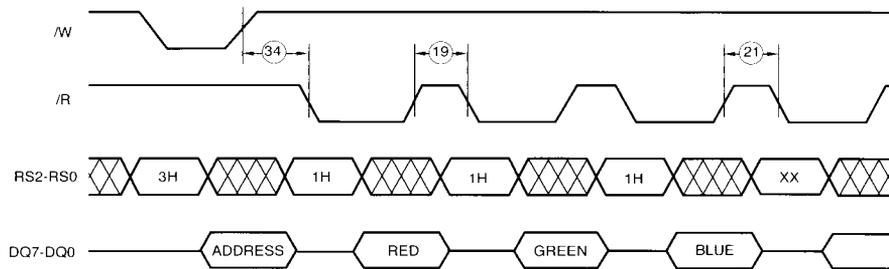
MICROPROCESSOR READ CYCLE



MICROPROCESSOR WRITE CYCLE



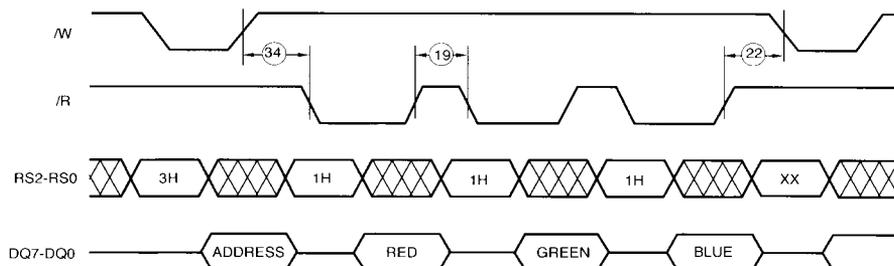
COLOR VALUE READ TO READ



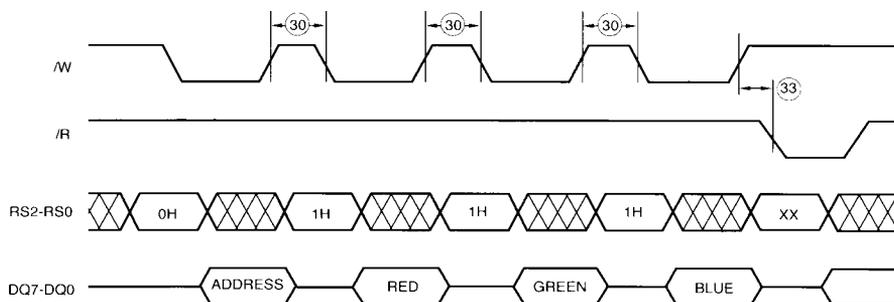
MU9C9760/V/A

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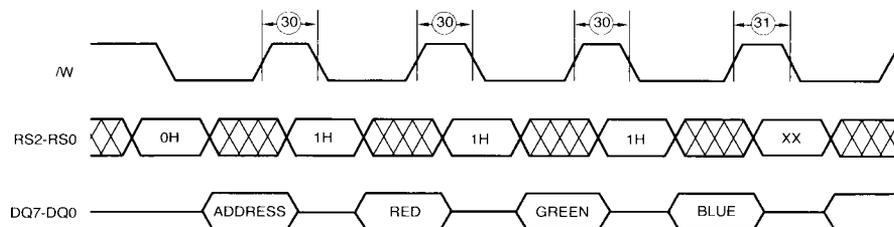
COLOR VALUE READ TO WRITE



READ AFTER COLOR VALUE WRITE



WRITE AFTER COLOR VALUE WRITE

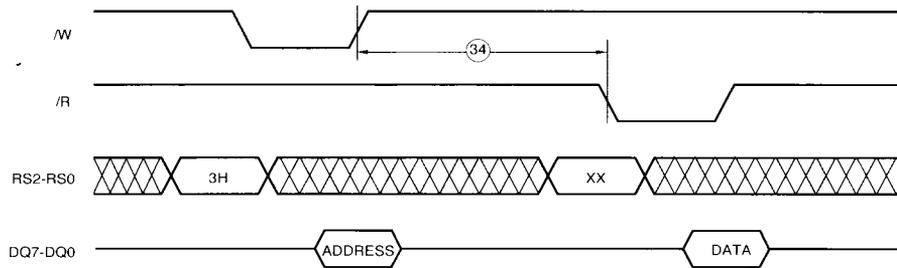


Rev. 1

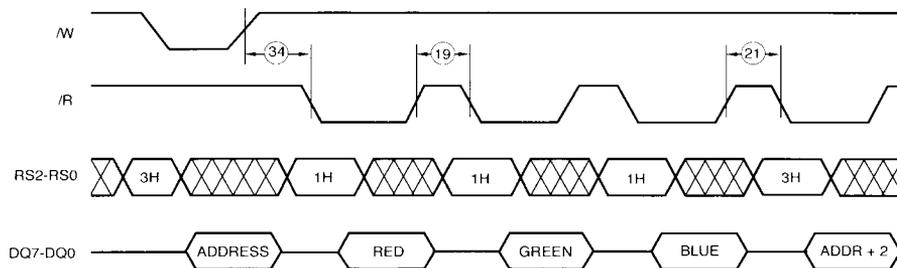
MU9C9760/V/A

TIMING DIAGRAMS (CONT'D)

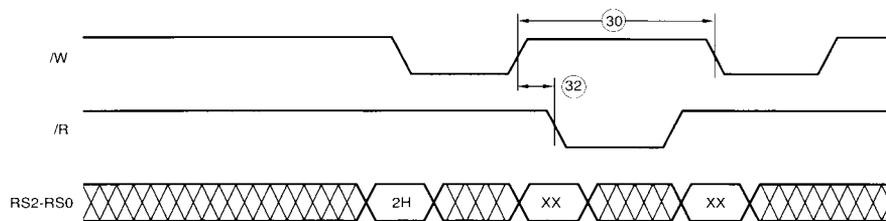
READ AFTER WRITING READ ADDRESS REGISTER



READ COLOR VALUE THEN READ ADDRESS



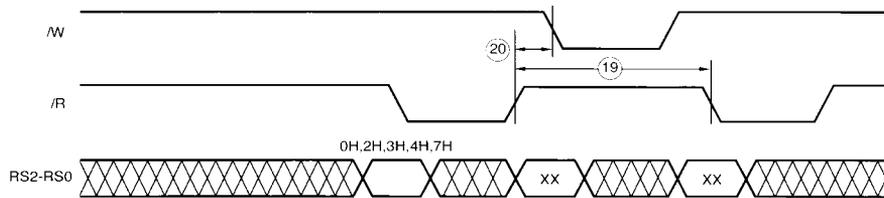
MASK REGISTER WRITE TO READ OR WRITE



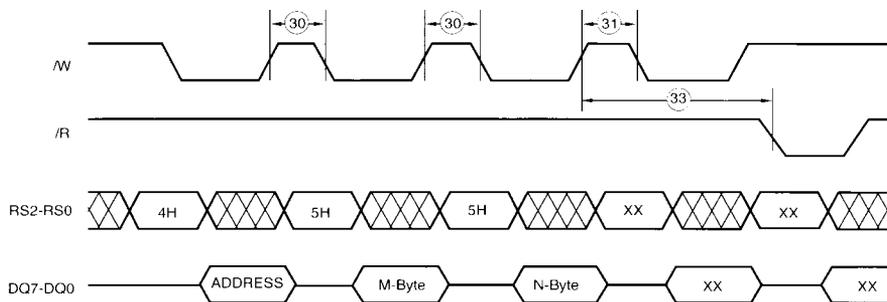
MU9C9760/V/A

TIMING DIAGRAMS (CONT'D)

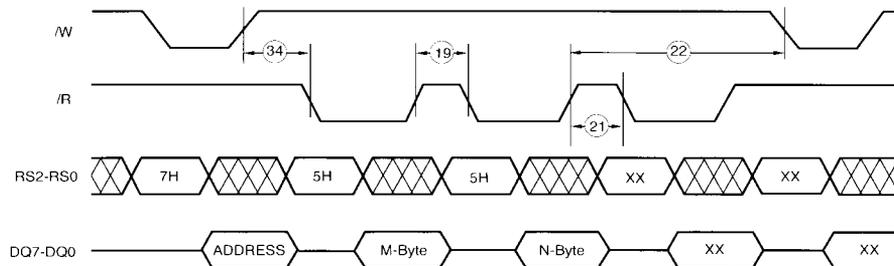
READ FROM MASK OR ADDRESS REGISTER TO READ OR WRITE



PLL PARAMETER WRITE



PLL PARAMETER READ

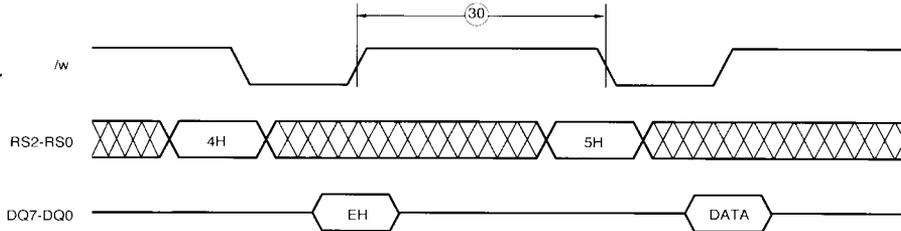


Rev. 1

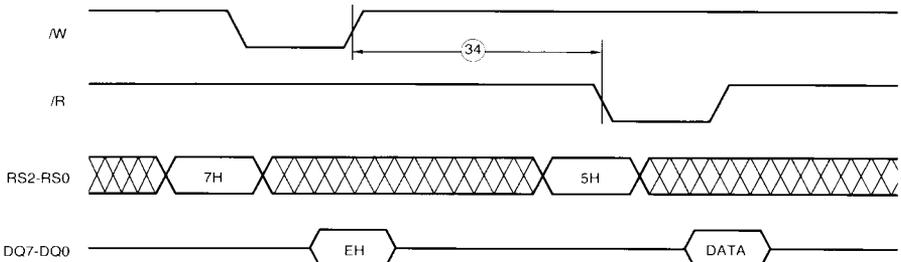
MU9C9760/V/A

TIMING DIAGRAMS (CONT'D)

PLL CONTROL REGISTER WRITE



PLL CONTROL REGISTER READ



WAVEFORM KEY

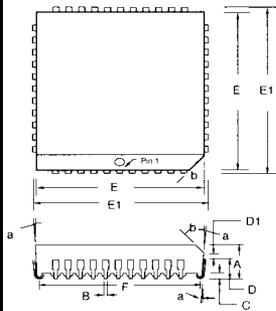
KEY		
WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care. Any change permitted	Undefined. State unknown
	Does not apply	Center line is high impedance "off state"

MU9C9760/V/A

ORDERING INFORMATION

PART NUMBER	SPEED	REFERENCE	PACKAGE	TEMPERATURE RANGE
MU9C9760-YYDC		CURRENT	44-PIN PLDCC	0-70°C
MU9C9760V-YYDC		VOLTAGE	44-PIN PLDCC	0-70°C
MU9C9760A-YYDC		VOLTAGE	44-PIN PLDCC	0-70°C
YY = 50	50MHz			
YY = 66	66MHz			
YY = 80	80MHz			

44-PIN PLDCC PACKAGE OUTLINE



Dim A	Dim B	Dim C	Dim D	Dim D1	Dim E
.170	.017	.033	.098	.050	.650
.176	TYP	.043	TYP	TYP	.656
Dim.E1	Dim.F	Dim.F1	Dim.a	Dim.b	
.685	.620	.050	3 ⁰	45 ⁰	
.695	.626	TYP	6 ⁰	TYP	

MUSIC Semiconductors

USA Headquarters
 MUSIC Semiconductors
 1150 Academy Park Loop, Suite 202
 Colorado Springs, CO 80910
 USA
 Tel: (1) 719-570-1550
 Fax: (1) 719-570-1555
 Tel within USA: (1) 800-933-1550

European Headquarters
 MUSIC Semiconductors
 Torenstraat 28
 PO Box 184
 6470 ED Eygelshoven
 The Netherlands
 Tel: +31 45 467878
 Fax: +31 45 467822

Far East Headquarters
 MUSIC Semiconductors
 3/F U-Warehouse Building
 Barangay Vitalez, NAIA Complex
 Parañaque, Metro Manila
 Philippines
 Tel: +63-2-834-2156
 Fax: +63-2-833-3959

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