COS/MOS INTEGRATED CIRCUITS

HCC/HCF 4032B HCC/HCF 4038B

TRIPLE SERIAL ADDERS

- INVERT INPUTS ON ALL ADDERS FOR SUM COMPLEMENTING APPLICATIONS
- FULLY STATIC OPERATION ..... DC TO 10 MHz (TYP.) @ V_{DD}= 10V
- BUFFERED INPUTS AND OUTPUTS
- SINGLE-PHASE CLOCKING
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED TO 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATING
- INPUT CURRENT OF 100 nA AT 18V and 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC/4032B/4038B** (extended temperature range) and **HCF 4032B/4038B** (intermediate temperature range) are monolithic integrated circuits, available in 16-lead dual in-line plastic or ceramic package and ceramic flat package.

The **HCC/HCF 4032B** and **HCC/HCF 4038B** types consist of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the **HCC/HCF 4032B** or at the negative-going clock for the **HCC/HCF 4038B**, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

ABSOLUTE MAXIMUM RATINGS

V_{DD}*	Supply voltage: **HCC** types	-0.5 to 20	V
	HCF types	-0.5 to 18	V
V_I	Input voltage	-0.5 to V_{DD} +0.5	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op}= full package-temperature range	100	mW
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C
T_{stg}	Storage temperature	-65 to 150	°C

* All voltage values are referred to V_{SS} pin voltage

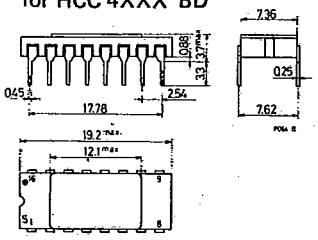
ORDERING NUMBERS:

HCC 4XXX BD for dual in-line ceramic package
HCC 4XXX BF for dual in-line ceramic package, frit seal
HCC 4XXX BK for ceramic flat package
HCF 4XXX BE for dual in-line plastic package
HCF 4XXX BF for dual in-line ceramic package, frit seal

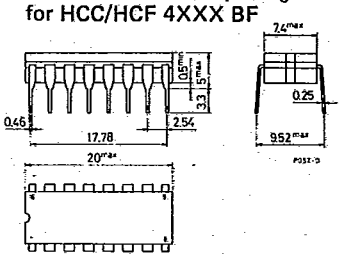
HCC/HCF 4032B
HCC/HCF 4038B

MECHANICAL DATA (dimensions in mm)

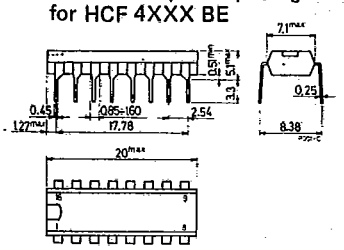
Dual in-line ceramic package for HCC 4XXX BD



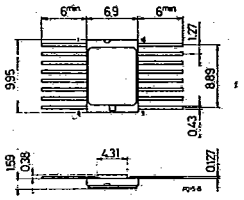
Dual in-line ceramic package for HCC/HCF 4XXX BF



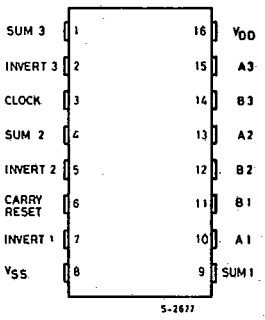
Dual in-line plastic package for HCF 4XXX BE



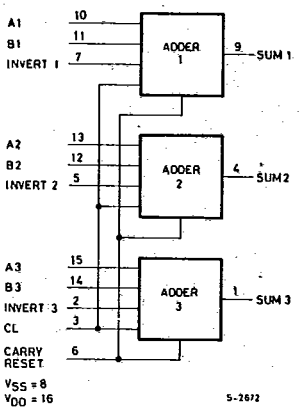
Ceramic flat package for HCC 4XXX BK



CONNECTION DIAGRAM



FUNCTIONAL DIAGRAM

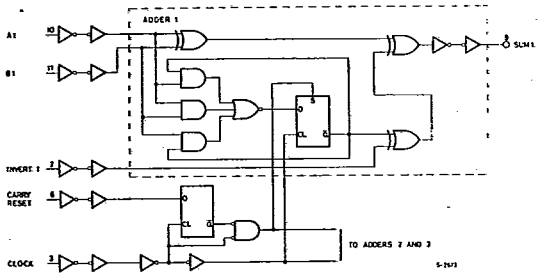


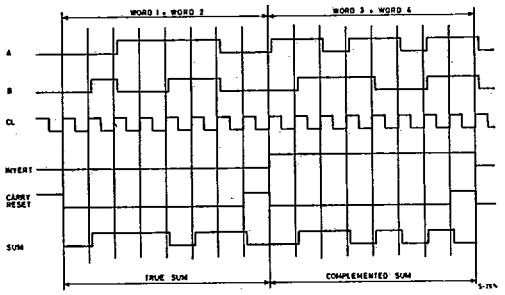
RECOMMENDED OPERATING CONDITIONS

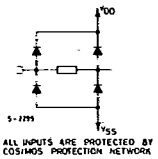
V_{DD}	Supply voltage: **HCC** types	3 to 18	V
	HCF types	3 to 15	V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: **HCC** types	-55 to 125	°C
	HCF types	-40 to 85	°C

LOGIC AND TIMING DIAGRAMS (One of three serial adders)

For 4032B

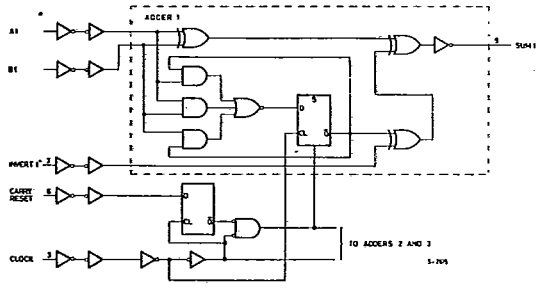


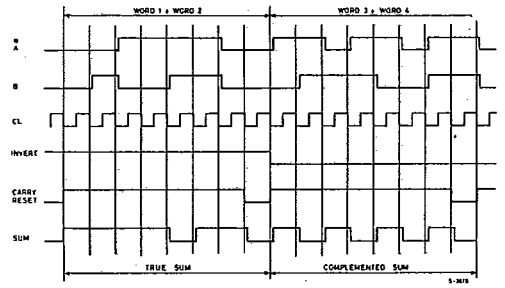


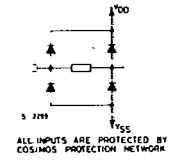


WORD 1	0.0111100 = + 60	WORD 3	1.1011011 = - 37
WORD 2	0.0110010 = + 50	WORD 4	1.1001110 = - 50
	0.1101110 = + 110		1.0101001 = - 87

For 4038B







WORD 1	1.1000011 = - 61	WORD 3	0.0100100 = + 36
WORD 2	1.1001101 = - 51	WORD 4	0.0110001 = + 49
	1.0010000 = - 112		0.1010101 = + 85

HCC/HCF 4032B
HCC/HCF 4038B

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter			Test conditions				Values							Unit
			V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}* Min.	T_{Low}* Max.	25°C Min.	25°C Typ.	25°C Max.	T_{High}* Min.	T_{High}* Max.	
I_L	Quiescent current	HCC types	0/ 5			5		5		0.04	5		150	μA
			0/10			10		10		0.04	10		300	
			0/15			15		20		0.04	20		600	
			0/20			20		100		0.08	100		3000	
		HCF types	0/ 5			5		20		0.04	20		150	
			0/10			10		40		0.04	40		300	
			0/15			15		80		0.04	80		600	
V_{OH}	Output high voltage		0/ 5		< 1	5	4.95		4.95			4.95		V
			0/10		< 1	10	9.95		9.95			9.95		
			0/15		< 1	15	14.95		14.95			14.95		
V_{OL}	Output low voltage		5/0		< 1	5		0.05			0.05		0.05	V
			10/0		< 1	10		0.05			0.05		0.05	
			15/0		< 1	15		0.05			0.05		0.05	
V_{IH}	Input high voltage			0.5/4.5	< 1	5	3.5		3.5			3.5		V
				1/9	< 1	10	7		7			7		
				1.5/13.5	< 1	15	11		11			11		
V_{IL}	Input low voltage			4.5/0.5	< 1	5		1.5			1.5		1.5	V
				9/1	< 1	10		3			3		3	
				13.5/1.5	< 1	15		4			4		4	
I_{OH}	Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
			0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
			0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
			0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		HCF types	0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
			0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
			0/10	9.5		10	-1.3		-1.1	-2.6		-0.9		
			0/15	13.5		15	-3.6		-3.0	-6.8		-2.4		
I_{OL}	Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
			0/10	0.5		10	1.6		1.3	2.6		0.9		
			0/15	1.5		15	4.2		3.4	6.8		2.4		
		HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
			0/10	0.5		10	1.3		1.1	2.6		0.9		
			0/15	1.5		15	3.6		3.0	6.8		2.4		
I_{IH}, I_{IL}	Input leakage current	HCC types	0/18	Any input		18		±0.1		$±10^{-5}$	±0.1		± 1	μA
		HCF types	0/15			15		±0.3		$±10^{-5}$	±0.3		± 1	
C_I	Input capacitance			Any input						5	7.5			pF

* T_{Low} = − 55°C for **HCC** device: −40°C for **HCF** device.
* T_{High} = +125°C for **HCC** device: +85°C for **HCF** device.
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}= 5V
2V min. with V_{DD}= 10V
2.5V min. with V_{DD}= 15V

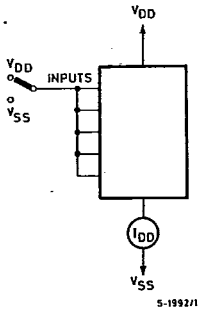
DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50 pF, R_L = 200 kΩ, all input rise and fall time = 20 ns)

Parameter		Test conditions	Values			Unit
		V_{DD} (V)	Min.	Typ.	Max.	
t_{PHL}, t_{PLH}	Propagation delay time A, B, or Inverter Inputs to Sum Outputs	5		260	520	ns
		10		120	240	
		15		90	180	
t_{PHL}, t_{PLH}	Propagation delay time (clock Input to Sum Outputs)	5		325	650	
		10		175	350	
		15		150	300	
t_{THL}, t_{THL}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{hold}	Data input hold time (Clock Edge to A, B, or Resetinputs)	5		120	200	ns
		10		50	80	
		15		40	60	
f_{max}	Maximum clock input frequency	5	2.5	4.5		MHz
		10	5	10		
		15	7.5	15		
t_r, t_f*	Clock input rise or fall time	5			500	μs
		10			500	
		15			500	

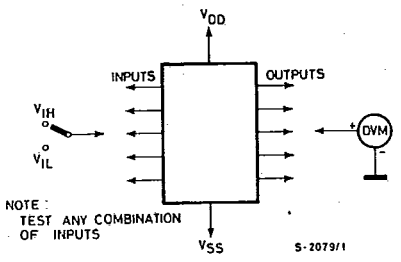
* If more than one unit is cascaded t_r should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

TEST CIRCUITS

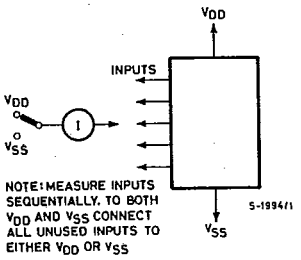
Quiescent device current



Input voltage

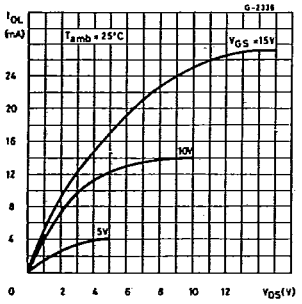


Input current

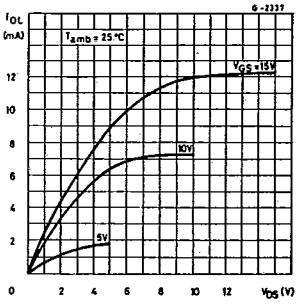


HCC/HCF 4032B
HCC/HCF 4038B

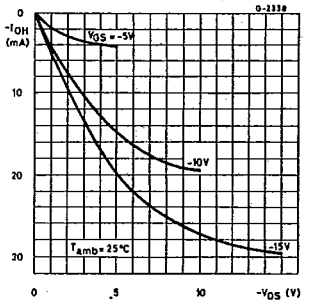
Typical output low (sink) current



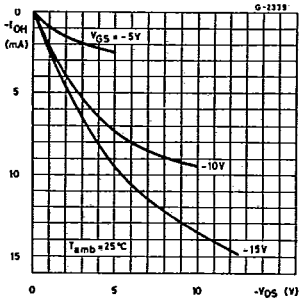
Minimum output low (sink) current characteristics

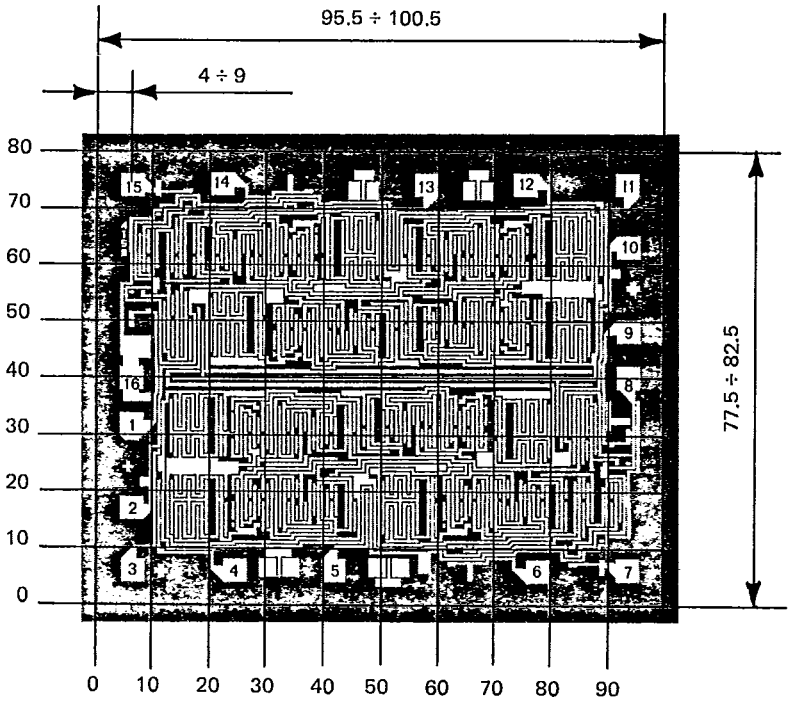


Typical output high (source) current characteristics

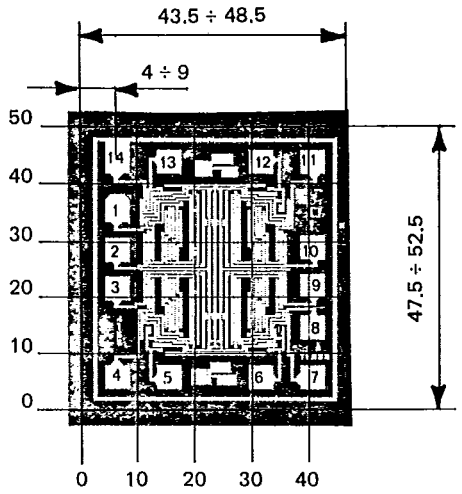


Minimum output high (source) current characteristics




95.5 ÷ 100.5
4 ÷ 9
77.5 ÷ 82.5
80
70
60
50
40
30
20
10
0
0 10 20 30 40 50 60 70 80 90
15 14 13 12 11 10 9 8 16 1 2 3 4 5 6 7

4015B


43.5 ÷ 48.5
4 ÷ 9
47.5 ÷ 52.5
50
40
30
20
10
0
0 10 20 30 40
14 13 12 11 1 2 3 10 9 8 4 5 6 7

4016B