Product Specification

AHA G.709-2.5 FEC Encoder Core

PSFECEncoderCore_0702

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1.0 INTRODUCTION

This G.709-2.5 core implements the RS(255,239) code specified in Annex A of the ITU G.709 standard. It is designed to efficiently perform the Reed Solomon encoding function specified by the standard. The core requires no configuration, no initialization, and no resynchronization procedure.

1.1 FEATURES

PERFORMANCE:

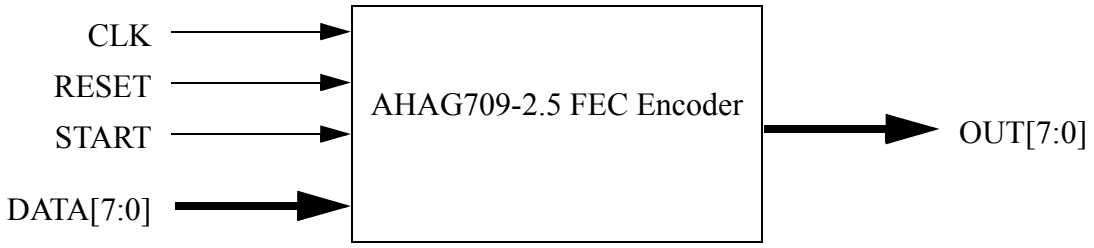
- ITU G.709 Compatible Reed Solomon core
- 2.5 Gbits/sec operation in 0.13 micron CMOS process with 332 MHz clock
- One-edge, one clock fully synchronous design
- Two clock latency
- 1K gates
- Only initialization is a RESET
- 8 bit input and output data interfaces

DELIVERABLES:

- ITU G.709 compatible RS Encoder core VHDL
- Timing constraints (Design Compiler and Ambit format)
- Test bench and verification vectors (VHDL)

2.0 FUNCTIONAL DESCRIPTION

Figure 1: BLOCK DIAGRAM



2.1 ENCODING

Uncoded block length is 239 Bytes with 16 check Bytes and a correction power of 8 Bytes per block. Latency through the encoder is two clocks. A global reset clears all of the flip-flops involved with generating the parity check bytes.

Processing begins by applying the first data byte on the DATA bus, asserting the START signal, and then asserting the CLK signal. Every input byte is then added with the REG15 output and the sum input to all the Galois Field constant multipliers (GFMx). The outputs of these multipliers are summed with the previous stage value and clocked into the next register stage. After processing all 239 bytes in this manner the 16 parity check bytes are strobed out. This process of strobing out the parity check bytes reinitializes the register stages in preparation for processing the next block, thus not requiring any additional RESET pulses.

2.2 REED SOLOMON CODE PARAMETERS

generator polynomial:

$$G(z) = \prod_{i=0}^{15} (z - \alpha^i)$$

where α is a root of the binary primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$.

Parity bytes are represented by:

$$R(z) = R_{15} \cdot z_{15} + R_{14} \cdot z_{14} \ldots + R_1 \cdot z_1 + R_0$$

where R_j (j = 0 to 15) is the parity byte represented by an element out of GF(256) and R_{15} corresponds to the byte 240 in the FEC sub-row and R_0 to byte 255.

3.0 SIGNAL DESCRIPTIONS

3.1 INPUT INTERFACE

Signal	*Type*	*Description*
DATA[7:0]	I	Data Bus. Input data bus for information word.
START	I	Block start signal. This signal is asserted with the first byte transfer of a block. Start signals should be at least 255 clocks apart, but can be more than 255 clocks.
CLK	I	System Clock.
RESET	I	Global Reset. When active (high) RESET forces a reset on all of the flip-flops involved in parity generation.

3.2 OUTPUT INTERFACE

Signal	*Type*	*Description*
OUT[7:0]	O	Output data bus. Message Bytes are passed through onto this bus followed by the 16 parity check bytes for each 239 Byte block that is processed.

4.0 TIMING DIAGRAMS

Figure 2: FUNCTIONAL TIMING