May 1992
Revision 1C

Related Product Literature:
- Integrated Development System
- CLi6000 Series Configuration
- CLi6000 Series Prototype Kit
- CLi6000 Series Download Board
- CLi6000 Series Application Notes

Concurrent Logic, Inc.

CLi6000 Series Field-Programmable Gate Arrays

CLi6000 Series FPGAs provide the density and performance of custom gate arrays without the prototyping and debugging delays associated with mask-programmed devices.

Supporting system speeds of up to 70 MHz and using a typical operating current of 50–70 mA, CLi6000 Series devices offer superior performance, predictability and silicon utilization. These FPGAs are infinitely reprogrammable, so they reduce design risk, shorten design cycles and speed time to market.

The patented CLi6000 Series architecture employs a symmetrical grid of small yet powerful cells connected to a flexible bussing network. Independently controlled clocks and resets govern every column of cells. The array is surrounded by programmable I/O.

Devices range in size from 1,200 to 10,000 usable gates. Pin locations are consistent throughout the Series for easy design migration. High-I/O versions are available for the lower gate count devices.

CLi6000 Series FPGAs utilize a reliable 0.8 µm single-poly, double-metal CMOS process and are 100% factory-tested.

Concurrent Logic's PC-based Integrated Development System is used to create CLi6000 Series designs.

FEATURES

High Performance
- System Speeds to 70 MHz
- Flip-Flop Toggle Rates to 150 MHz

Symmetrical Architecture
- Thousands of Registers
- Flexible Busing Network
- Complete/Partial In-System Reconfiguration
- Predictable Timing Delays
- 100% Factory-Tested

Very Low Power Consumption
- Standby Current of 500 µA
- Typical Operating Current of 50–70 mA

Programmable Clock Options
- Independently Controlled Column Clocks
- Independently Controlled Column Resets
- Clock Skew Less Than 1 ns Across Chip

Configurable I/O
- High-I/O Versions for Low-Density Devices
- TTL/CMOS Input Thresholds
- Open Collector/Tristate Outputs
- Programmable Slew Rate Control
- I/O Drive to 12 mA (Combinable to 48 mA)
- Registered/Direct Inputs and Outputs

Table 1. The CLi6000 Series of Field-Programmable Gate Arrays (Shaded Box Indicates Available Device)

Device	CLi6001	CLi6002	CLi6003	CLi6004	CLi6005	CLi6006	CLi6008	CLi6010
Capacity, Gates	1200	2000	3000	4000	5000	6000	8000	10000
Cells	576	1024	1600	2304	3136	4096	5184	6400
Registers (maximum)	576	1024	1600	2304	3136	4096	5184	6400
I/O (maximum)	64	96	108	108	108	128	144	160
Operating Current (mA)	15	30	45	60	80	110	140	170
Cell Rows x Columns	24x24	32x32	40x40	48x48	56x56	64x64	72x72	80x80

GENERAL DESCRIPTION

The Concurrent Logic architecture was developed to provide the highest levels of performance, functional density and design flexibility in a Field-Programmable Gate Array (FPGA). The cells in the Concurrent Logic array are small, very efficient and contain the most important and most commonly used logic and wiring functions. The cell's small size leads to arrays with large numbers of cells, greatly multiplying the functionality in each cell. A simple, high-speed busing network provides fast, efficient communication over medium and long distances.

The Symmetrical Array

At the heart of the Concurrent Logic architecture is a symmetrical array of identical cells (Figure 1). Except for "repeaters" spaced every eight cells (Figure 2), the array is continuous and completely uninterrupted from one edge to the other.

In addition to logic and storage, cells can also be used as wires to connect functions together over short distances and are useful for routing in tight spaces. Buses support fast, efficient communication over medium and long distances.

The Busing Network

There are two kinds of buses: local and express (Figures 2 and 3).

Local buses are the link between the array of cells and the busing network. There are two local buses —North-South 1 and 2 (NS1 and NS2)—for every column of cells, and two local buses—East-West 1 and 2 (EW1 and EW2)—for every row of cells. Each local bus is connected to every cell in its column or row, thus providing every cell in the array with read/write access to two North-South and two East-West buses.

Each cell, in addition, provides the ability to make a 90° turn between either of the two North-South buses and either of the two East-West buses.

Express buses are not connected directly to cells and, thus, provide higher speeds. They are the fastest way to cover long, straight-line distances within the array.

Each express bus is paired with a local bus, so there are two express buses for every column and two express buses for every row of cells.

Connective units, called repeaters, spaced every eight cells, divide each bus—both local and express —into segments spanning eight cells. Repeaters are aligned in rows and columns thereby partitioning the array into 8 x 8 sectors of cells. Each repeater is associated with a local/express pair, and on each side of the repeater are connections to a local-bus segment and an express-bus segment. The repeater

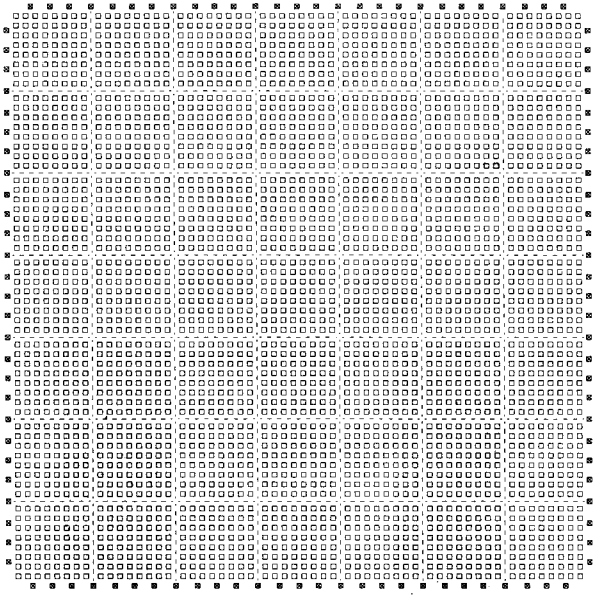


Figure 1. Symmetrical Array Surrounded by I/O

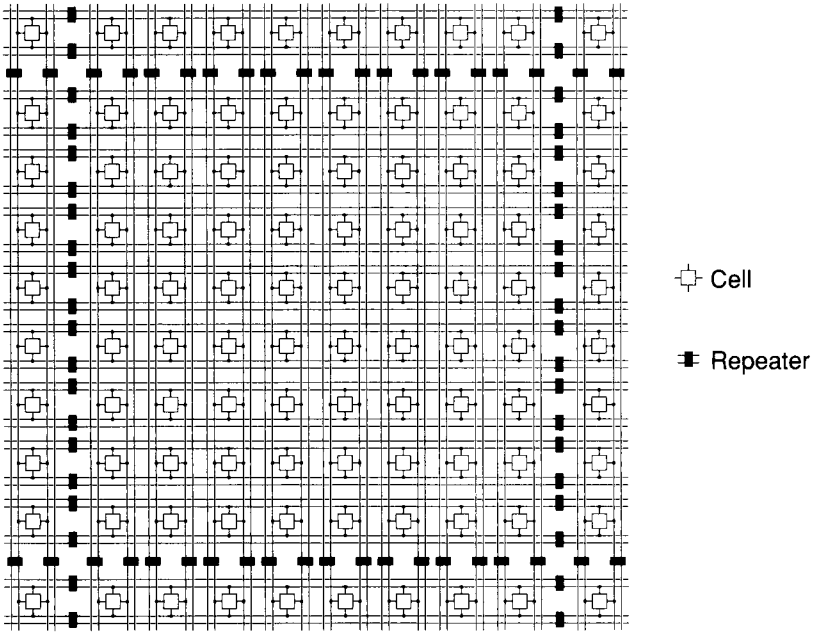


Figure 2. Busing Network

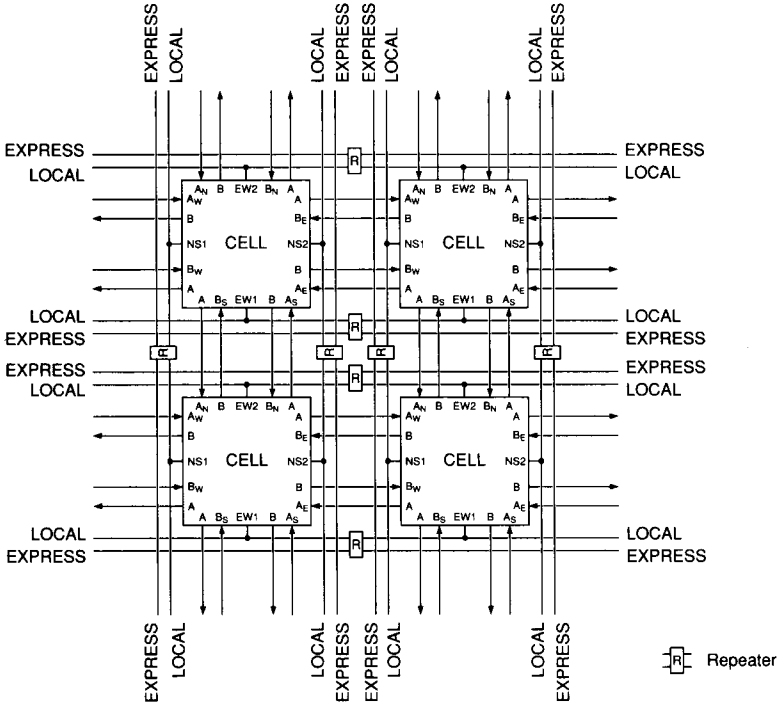


Figure 3. Cell-to-Cell and Cell-to-Bus Connections

can be programmed to provide any one of twenty-nine connecting functions. These functions are symmetric with respect to both the two repeater sides and the two types of buses.

Among the functions provided are the ability to:

- Isolate bus segments from one another
- Connect two local-bus segments
- Connect two express-bus segments
- Implement a local/express transfer

In all of these cases, each connection provides signal regeneration and is thus unidirectional. For bidirectional connections, the basic repeater function for the NS1 and EW2 repeaters is augmented with a special programmable connection allowing bidirectional communication between local-bus segments. This option is primarily used to implement long, tristate buses.

The Cell Structure

The Concurrent Logic cell (Figure 4) is simple and small and yet can be programmed to perform all the logic and wiring functions needed to implement any digital circuit. Because its four sides are functionally identical, each cell is completely symmetrical.

Read/write access to the four local buses—NS1, NS2, EW1 and EW2—is provided by four bidirectional pass gates. When one pass gate is active (conducting), reading is controlled by a pair of two-input multiplexers feeding two "upstream" AND gates. Writing is by a tristate driver under the control of a three-input multiplexer.

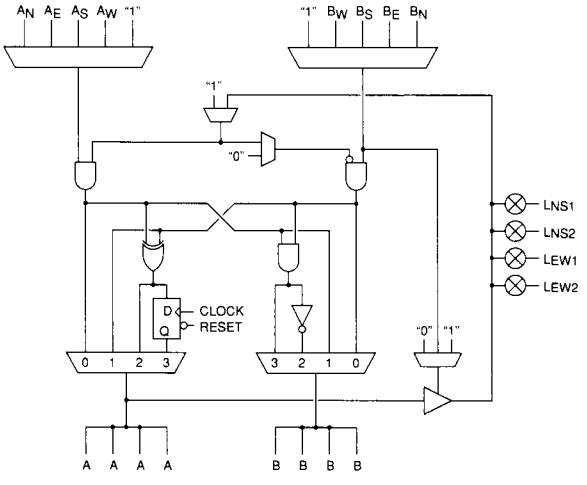


Figure 4. Cell Structure

In addition to the four local-bus connections, a cell receives eight inputs and provides two outputs to its North (N), South (S), East (E) and West (W) neighbors. These ten inputs and outputs are divided into two classes: "A" and "B." There is an A input and a B input for each neighboring cell and a single A output and single B output driving all four neighbors. Between cells, an A output is always connected to an A input and a B output to a B input.

Within the cell, the four A inputs and the four B inputs enter two separate, independently configurable multiplexers. Cell flexibility is enhanced by allowing each multiplexer to select also the logical constant "1." The two multiplexer outputs enter the two upstream AND gates.

Downstream from these two AND gates are an Exclusive-OR (XOR) gate, a register, a downstream AND gate, an inverter and two four-input multiplexers producing the A and B outputs. These multiplexers are controlled in tandem (unlike the A and B input multiplexers) and determine the function of the cell.

- In State 0—corresponding to the "0" inputs of the multiplexers—the output of the left-hand upstream AND gate is connected to the cell's A output, and the output of the right-hand upstream AND gate is connected to the cell's B output.
- In State 1—corresponding to the "1" inputs of the multiplexers—the output of the left-hand upstream AND gate is connected to the cell's B output, the output of the right-hand upstream AND gate is connected to the cell's A output.
- In State 2—corresponding to the "2" inputs of the multiplexers—the XOR of the outputs from the two upstream AND gates is provided to the cell's A output, while the NAND of these two outputs is provided to the cell's B output.
- In State 3—corresponding to the "3" inputs of the multiplexers—the XOR function of State 2 is provided to the D input of a D-type flip-flop, the Q output of which is connected to the cell's A output. Clock and asynchronous reset signals are supplied externally as described later. The AND of the outputs from the two upstream AND gates is provided to the cell's B output.

Logic States

The Concurrent Logic cell implements a rich and powerful set of logic functions, stemming from forty-four cell states. Some states use both A and B inputs. Other states are created by selecting the "1" input on either or both of the input multiplexers.

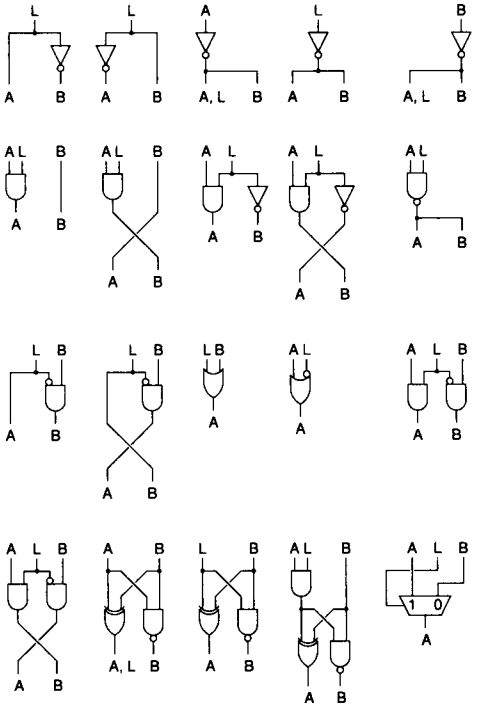


Figure 5a. Combinatorial States

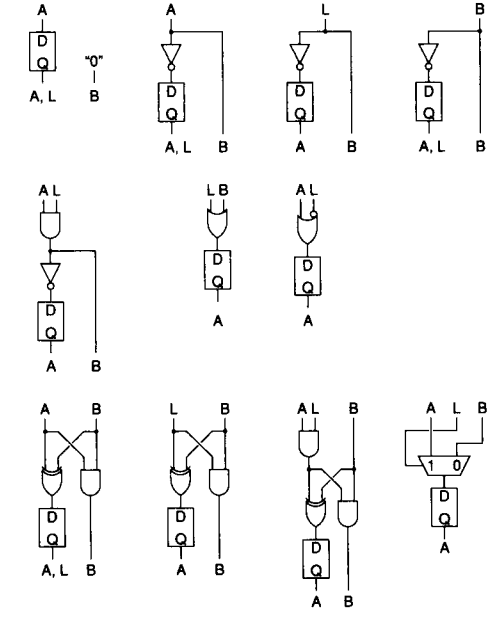


Figure 5b. Register States

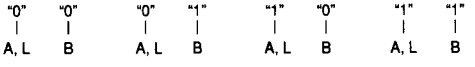
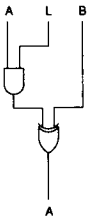


Figure 5c. Constant States

There are twenty-five purely combinatorial states with a range of functions, including NOR, AND, NAND, OR and two-input multiplexer (Figure 5a). There are eleven register states ranging from a simple register to a register preceded by a two-input multiplexer (Figure 5b). Five constant states produce all combinations of constant values at the two cell outputs (Figure 5c). There are five tristate states. More complex functions are created by using cells in combination.



(A•L) XOR B

Figure 6a. 2-Input AND Feeding XOR

A 2-input AND feeding an XOR (Figure 6a) is produced using a single cell (Figure 6b). The downstream 2-1 multiplexer selects the logical constant "0" and feeds it to the right-hand AND gate. The AND gate acts as a feed-through, letting the B input pass through to the XOR. The upstream 2-1 multiplexer selects the local-bus input, L, and passes it to the left-hand AND gate. The A and L signals are the inputs to the AND gate. The output of the AND gate feeds into the XOR, producing the logic state (A•L) XOR B.

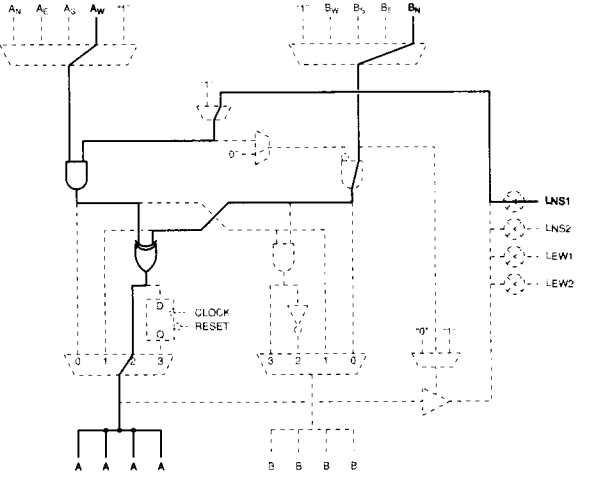


Figure 6b. Cell Configuration: (A•L) XOR B

Clock Distribution

Along the top edge of the array is logic for distributing clock signals to the D flip-flop in each logic cell (Figure 7). The distribution network is organized by column and permits columns of cells to be independently clocked. At the head of each column is a user-configurable multiplexer providing the clock signal for that column. It has four inputs:

- Global clock supplied through the CLOCK pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the head of the $\overline{\text{COLUMN}}$
- Logical constant "1"

Through the global clock, the network provides low-skew distribution of an externally supplied clock to any or all the columns of the array. The global clock pin is also connected directly to the array via the A input of the upper left and right corner cells (A_W on the left, and A_N on the right). The express bus is useful in distributing a secondary clock to multiple columns when the global clock line is used as a primary clock. The A output of a cell is useful in providing a clock signal to a single column. The constant "1" is used to reduce power dissipation in columns using no registers.

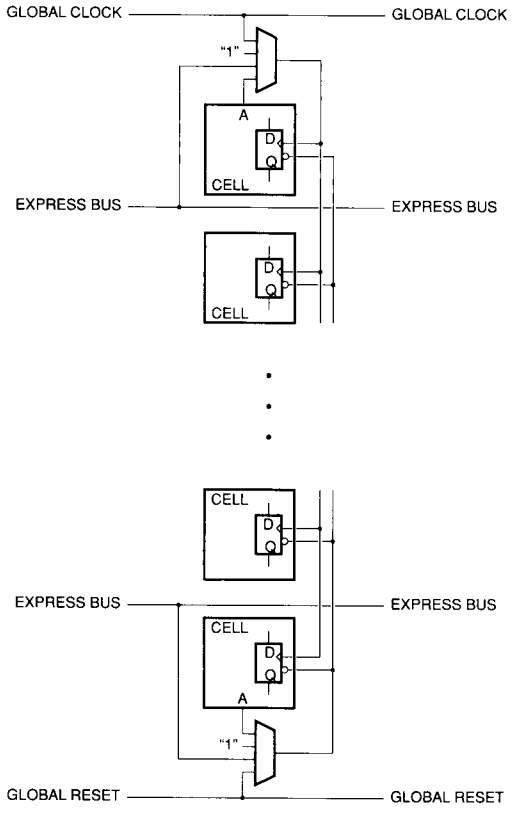


Figure 7. Column Clock and Column Reset

Asynchronous Reset

Along the bottom edge of the array is logic for asynchronously resetting the D flip-flops in the logic cells (Figure 7). Like the clock network, the asynchronous reset network is organized by column and permits columns to be independently reset. At the bottom of each column is a user-configurable multiplexer providing the reset signal for that column. It has four inputs:

- Global asynchronous reset supplied through the $\overline{\text{RESET}}$ pin
- Express bus adjacent to the distribution logic
- "A" output of the cell at the foot of the $\overline{\text{COLUMN}}$
- Logical constant "1"

The asynchronous reset logic uses these four inputs in the same way that the clock distribution logic does. Through the global asynchronous reset, any or all columns can be reset by an externally supplied signal. The global asynchronous reset pin is also connected directly to the array via the A input of the lower left and right corner cells (A_S on the left, and A_E on the right). The express bus can be used to distribute a secondary reset to multiple columns when the global reset line is used as a primary reset, the A output of a cell can also provide an asynchronous reset signal to a single column, and the constant "1" is used by columns with registers requiring no reset. All registers are reset during power-up.

Input/Output

The Concurrent Logic architecture provides a flexible interface between the logic array, the configuration control logic and the I/O pins.

Two adjacent cells—an "exit" and an "entrance" cell—on the perimeter of the logic array are associated with each I/O pin.

There are two types of I/Os: A-type (Figure 8a) and B-type (Figure 8b). For A-type I/Os, the edge-facing A output of an exit cell is connected to an output driver, and the edge-facing A input of the adjacent entrace cell is connected to an input buffer. The output of the output driver and the input of the input buffer are connected to a common pin.

B-type I/Os are the same as A-type I/Os, but use the B inputs and outputs of their respective entrance

and exit cells. A- and B-type I/Os alternate around the array.

Control of the I/O logic is provided by user-configurable memory bits.

TTL/CMOS Inputs

A user-configurable bit determining the threshold level—TTL or CMOS—of the input buffer.

Open Collector/Tristate Outputs

A user-configurable bit which enables or disables the active pull-up of the output device.

Slew Rate

A user-configurable bit which controls the slew rate—fast or slow—of the output buffer. A slow slew rate, which reduces noise and ground bounce, is recommended for outputs that are not speed-critical. Fast and slow slew rates have the same DC-current sinking capabilities, but the rate at which each allows the output devices to reach full drive differs.

Pull-up

A user-configurable bit controlling the pull-up transistor in the I/O pin. It's primary function is to provide a logical "1" to unused input pins. When on, it is roughly equivalent to a 25k resistor to V_{CC}.

Enable Select

User-configurable bits determining the output-enable for the output driver. The output driver can be static, always on, always off, or dynamically controlled by a signal generated in the array. Four options are available from the array: (1) the control is low and always driving; (2) the control is high and never driving; (3) the control is connected to a vertical local bus associated with the output cell; and (4) the control is connected to a horizontal local bus associated with the output cell. The power-up default is never driving.

In addition to the functionality provided by the I/O logic, the entrance and exit cells provide the ability to register both inputs and outputs. Also, these perimeter cells (unlike interior cells) are connected directly to express buses: the edge-facing A and B outputs of the entrance cell are connected to express buses, as are the edge-facing A and B inputs of the exit cell. These buses are perpendicular to the edge, and provide a rapid means of bringing I/O signals to and from the array interior and the opposite edge of the chip.

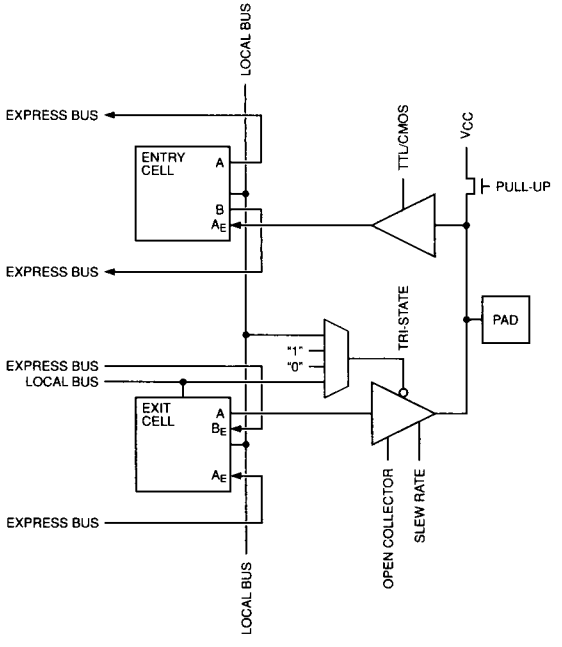


Figure 8a. A-Type I/O Logic

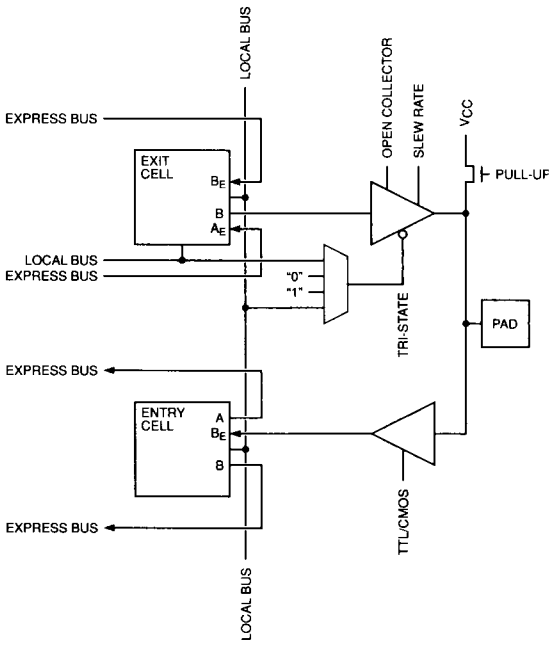


Figure 8b. B-Type I/O Logic

CHIP CONFIGURATION

The Integrated Development System generates the SRAM bit pattern required to configure a CLi6000 Series device. A PC parallel port, microprocessor or EPROM can be used to download configuration patterns.

Users select from seven configuration modes. Many factors, including board area, configuration speed and the number of designs implemented in parallel can influence the user's final choice:

- Mode 0: Configuration Reset
- Mode 1: Address Count-Up, External CCLK
- Mode 2: Address Count-Down, External CCLK
- Mode 3: Bit-Sequential, External CCLK
- Mode 4: Bit-Sequential, Internal CCLK
- Mode 5: Address Count-Up, Internal CCLK
- Mode 6: Byte-Sequential, External CCLK

Configuration is controlled by dedicated configuration pins and dual-function pins that double as I/O pins when the device is in operation. The number of dual-function pins required for each mode varies:

Mode	Dual-Function Pins Used
0	0
1, 2, 5	25
3, 4	1
6	8

The devices can be partially reconfigured while in operation. Portions of the device not being modified remain operational during configuration. Simultaneous configuration of more than one device is also possible. Full configuration takes as little as a millisecond, partial configuration is even faster.

Refer to the Pin Description section below for a brief summary of the pins used in configuration. For more information about configuration, refer to the CLi6000 Series Configuration Data Sheet.

PIN DESCRIPTIONS

This section provides abbreviated descriptions of the various CLi6000 Series pins. For more complete descriptions, refer to the CLi6000 Series Configuration Data Sheet.

Pinout tables for the CLi6005 and CLi6002 devices appear on pages ten and eleven.

Power Pins

V_{CC}, V_{DD}, GND, V_{SS}

V_{CC} and GND are the I/O supply pins, V_{DD} and V_{SS} are the internal logic supply pins. V_{CC} and V_{DD} should be tied to the same trace on the printed circuit board. GND and V_{SS} should be tied to the same trace on the printed circuit board.

Input/Output Pins

All I/O pins can be used in the same way (refer to the I/O section of the architecture description). Some I/O pins are dual-function pins used during configuration of the array. When not being used for configuration, dual-function I/Os are fully functional as normal I/O pins. On initial power-up, all I/Os are configured as TTL inputs with a pull-up.

Dedicated Timing and Control Pins

$\overline{CON}$

Configuration in process pin. After power-up, $\overline{CON}$ remains low until power-up initialization is complete. $\overline{CON}$ is an open collector signal. After power-up initialization, forcing $\overline{CON}$ low begins the configuration process.

$\overline{CS}$

Configuration enable pin. All configuration pins are ignored if $\overline{CS}$ is high. $\overline{CS}$ must be held low throughout the configuration process. $\overline{CS}$ is a TTL-type input pin.

M0, M1, M2

Configuration mode pins used to determine the configuration mode. All three are TTL-type input pins.

CCLK

Configuration clock pin. CCLK is an input or an output depending on the configuration mode selected. It is an output in two modes. The output modes support configuration using the fewest external components. In either of these modes,

the configuration time will vary from part to part depending on clock speed. CCLK is a TTL-type input in modes that use it as an input and a CMOS-type output in those modes that use it as an output. When not in use, CCLK is set low.

CLOCK
External logic source used to drive the internal global clock line. Registers toggle on the rising edge of CLOCK. The CLOCK signal is neither used nor affected by the configuration modes. It is always a TTL input.

$\overline{\text{RESET}}$
Array register asynchronous reset. $\overline{\text{RESET}}$ drives the internal global reset. The $\overline{\text{RESET}}$ signal is neither used nor affected by the configuration modes. It is always a TTL input.

Dual-Function Pins

When $\overline{\text{CON}}$ is high, dual-function I/O pins act as device I/Os; when $\overline{\text{CON}}$ is low, dual-function pins are used as configuration control or data signals as determined by the configuration modes. Care must be taken when using these pins to ensure that configuration activity does not interfere with other circuitry associated with the pin's net.

D0 or I/O
Serial configuration modes use D0 as the serial data input pin. Parallel configuration modes use D0 as the least-significant bit. Input data must meet setup and hold requirements with respect to the rising edge of CCLK.

D1 to D7 or I/O
Parallel configuration modes use these pins as inputs. Serial configuration modes do not use them. Data must meet setup and hold requirements with respect to the rising edge of CCLK.

$\overline{\text{CEN}}$ or I/O
During address count-up/down configuration, $\overline{\text{CEN}}$ is an output. $\overline{\text{CEN}}$ can be used as the output enable of a parallel EPROM. In this case, it should be configured as a constant high, and not used as a configurable I/O pin. $\overline{\text{CEN}}$ is only available on the CLi6005 device.

A0 to A16 or I/O
During address count-up/down configuration, these pins are outputs and act as the address pins for a parallel EPROM. A0–A16 eliminate the need for an external address counter if the user wishes to use an inexpensive parallel EPROM to program a device. Addresses change after the rising edge of the CCLK signal.

CLKOUT or I/O
When cascading devices, CLKOUT is an output used with DATAOUT to configure other devices. CLKOUT should be connected to the CCLK input of the downstream device. The CLKOUT function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, CLKOUT should be dedicated to configuration and not used as a configurable I/O.

DATAOUT or I/O
When cascading devices, DATAOUT is an output used with CLKOUT to configure other devices. The DATAOUT signal is designed to have sufficient setup and hold time with respect to the rising edge of CLKOUT to satisfy the next device in the cascade. The DATAOUT function is optional and can be disabled during initial programming when cascading is not used. When cascading devices, DATAOUT should be dedicated to configuration and not used as a configurable I/O.

$\overline{\text{CHECK}}$ or I/O
During configuration, $\overline{\text{CHECK}}$ is an input that can be used to enable the data check function at the beginning of a configuration cycle. No data is written to the device while $\overline{\text{CHECK}}$ is low. Instead, the configuration file being applied to D0–D7 is compared with the current contents of the internal configuration RAM. If a mismatch is detected between the data being loaded and the data already in the RAM, the $\overline{\text{ERR}}$ pin goes low. The $\overline{\text{CHECK}}$ function is optional and can be disabled during initial programming.

$\overline{\text{ERR}}$ or I/O
During configuration, $\overline{\text{ERR}}$ is an output. When the $\overline{\text{CHECK}}$ function is activated and a mismatch is detected between the current configuration data stream and the data already loaded in the configuration RAM, $\overline{\text{ERR}}$ goes low. The $\overline{\text{ERR}}$ output is a registered signal. Once a mismatch is found, the signal is set and is only reset after the configuration cycle is complete. $\overline{\text{ERR}}$ is also asserted for configuration file errors. The $\overline{\text{ERR}}$ function is optional and can be disabled during initial programming.

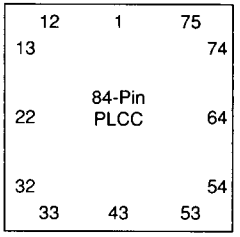
PINOUTS—CLi6005 DEVICE

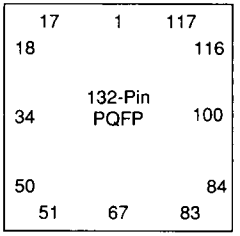
84-Pin PLCC

- 64 I/O
- 4 VCC
- 4 GND
- 2 VDD
- 2 VSS
- 8 Fixed-Function
- 30 Dual-Function

132-Pin PQFP

- 108 I/O
- 4 VCC
- 8 GND
- 2 VDD
- 2 VSS
- 8 Fixed-Function
- 30 Dual-Function





CLi6005 Pin Name	84 PLCC	132 PQFP
CLOCK	1	1
A15 or I/O	2	2
A14 or I/O	3	3
VCC	4	4
A13 or I/O	5	5
I/O	*	6
A12 or I/O	6	7
I/O	*	8
A11 or I/O	7	9
I/O	*	10
GND	*	11
A10 or I/O	8	12
I/O	*	13
A9 or I/O	9	14
I/O	*	15
A8 or I/O	10	16
M0	11	17
A7 or I/O	12	18
I/O	*	19
A6 or I/O	13	20
I/O	*	21
A5 or I/O	14	22
I/O	*	23
A4 or I/O	15	24
I/O	*	25
A3 or I/O	16	26
I/O	*	27
A2 or I/O	17	28
I/O	*	29
GND	18	30
VSS	19	31
A1 or I/O	20	32
A0 or I/O	21	33
D7 or I/O	22	34
D6 or I/O	23	35
D5 or I/O	24	36
VDD	25	37
VCC	26	38
I/O	*	39
D4 or I/O	27	40
I/O	*	41
D3 or I/O	28	42
I/O	*	43
GND	*	44

CLi6005 Pin Name	84 PLCC	132 PQFP
D2 or I/O	29	45
I/O	*	46
D1 or I/O	30	47
I/O	*	48
D0 or I/O	31	49
CCLK	32	50
$\overline{CON}$	33	51
$\overline{CEN}$ or I/O	34	52
I/O	*	53
CLKOUT or I/O	35	54
I/O	*	55
DATAOUT or I/O	36	56
I/O	*	57
$\overline{CHECK}$ or I/O	37	58
I/O	*	59
$\overline{ERR}$ or I/O	38	60
I/O	*	61
I/O	39	62
I/O	*	63
GND	40	64
I/O	41	65
I/O	42	66
$\overline{CS}$	43	67
I/O	44	68
I/O	45	69
VCC	46	70
I/O	47	71
I/O	*	72
I/O	48	73
I/O	*	74
I/O	49	75
I/O	*	76
GND	*	77
I/O	50	78
I/O	*	79
I/O	51	80
I/O	*	81
I/O	52	82
$\overline{RESET}$	53	83
I/O	54	84
I/O	*	85
I/O	55	86
I/O	*	87
I/O	56	88

CLi6005 Pin Name	84 PLCC	132 PQFP
I/O	*	89
I/O	57	90
I/O	*	91
I/O	58	92
I/O	*	93
I/O	59	94
I/O	*	95
GND	60	96
VSS	61	97
I/O	62	98
I/O	63	99
I/O	64	100
I/O	65	101
I/O	66	102
VDD	67	103
VCC	68	104
I/O	*	105
I/O	69	106
I/O	*	107
I/O	70	108
I/O	*	109
GND	*	110
I/O	71	111
I/O	*	112
I/O	72	113
I/O	*	114
I/O	73	115
M2	74	116
M1	75	117
I/O	76	118
I/O	*	119
I/O	77	120
I/O	*	121
I/O	78	122
I/O	*	123
I/O	79	124
I/O	*	125
I/O	80	126
I/O	*	127
I/O	81	128
I/O	*	129
GND	82	130
I/O	83	131
A16 or I/O	84	132

* Indicates unconnected package pin

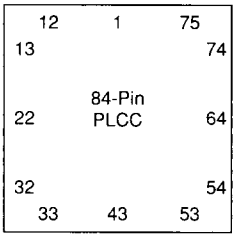
PINOUTS—CLi6002 DEVICE

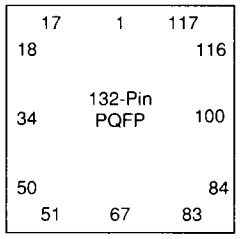
84-Pin PLCC

- 64 I/O
- 4 VCC
- 4 GND
- 2 VDD
- 2 VSS
- 8 Fixed-Function
- 29 Dual-Function

132-Pin PQFP

- 96 I/O
- 4 VCC
- 8 GND
- 2 VDD
- 2 VSS
- 8 Fixed-Function
- 29 Dual-Function





CLi6002 Pin Name	84 PLCC	132 PQFP
CLOCK	1	1
A15 or I/O	2	2
A14 or I/O	3	3
VCC	4	4
A13 or I/O	5	5
I/O	*	6
A12 or I/O	6	7
I/O	*	8
A11 or I/O	7	9
*	*	10
GND	*	11
A10 or I/O	8	12
I/O	*	13
A9 or I/O	9	14
I/O	*	15
A8 or I/O	10	16
M0	11	17
A7 or I/O	12	18
*	*	19
A6 or I/O	13	20
I/O	*	21
A5 or I/O	14	22
I/O	*	23
A4 or I/O	15	24
I/O	*	25
A3 or I/O	16	26
I/O	*	27
A2 or I/O	17	28
*	*	29
GND	18	30
VSS	19	31
A1 or I/O	20	32
A0 or I/O	21	33
D7 or I/O	22	34
D6 or I/O	23	35
D5 or I/O	24	36
VDD	25	37
VCC	26	38
I/O	*	39
D4 or I/O	27	40
I/O	*	41
D3 or I/O	28	42
*	*	43
GND	*	44

CLi6002 Pin Name	84 PLCC	132 PQFP
D2 or I/O	29	45
I/O	*	46
D1 or I/O	30	47
I/O	*	48
D0 or I/O	31	49
CCLK	32	50
$\overline{CON}$	33	51
I/O	34	52
*	*	53
CLKOUT or I/O	35	54
I/O	*	55
DATAOUT or I/O	36	56
I/O	*	57
$\overline{CHECK}$ or I/O	37	58
I/O	*	59
$\overline{ERR}$ or I/O	38	60
I/O	*	61
I/O	39	62
*	*	63
GND	40	64
I/O	41	65
I/O	42	66
$\overline{CS}$	43	67
I/O	44	68
I/O	45	69
VCC	46	70
I/O	47	71
I/O	*	72
I/O	48	73
I/O	*	74
I/O	49	75
*	*	76
GND	*	77
I/O	50	78
I/O	*	79
I/O	51	80
I/O	*	81
I/O	52	82
$\overline{RESET}$	53	83
I/O	54	84
*	*	85
I/O	55	86
I/O	*	87
I/O	56	88

CLi6002 Pin Name	84 PLCC	132 PQFP
I/O	*	89
I/O	57	90
I/O	*	91
I/O	58	92
I/O	*	93
I/O	59	94
*	*	95
GND	60	96
VSS	61	97
I/O	62	98
I/O	63	99
I/O	64	100
I/O	65	101
I/O	66	102
VDD	67	103
VCC	68	104
I/O	*	105
I/O	69	106
I/O	*	107
I/O	70	108
*	*	109
GND	*	110
I/O	71	111
I/O	*	112
I/O	72	113
I/O	*	114
I/O	73	115
M2	74	116
M1	75	117
I/O	76	118
*	*	119
I/O	77	120
I/O	*	121
I/O	78	122
I/O	*	123
I/O	79	124
I/O	*	125
I/O	80	126
I/O	*	127
I/O	81	128
*	*	129
GND	82	130
I/O	83	131
A16 or I/O	84	132

* Indicates unconnected package pin

BASIC AC TIMING CHARACTERISTICS

Delays are based on fixed load. Loads for each type of device are described in the notes. Delays are in nanoseconds. Worst case: Vcc = 4.75V to 5.25V. Temperature = 0 °C to 70 °C.

CELL FUNCTION	PARAMETER	FROM	TO	LOAD	- 2	- 4	UNITS
Wire [4]	t_{PD} (max) [4]	A, B, L	A, B	1	1.2	1.8	ns
NAND	t_{PD} (max)	A, B, L	B	1	2.2	3.2	ns
XOR	t_{PD} (max)	A, B, L	A	1	2.4	4.0	ns
AND	t_{PD} (max)	A, B, L	B	1	2.3	3.2	ns
MUX	t_{PD} (max)	A, B L	A A	1 1	2.4 2.9	4.0 4.9	ns ns
D-FlipFlop [5]	t_{setup} (min)	A, B, L	CLK		2.0	3.0	ns
D-FlipFlop [5]	t_{hold} (min)	CLK	A, B, L		0.0	0.0	ns
D-FlipFlop	t_{PD} (max)	CLK RES	A A	1 1	2.0 2.0	3.0 3.0	ns ns
Bus Driver	t_{PD} (max)	A	L	2	2.7	4.0	ns
Repeater	t_{PD} (max)	L, E L, E	E L	3 2	1.8 2.2	2.3 3.0	ns ns
Column Clock	t_{PD} (max)	GCLK, A, ES	CLK	3	2.0	3.0	ns
Column Reset	t_{PD} (max)	GRES, A, EN	RES	3	2.0	3.0	ns
Clock Buffer [5]	t_{PD} (max)	CLOCK PIN	GCLK	4	2.0	2.9	ns
Reset Buffer [5]	t_{PD} (max)	RESET PIN	GRES	5	1.9	2.8	ns
TTL Input [1]	t_{PD} (max)	I/O	A	3	1.0	1.5	ns
CMOS Input [2]	t_{PD} (max)	I/O	A	3	1.5	2.3	ns
Fast Output [3] Slow Output [3]	t_{PD} (max)	A A	I/O PIN I/O PIN	6 6	3.7 9.2	6.0 12.0	ns ns
Output Disable [5]	t_{PXZ} (max)	L	I/O PIN	6	3.2	5.5	ns
Fast Enable [3, 5] Slow Enable [3, 5]	t_{PZX} (max)	L L	I/O PIN I/O PIN	6 6	4.2 9.7	6.5 12.5	ns ns

DEVICE	CELL TYPES	OUTPUTS	-4 Icc	-2 Icc	NOTE
Cell	Wire, XWire, Half-Adder, Flip-Flop	A, B	7 µA/MHz	4.5 µA/MHz	—
Bus	Wire, XWire, Half-Adder, Flip-Flop, Repeater	L	4 µA/MHz	2.5 µA/MHz	—
Column Clock	Column Clock Driver	CLK	60 µA/MHz	40 µA/MHz	—

Load Definition:
1. Load of one A or B input
2. Load of one L input
3. Constant Load
4. Load of 28 Clock Columns
5. Load of 28 Reset Columns
6. Tester Load of 50 pF

Notes:
1. TTL buffer delays are measured from a Vth of 1.5V at the pad to the intrenal Vth at A. The input buffer load is constant.
2. CMOS buffer delays are measured from a Vth of 1/2 Vcc at the pad to the internal Vth at A. The input buffer load is constant.
3. Buffer delay is to a pad Vth of 1.5V with one output switching.
4. Max specifications are the average of max tpdlh and tpdhl.
5. Parameter based on characterization and simulation; not tested in production.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Voltage (V_{IN})	-0.5V to VCC + 0.5V
DC Output Voltage (V_{ON})	-0.5V to VCC + 0.5V
Storage Temperature Range (T_{STG})	-65°C to +150°C
Power Dissipation (PD)	1500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C
ESD (R_{ZAP}=1.5K, C_{ZAP}=100pF)	2000V

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device reliability. Device should not be operated outside the Recommended Operating Conditions. For military-specified devices, contact your local Concurrent Logic representative for availability and specifications.

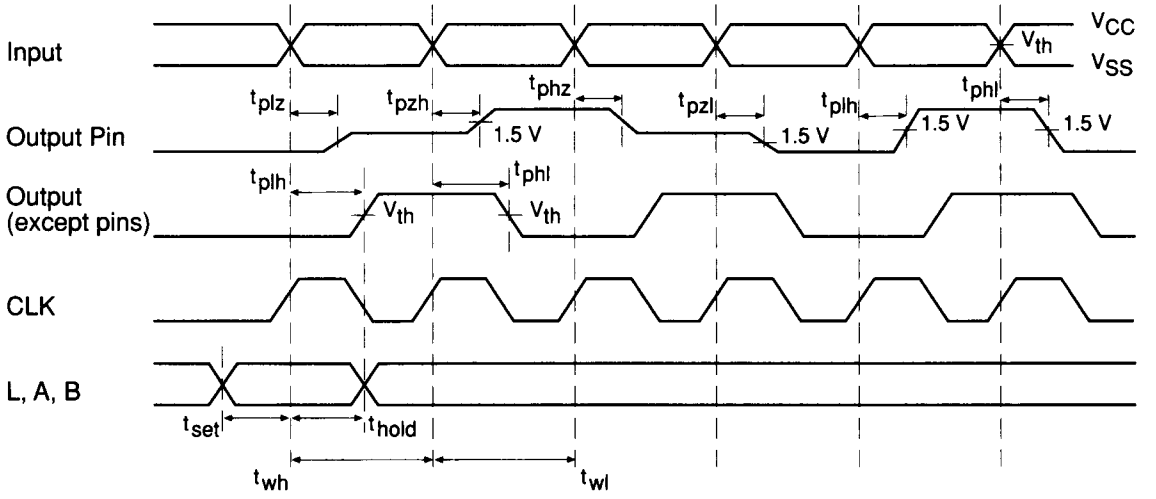
RECOMMENDED OPERATING

Supply Voltage (V_{CC})	
Commercial	4.75V to 5.25V
Industrial	4.50V to 5.50V
Military	4.50V to 5.50V
Temperature Range	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
High-Level Input Voltage (TTL) (V_{IHT})	2.0V to V_{CC}
Low-Level Input Voltage (TTL) (V_{ILT})	0V to 0.8V
High-Level Input Volt. (CMOS) (V_{IHC})	70% to 100% V_{CC}
Low-Level Input Volt. (CMOS) (V_{ILC})	0 to 30% V_{CC}
Input Signal Transition Time (T_{IN})	50ns (max)

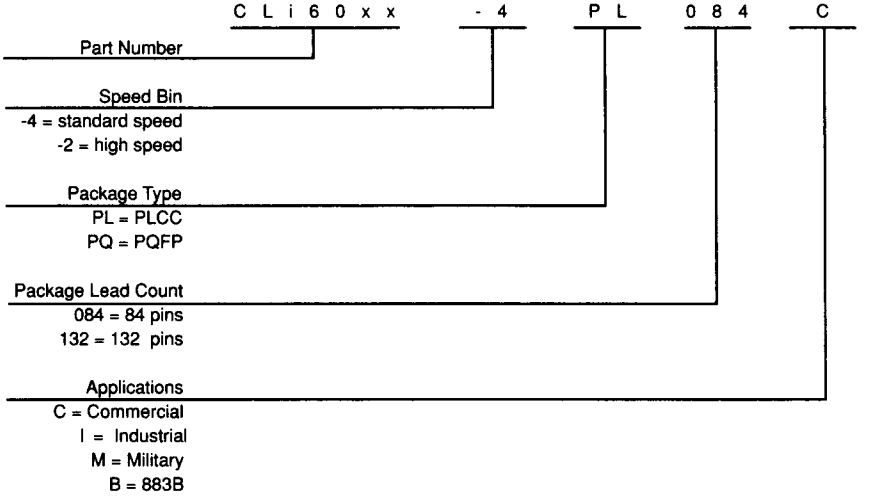
DC SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{IH}	High-Level Input Voltage	Commercial			
		CMOS	70% V_{CC}	V_{CC}	V
		TTL	2.0	V_{CC}	V
V_{IL}	Low-Level Input Voltage	Commercial			
		CMOS	0	20% V_{CC}	V
		TTL	0	0.8	V
V_{OH}	High-Level Output Voltage	Commercial			
		I_{OH} = -4mA, V_{CC} min	3.9		V
		I_{OH} = -12mA, V_{CC} min	3.0		V
V_{OL}	Low-Level Output Voltage	Commercial			
		I_{OL} = -4mA, V_{CC} min		0.4	V
		I_{OL} = -12mA, V_{CC} min		0.5	V
I_{OZH}	High-Level Tristate Output Leakage Current	V_O = V_{CC} (max)		10	µA
I_{OZL}	Low-Level Tristate Output Leakage Current	Without Pull-Up, V_O = V_{SS}	-10		µA
		With Pull-Up, V_O = V_{SS}	-500		µA
I_{IH}	High-Level Input Current	V_{IN} = V_{CC} (max)		10	µA
I_{IL}	Low-Level Input Current	Without Pull-Up, V_{IN} = V_{SS}	-10		µA
		With Pull-Up, V_{IN} = V_{SS}	-500		µA
I_{CC}	Power Consumption	Without Internal Oscillator		500	µA
C_{IN}	Input Capacitance	All Pins		10	pF

DEVICE TIMING: DURING OPERATION

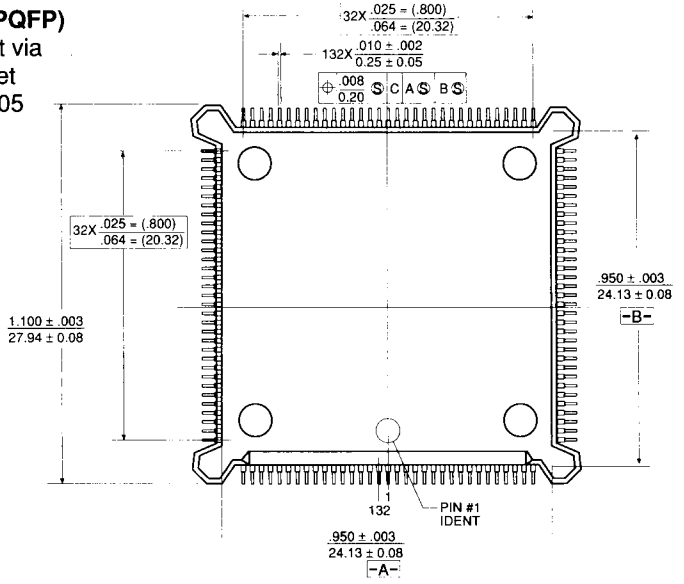


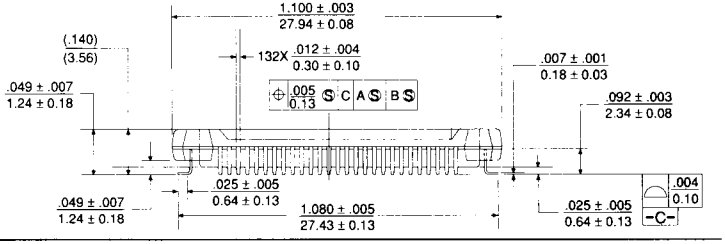
ORDERING INFORMATION



PACKAGE DIAGRAMS (CLi6002 and CLi6005)

132-Lead Plastic Quad Flatpack (PQFP)
Convertible to Pin Grid Array Format via AMP 132-Position Micro-Pitch Socket Housing Sub-Assembly No. 82194905 and Cover No. 821942-1





84-Lead Plastic Chip Carrier (PLCC)
Convertible to Pin Grid Array Format via AMP 84-Position Plastic Chip Carrier Socket No. 821573-1