

# BLF7G20L-160P; BLF7G20LS-160P

Power LDMOS transistor

Rev. 01 — 22 June 2010

Objective data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.

Mode of operation	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR <sub>400k</sub> (dBc)	ACPR <sub>600k</sub> (dBc)	EVM <sub>rms</sub> (%)
CW	1805 to 1880	850	28	135	17.5	57	-	-	-
GSM EDGE	1805 to 1880	850	28	65	18.5	43	-61	-74	2.5

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low  $R_{th}$  providing excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low-memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF7G20L-160P (SOT1121A)</b>			
1	drain1		<p style="text-align: right;">sym117</p>
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF7G20LS-160P (SOT1121B)</b>			
1	drain1		<p style="text-align: right;">sym117</p>
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF7G20L-160P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF7G20LS-160P	-	earless flanged LDMOST ceramic package; 4 leads	SOT1121B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$I_D$	drain current		-	<tbid>	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 100\text{ W}$	0.41	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 90\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	14	-	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	200	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 2.5\text{ A}$	-	<tbid>	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 3.15\text{ A}$	-	0.15	-	$\Omega$

## 7. Test information

**Table 7. Application information**

$f = 1805\text{ MHz}$  and  $1880\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 850\text{ mA}; T_{case} = 25\text{ °C}$ ; 2 sections combined unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Mode of operation: GSM EDGE; <math>P_{L(AV)} = 65\text{ W}</math></b>						
$G_p$	power gain		17.3	18.5	-	dB
$RL_{in}$	input return loss		-	-15	-8	dB
$\eta_D$	drain efficiency		40	43	-	%
$ACPR_{400k}$	adjacent channel power ratio (400 kHz)		-	-61	-58	dBc
$ACPR_{600k}$	adjacent channel power ratio (600 kHz)		-	-74	-70.5	dBc
$EVM_{rms}$	RMS EDGE signal distortion error		-	2.5	3.8	%
$EVM_M$	peak EDGE signal distortion error		-	8	12.5	%
<b>Mode of operation: CW; <math>P_{L(AV)} = 135\text{ W}</math></b>						
$G_p$	power gain		16.8	17.5	-	dB
$\eta_D$	drain efficiency		52	57	-	%

### 7.1 Ruggedness in class-AB operation

The BLF7G20L-160P and BLF7G20LS-160P are capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 850\text{ mA}; P_L = 160\text{ W (CW)}; f = 1805\text{ MHz}$ .

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A

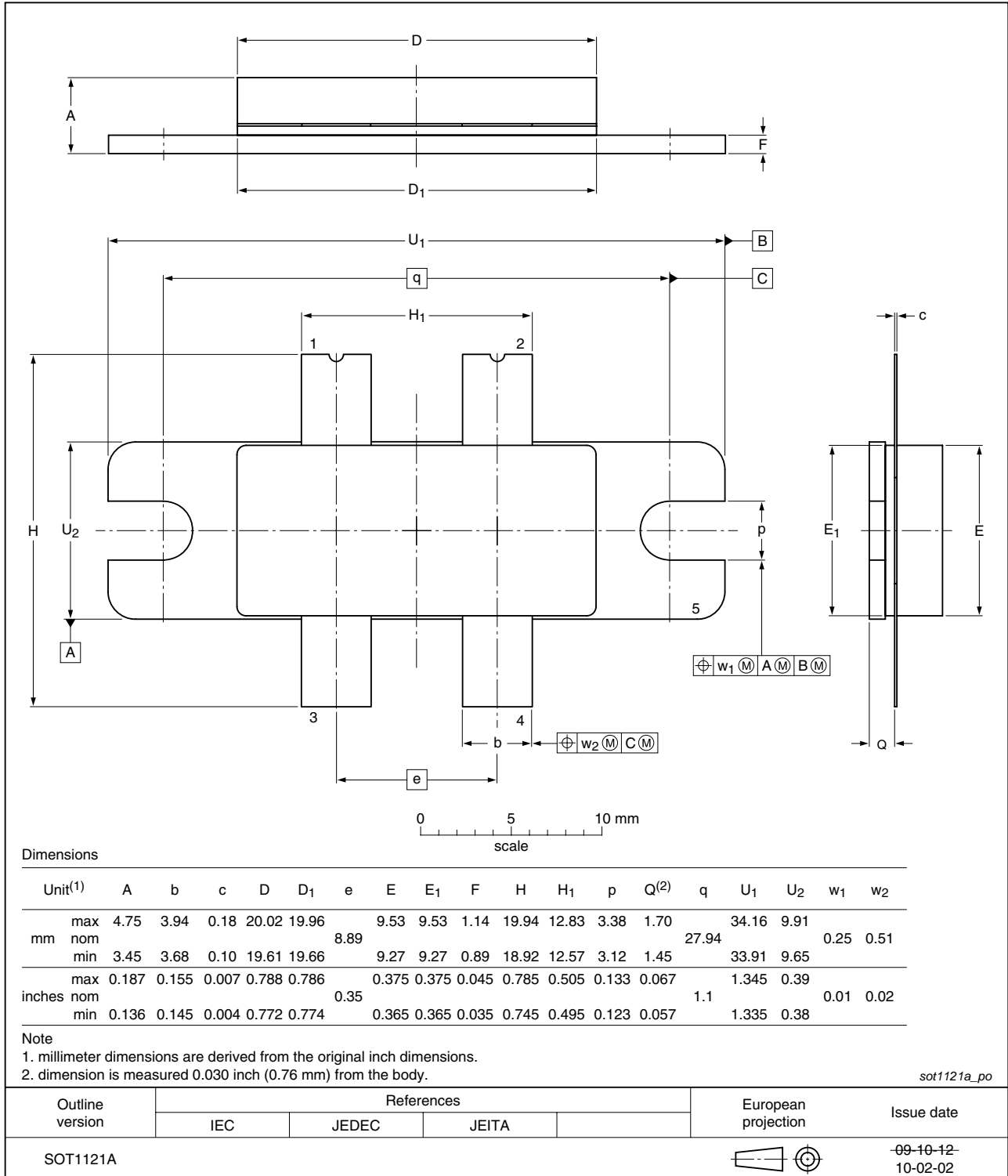


Fig 1. Package outline SOT1121A

Earless flanged LDMOST ceramic package; 4 leads

SOT1121B

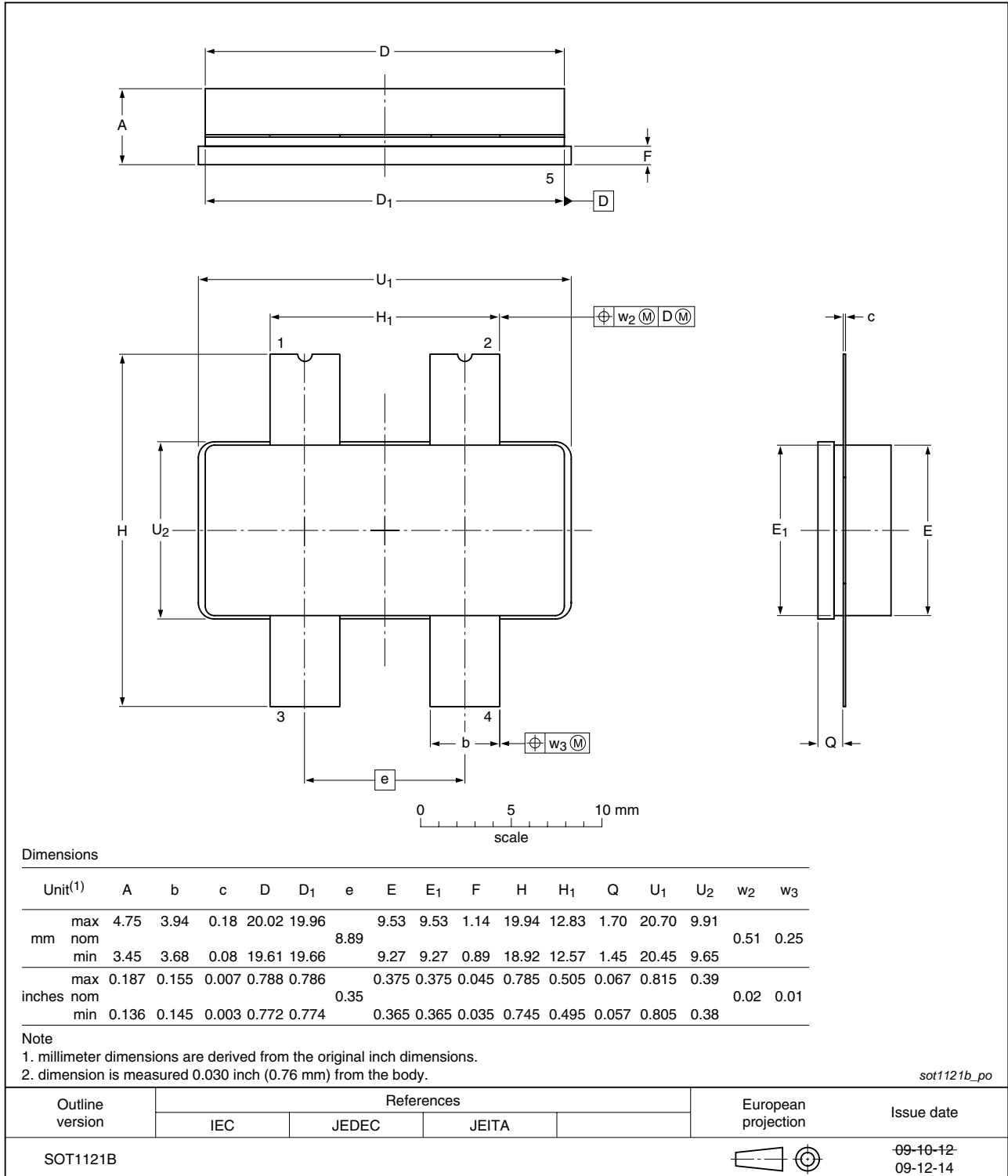


Fig 2. Package outline SOT1121B

## 9. Abbreviations

**Table 8. Abbreviations**

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
ESD	ElectroStatic Discharge
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 10. Revision history

**Table 9. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF7G20L-160P_7G20LS-160P v.1	20100622	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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