Product Brief
April 1993

AT&T Microelectronics

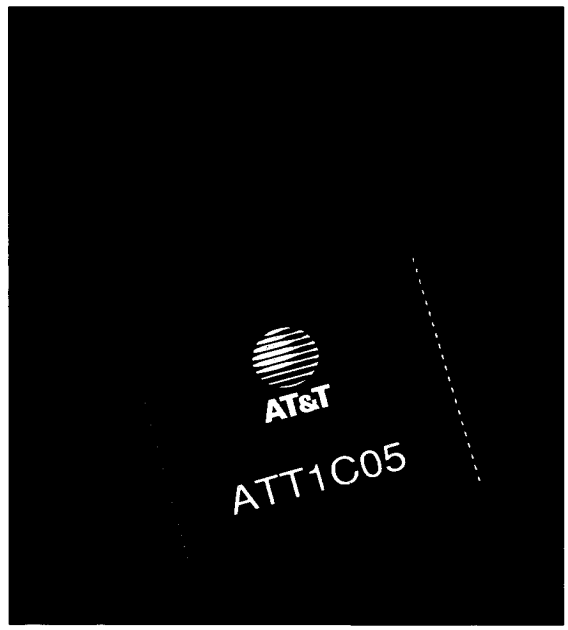
AT&T Optimized Reconfigurable Cell Array (ORCA) Series Field-Programmable Gate Arrays (FPGAs)

Features

- 0.6 µm CMOS process technology
- High-density 3,500 to 22,000 usable gates
- Up to 288 usable I/O
- High-performance (system) operating frequency (33 MHz—80 MHz)
- Low power consumption
- In-circuit reprogrammable
- Built-in boundary scan (IEEE 1149.1)
- Multiple device and package types

Device	Usable Gates	Registers	Max User RAM Bits	User I/Os	Array Size
ATT1C03	3,500	400	6,400	160	10 x 10
ATT1C05	5,000	576	9,216	192	12 x 12
ATT1C07	7,000	784	12,544	224	14 x 14
ATT1C12	12,000	1296	20,736	216	18 x 18
ATT1C15	15,000	1600	25,600	240	20 x 20
ATT1C22	22,000	2304	36,864	288	24 x 24

- Configurable large-/medium-grain structure optimizes logic utilization
- TTL or CMOS input thresholds
- User-defined I/Os
- Nibble-wide input structure for ease of implementing 4-, 8-, 16-, or 32-bit bus interface
- Identical and symmetrical programmable logic cells (PLCs)
- Four programmable latches/FFs per PLC
- Fast on-chip user-programmable SRAM memory
- Multiple user-defined low-skew clocks
- Global or local set and reset
- Selectable output sink/source current capability per I/O (12 mA/6 mA sink, 6 mA/3 mA source)
- Expandable fast-carry overflow for arithmetic functions and counters



Introduction

The AT&T Optimized Reconfigurable Cell Array (ORCA) series is the second generation of SRAM-based field-programmable gate arrays (FPGAs) from AT&T Microelectronics. This new series provides a family of high-performance, high-density, low-power, user-programmable integrated circuits.

The ORCA architecture and software have been developed in tandem, yielding a complete development system/integrated circuit package that is easy to use, yet also very powerful. The hardware architecture is composed of two types of programmable elements: programmable I/O cells (PICs) and programmable logic cells (PLCs) arranged in a homogenous array structure. These programmable cells are interconnected with abundant symmetrical routing.

This architecture, coupled with AT&T's performance-driven development system, provides an easy to use and powerful solution for implementing advanced system designs.

Architectural Overview

Programmable Logic Cells (PLCs)

A PLC contains the circuitry required to create user application logic functions and the internal routing resources to connect these functions together. It is composed of a programmable function unit (PFU) and programmable routing resources.

Programmable Function Unit (PFU)

The main components of a PFU are four latches/FFs and a 64-bit look-up table (LUT) as shown in Figure 1. The LUT can be configured to operate in one of three modes:

- Combinational mode
- Ripple mode
- On-chip memory mode

The large-/medium-grain PLCs offer the user significant advances over alternative architectures. Complex logic functions can be implemented very efficiently in single PFUs. This, in turn, simplifies the place-and-route functions for large system designs.

Lower-density logic functions are also efficiently implemented because each PFU can be configured to implement multiple smaller functions. The PFU can also be configured as on-chip RAM.

Inter-PLC Routing Resources

The unique routing between PLCs presents a high-speed, high-density, straight-forward interconnect structure. Bidirectional, symmetrical, horizontal, and vertical routing have been designed to take the art out of the place-and-route function. In conjunction with ODS (described below), the numerous bidirectional lines, direct lines, and clock lines are automatically placed and routed. ODS offers complete autorouting using minimal silicon area, producing a more cost-effective as well as a more dense and effective system solution, without manual intervention.

Programmable I/O Cells (PICs)

The programmable I/O cells (PIC), with an I/O count up to 288, can literally fit any application. Each I/O can accept or drive either TTL or CMOS levels and be configured for input, output, or I/O. All outputs can be driven to a 3-state level. Output slews, as well as source/sink current, are programmable. Pull-up or pull-down resistors are available on inputs.

ORCA Development System (ODS)

The ORCA Development System is a performance-driven software tool that is very easy to use. ODS, coupled with third-party schematic entry and simulation tools, allows designers to easily and quickly realize their designs in ORCA chips. It is available for both *Windows** 3.1 based PCs and *Sun Workstations*†. ODS and the advanced ORCA architecture enable significant gains in system designer creativity and productivity. Please refer to the ODS product brief for more information.

* *Windows* is a registered trademark of Microsoft Corporation.
† *Sun Workstation* is a registered trademark of Sun Microsystems, Inc.

Programmable Function Unit

Each PFU has 19 inputs and six outputs. Eleven of the inputs to the PFU are inputs to the LUT. These are labelled as A[4:0], B[4:0], and C0. The rest of the inputs to the PFU are the following:

- WD[3:0] are direct data inputs to the PFU latches/FFs. If the PFU is programmed to operate in on-chip memory mode, WD[3:0] are used as a 4-bit data input bus.
- CK, clock distribution to each PFU, can be programmed to select from either a vertical or a horizontal clock net. The clock to PFU latches/FFs can be configured as either positive edge triggered, negative edge triggered, positive level sensitive, or negative level sensitive.
- CE, clock enable, is an input control signal. If enabled, data will be clocked according to the user's choice of the above clock-triggering scheme. If CE is disabled, the output retains its previous state when clocked.
- Each individual latch/FF can either be set or reset by the S/R set or reset input line. Each PFU can be configured to cause either a synchronous or an asynchronous set or reset.

From the PFU block diagram, there are eight possible outputs from the PFU. Four are the result of the combinational logic functions, and four are directly from the four latches/FFs. Any combination of five of these eight signals can be routed to the output of the PFU as O[4:0]. The sixth output, COUT, is the fast carry-out signal. O4 can also be used as an optional carry-out.

The LUT can be programmed to operate in mixed on-chip memory and combinational modes. This is done by placing half of the PFU in memory mode and the other half in combinational mode or vice versa. Ripple mode cannot be enabled simultaneously with any other mode.

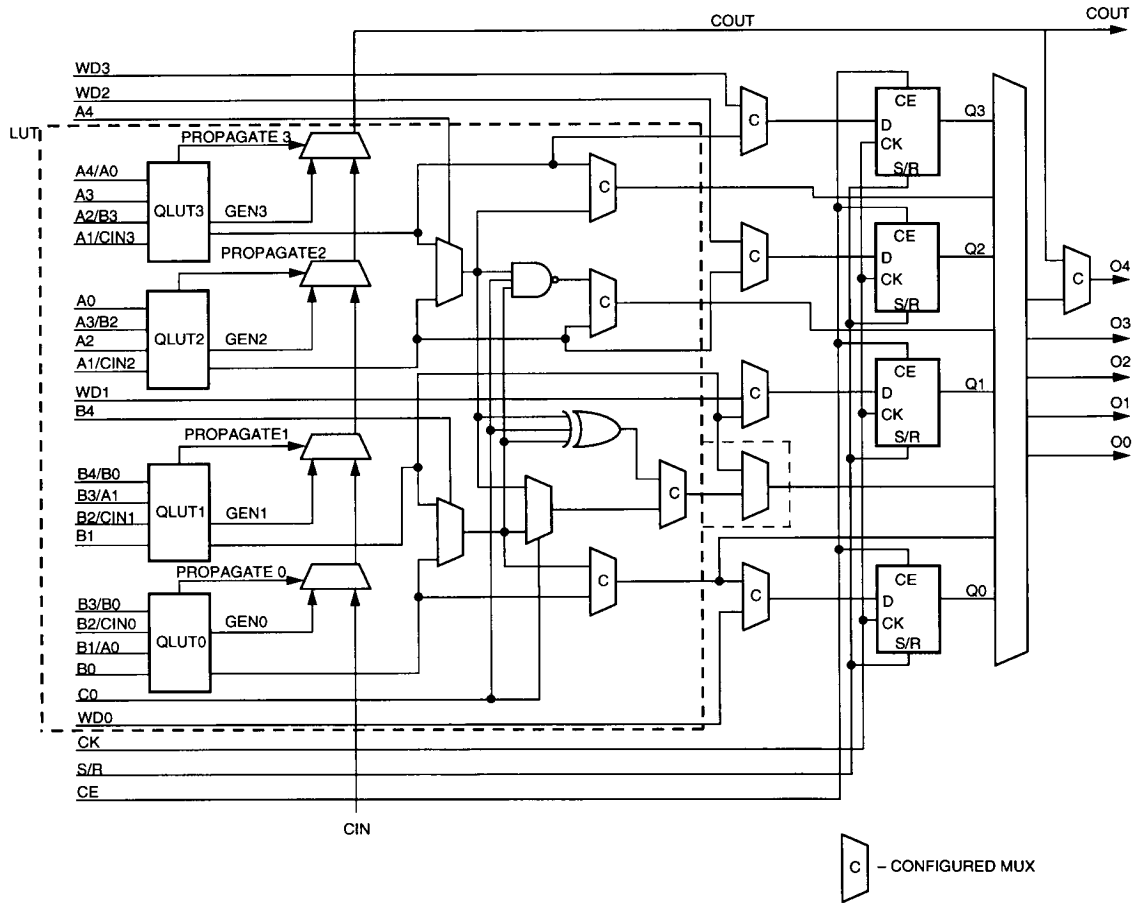


Figure 1. PFU Block Diagram

Programmable Function Unit (continued)

Combinational Mode

While in combinational mode, the LUT can be configured to do the following:

- Each quarter LUT can be configured to perform functions of four inputs (see Figure 2). The two quarter LUTs on each side of the LUT use shared inputs as shown.

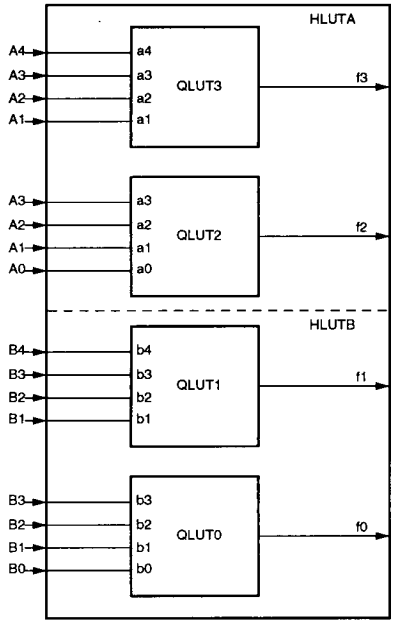


Figure 2. Four Dependent Four-Input Functions

- Each half LUT can be configured to perform functions of five inputs. A[4:0] and B[4:0] are inputs to each half. f3 and f0 are the outputs.
- In order to do any function of six inputs, tie A[4:0] to B[4:0]. The sixth input is C0.
- The entire LUT can also be used to perform some logic functions of up to 11 inputs.

Ripple Mode

The LUT can be programmed to perform ripple functions with high-speed carry logic. Since the ORCA FPGA series is a nibble-wide device, a very fast 4-bit adder can be implemented in one PLC, taking advantage of the internal fast-carry circuits. The ORCA series also has dedicated carry-out (COUT) lines to route the carry to/from the four abutting PLCs.

Using the dedicated fast-carry logic and routing, a very fast *n*-bit adder can be easily constructed (see Figure 3).

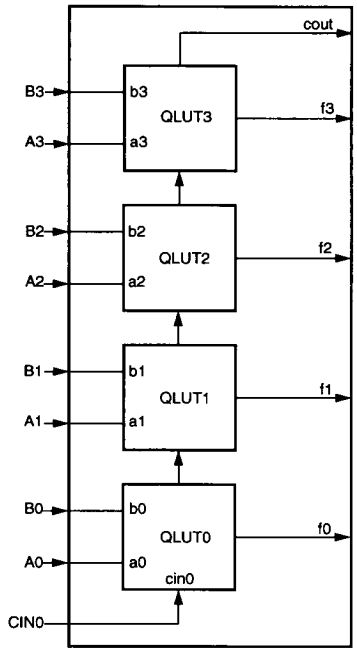


Figure 3. Ripple Mode

On-Chip Memory Mode

The PFU can be configured to access memory in the LUT as RAM. Each PFU can be configured as a dual 16 x 2 RAM. A[3:0] and B[3:0] can be used to address these memory locations. A4 and B4 are used as write-enable signals. WD[3:0] are used as the data inputs, and f[3:0] are used as the data outputs (see Figure 4).

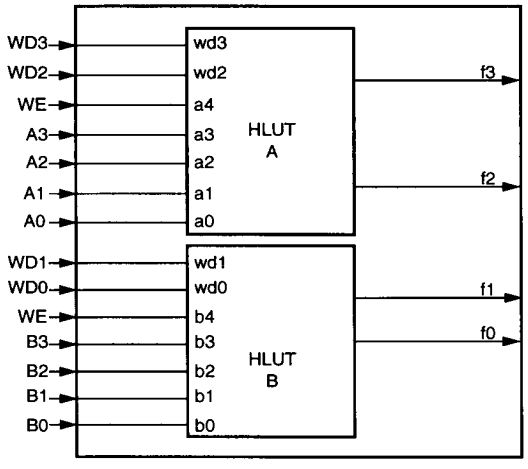


Figure 4. Dual 16 x 2 RAM/ROM

Routing Resources

ORCA routing resources are made from metal segments called resource routing nodes (R-nodes). These R-nodes are connected together at configurable interconnect points (CIPs) to form user-defined nets. They are categorized into two major types: internal and inter-PLC.

Internal Routing

The internal routing resources or R-nodes are used to route signals within the PLC. Internal routing resources consist of PFU input R-nodes, PFU output R-nodes, switching R-nodes, and bidirectional R-nodes.

Inter-PLC Routing

Inter-PLC routing resources or R-nodes are used to route signals from one PLC to another. These resources are known as x1 R-nodes, x4 R-nodes, xL R-nodes, and direct R-nodes (see Figure 5).

x1 R-Nodes

An x1 line is one PLC long. If signals need to travel more than one PLC away, an x1 R-node can be lengthened to *n* times its length by turning on *n* CIPs.

x4 R-Nodes

x4 R-nodes allow a signal to be routed four PLCs away in any direction without using any additional CIPs. A longer R-node can be programmed by connecting two x4 R-nodes together with a CIP.

xL R-Nodes

xL R-nodes span the entire length or width of the ORCA chip. They are used for clock routing or for routing signals that require low skew and high fan-out. In many other FPGAs, low-skew clocks can only be applied to dedicated clock input pads, which results in a limited number of clocks. ORCA clock distribution allow users flexibility in choosing their own clock input pins and number of clocks.

Direct R-Nodes

There are four sets of five direct R-nodes, one for each side of a PFU. Direct R-nodes allow high-speed connections to directly adjacent PFUs on all four sides without using inter-PLC routing resources.

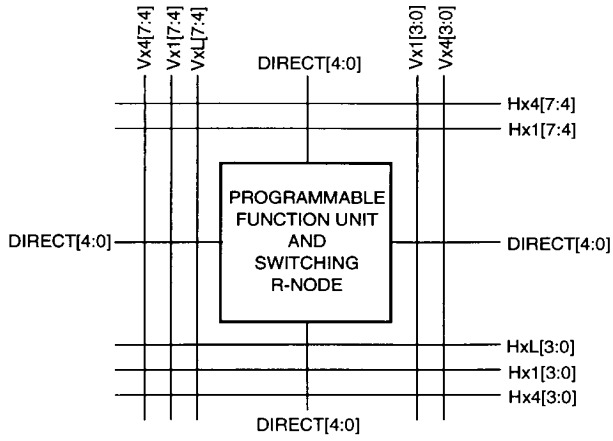


Figure 5. PLC Routing Resources

Programmable I/O Cells

PICs are located along the perimeter of the device. Each PIC has three or four pads depending on the size of the device. Each PIC contains the necessary routing resources to provide an interface between the I/O pad of the device and the core PLCs. Each PIC is composed of I/O drivers, I/O pads, and routing resources.

I/O Driver

The I/O driver is the interface between the I/O pad and the PIC routing resources (see Figure 6). The designer can program the I/O[3:0] drivers to do the following:

- Select each I/O pad as input, output, or I/O
- Select either a TTL or CMOS input threshold
- Delay the input to allow zero hold time on PLC latches/FFs
- Program output slew rates
- Select 12 mA/6 mA sink current and 6 mA/3 mA source current
- Program the 3-state enable control signal to either active-high or active-low
- Select either inverted or noninverted output
- Select a programmable pull-up or pull-down for the inputs

Programmable I/O Cells (continued)

PIC Routing Resources

The PIC routing is designed to route 4-bit wide buses efficiently. Any four consecutive I/O pads can have both their input and output signals gathered into one PIC. (see Figure 6).

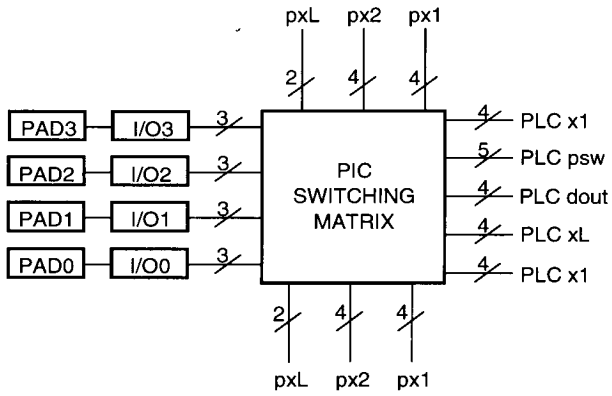


Figure 6. Simplified PIC Routing Resources

PIC-PIC Routing Resources

- pxL R-nodes — Span the entire length of the device.
- px2 R-nodes — Route nets that need to travel two or more PICs away.
- px1 R-nodes — One PIC long and can be extended by enabling CIPs.

Other PIC Routing Resources

psw[4:0] are switching R-nodes in the PIC that are physically connected to switching R-nodes in adjacent PLCs. The direct output R-nodes allow signals to go directly from a PLC register to the I/O driver without going through any additional routing resources, thus ensuring an extremely low register to I/O pad propagation delay.

ORCA Package Information

	84 Pin	132 Pin	208 Pin	240 Pin	304 Pin	225 Pin		280 Pin	364 Pin
	PLCC	JEDEC PQFP	EIAJ SQFP	EIAJ SQFP	EIAJ SQFP	Plastic PGA	Ceramic PGA	Ceramic PGA	Ceramic PGA
Device	**M84**	**F132**	**S208**	**S240**	**G304**	**H225**	**R225**	**R280**	**R364**
ATT1C03	X	X	X			X	X		
ATT1C05	X	X	X	X		X	X		
ATT1C07			X	X	X			X	
ATT1C12			X		X			X	
ATT1C15			X		X			X	
ATT1C22			X		X				X

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April 1993
PN93-030FPGA (Replaces PN93-017FPGA)