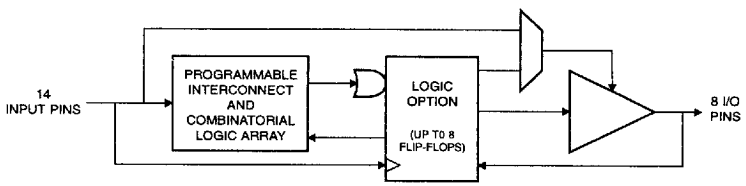
High Performance Flash PLD

Preliminary

Features

- **Industry Standard Architecture**
  - **Emulates Many 24-Pin PALs®**
  - **Low Cost Easy-to-Use Software Tools**
- **High Speed Electrically Erasable Programmable Logic Devices**
  - **7.5 ns Maximum Pin-to-Pin Delay**
- **Low Power ATF20V8BL - 10 mA Maximum Standby**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pull-Up Resistors**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High Reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000 V ESD Protection**
  - **200 mA Latchup Immunity**
- **Full Military, Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

Block Diagram



Description

The ATF20V8B is a high performance CMOS (Electrically Erasable) Programmable Logic Device (PLD) which utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 7.5 ns and power dissipation as low as 10 mA are offered. All speed ranges are specified over the full 5 V ± 10% range for military and industrial temperature ranges, and 5 V ± 5% for commercial ranges.

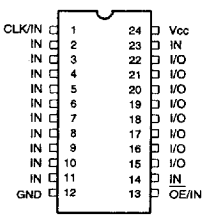
The ATF20V8BL provides the low power CMOS PLD solution, with low DC power (5.0 mA typical). The ATF20V8BL significantly reduces total system power and enhances system reliability

The ATF20V8Bs incorporate a superset of the generic architectures, which allows direct replacement of the 20R8 family and most 24-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

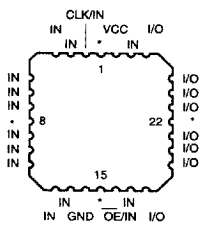
Pin Configurations

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
*	No Internal Connection
VCC	+5 V Supply

DIP/SOIC



LCC/PLCC



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0 V to +7.0 V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0 V to +14.0 V(1)
Programming Voltage with Respect to Ground	-2.0 V to +14.0 V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum voltage is -0.6 V dc, which may undershoot to -2.0 V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75 V dc, which may overshoot to 7.0 V for pulses of less than 20 ns.

D.C. and A.C. Operating Conditions

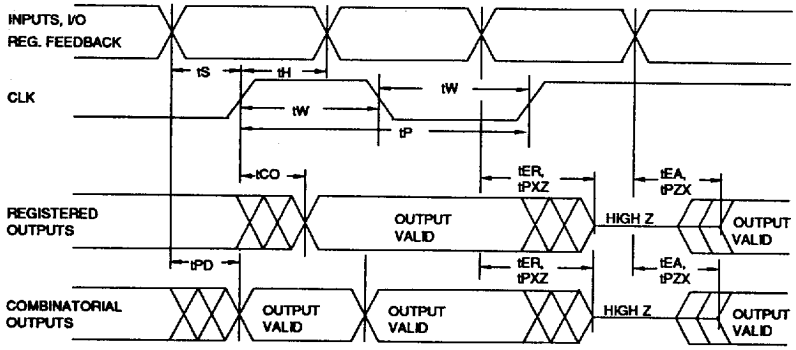
	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V_{CC} Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

D.C. Characteristics

Symbol	Parameter	Condition			Min	Typ.	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(MAX)				-35	-100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$					10	µA
I_{CC}	Power Supply Current, Standby	V_{CC} = MAX, V_{IN} = MAX, Outputs Open	B-7, -10	Com.		60	90	mA
				Ind., Mil.		60	100	mA
			B-15, -25	Com.		55	80	mA
				Ind., Mil.		55	90	mA
			BL-15	Com.		5	10	mA
				Ind., Mil.		5	15	mA
I_{CC2}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open	ATF20V8BL-15	Com.		1		mA/MHz(2)
I_{CC3}	Clocked Power Supply Current	V_{CC} = MAX, Outputs Open, f=25 MHz	B-7, -10	Com.		80	110	mA
				Ind., Mil.		80	125	mA
			B-15, -25	Com.		60	90	mA
				Ind., Mil.		60	105	mA
			BL-15	Com.		30	40	mA
				Ind., Mil.		30	50	mA
I_{OS} (1)	Output Short Circuit Current	V_{OUT} = 0.5 V					-130	mA
V_{IL}	Input Low Voltage				-0.5	-0.5	0.8	V
V_{IH}	Input High Voltage				2.0	2.0	V_{CC}+0.75	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}, V_{CC} = MIN	I_{OL} = 24 mA	Com., Ind.			0.5	V
			I_{OL} = 16 mA	Mil.			0.5	V
V_{OH}	Output High Voltage	V_{IN}=V_{IH} or V_{IL}, V_{CC}=MIN	I_{OH} = -4.0 mA		2.4	2.4		V

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. Low frequency only, contact factory for I_{CC} versus frequency characterization curves.

A.C. Waveforms (1)



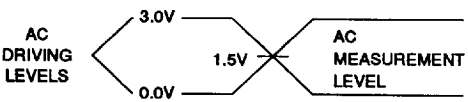
Note: 1. Timing measurement reference is 1.5 V. Input AC driving levels are 0.0 V and 3.0 V, unless otherwise specified.

A.C. Characteristics (1)

Symbol	Parameter	-7 Min	-7 Max	-10 Min	-10 Max	-15 Min	-15 Max	-25 Min	-25 Max	Units
t_{PD}	Input or Feedback to Non-Registered Output	3	7.5	3	10	3	15	3	25	ns
t_{CF}	Clock to Feedback		3		6		8		10	ns
t_{CO}	Clock to Output	2	5	2	7	2	10	2	12	ns
t_S	Input or Feedback Setup Time	5		7.5		12		15		ns
t_H	Hold Time	0		0		0		0		ns
t_P	Clock Period	8		12		16		24		ns
t_W	Clock Width	4		6		8		12		ns
F_{MAX}	External Feedback 1/(ts+tco)		100		68		45		37	MHz
	Internal Feedback 1/(ts + tCF)		125		74		50		40	MHz
	No Feedback 1/(tp)		125		83		62		41	MHz
t_{EA}	Input to Output Enable — Product Term	3	9	3	10	3	15	3	25	ns
t_{ER}	Input to Output Disable — Product Term	2	9	2	10	2	15	2	25	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	6	2	10	2	15	2	20	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	6	1.5	10	1.5	15	1.5	20	ns

Note: 1. See ordering information for valid part numbers and speed grades.

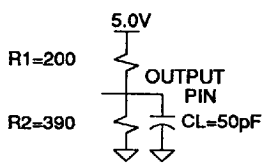
Input Test Waveforms and Measurement Levels:



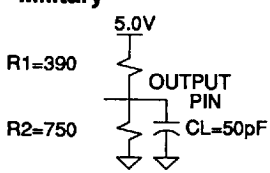
tR, tF < 5ns (10% to 90%)

Output Test Loads:

Commercial



Military



Pin Capacitance (f = 1 MHz, T = 25°C) [1]

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0 V
C_{OUT}	6	8	pF	V_{OUT} = 0 V

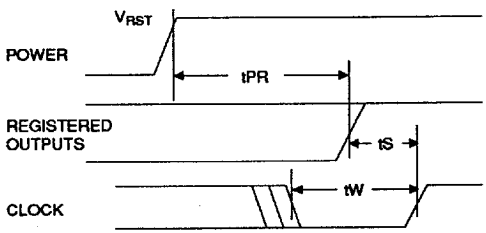
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Power Up Reset

The registers in the ATF20V8Bs are designed to reset during power up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1) The V_{CC} rise must be monotonic,
2) After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3) The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-Up Reset Time	600	1,000	ns
V_{RST}	Power-Up Reset Voltage	3.8	4.5	V

Preload of Registered Outputs

The ATF20V8B's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

Security Fuse Usage

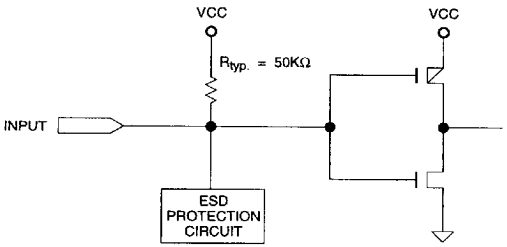
A single fuse is provided to prevent unauthorized copying of the ATF20V8B fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

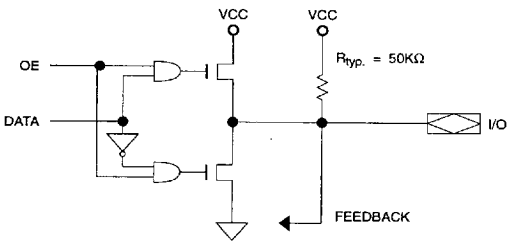
Input and I/O Pull-Ups

The ATF20V8B and ATF20V8BL have internal input and I/O pull-up resistors. Therefore, whenever inputs or I/Os are not being driven externally, they will float to Vcc. This ensures that all logic array inputs are at known states. These are relatively weak active pull-ups that can easily be overdriven by TTL-compatible drivers (see input and I/O diagrams below).

Input Diagram



I/O Diagram



Functional Logic Diagram Description

The Logic Option and Functional Diagrams describe the ATF20V8B architecture. Eight configurable macrocells can be configured as a registered output, combinatorial I/O, combinatorial output, or dedicated input.

The ATF20V8B can be configured in one of three different modes. Each mode makes the ATF20V8B look like a different device. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of register versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF20V8B universal architecture can be programmed to emulate many 24-pin PAL devices. These architectural subsets can be found in each of the configuration modes described in the following pages. The user can download the listed subset device JEDEC programming file to the PLD programmer, and the ATF20V8B can be configured to act like the chosen device. Check with your programmer manufacturer for this capability.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the content of the ATF20V8B. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision, or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P20V8R	P20V8C	P20V8AS	P20V8
CUPL	G20V8MS	G20V8MA	G20V8AS	G20V8
LOG/iC	GAL20V8_R (1)	GAL20V8_C7 (1)	GAL20V8_C8 (1)	GAL20V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL20V8A
PLDesigner	P20V8R	P20V8C	P20V8C	P20V8A
Tango-PLD	G20V8R	G20V8C	G20V8AS	G20V8

Note: 1. Only applicable for version 3.4 or lower.

ATF20V8B Registered Mode

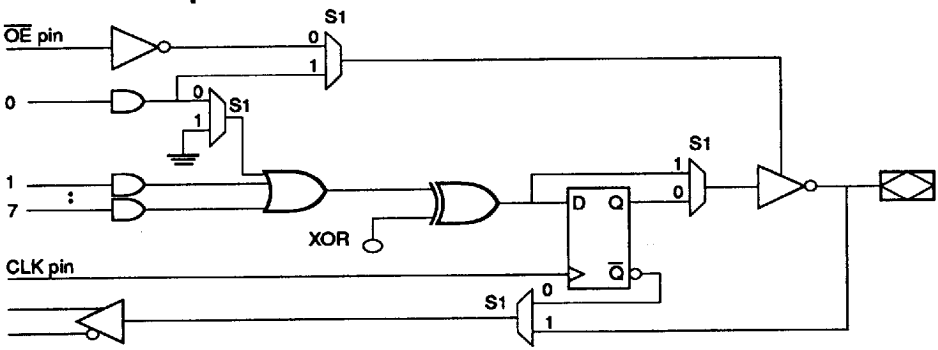
PAL Device Emulation / PAL Replacement

The registered mode is used if one or more registers are required. Each macrocell can be configured as either a registered or combinatorial output or I/O, or as an input. For a registered output or I/O, the output is enabled by the $\overline{OE}$ pin, and the register is clocked by the CLK pin. Eight product terms are allocated to the sum term. For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term. When the macrocell is configured as an input, the output enable is permanently disabled.

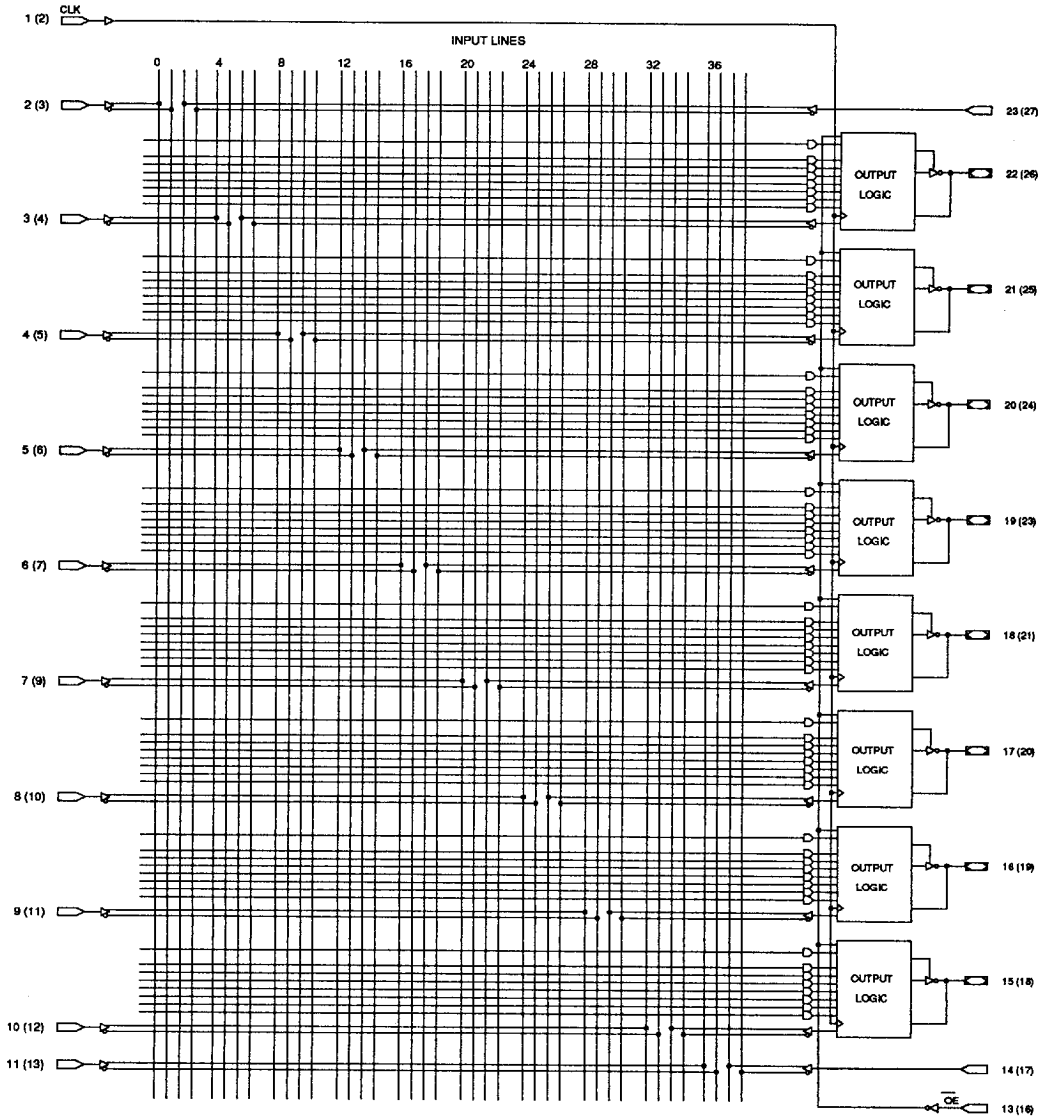
Any register usage will make the compiler select this mode. The following registered devices can be emulated using this mode:

20R8	20RP8
20R6	20RP6
20R4	20RP4

Registered Mode Option



Registered Mode Logic Diagram



ATF20V8B Complex Mode

PAL Device Emulation/PAL Replacement

In the Complex Mode, combinatorial output and I/O functions are possible. Pins 1 and 13 are regular inputs to the array. Pins 16 through 21 have pin feedback paths back to the AND-array, which makes full I/O capability possible. Pins 15 and 22 (outermost macrocells) are outputs only. They do not have input capability. In this mode, each macrocell has seven product terms going to the sum term and one product term enabling the output.

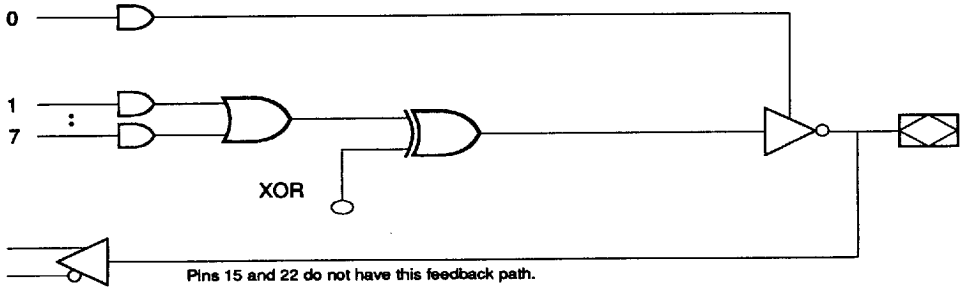
Combinatorial applications with an OE requirement will make the compiler select this mode. The following devices can be emulated using this mode:

20L8

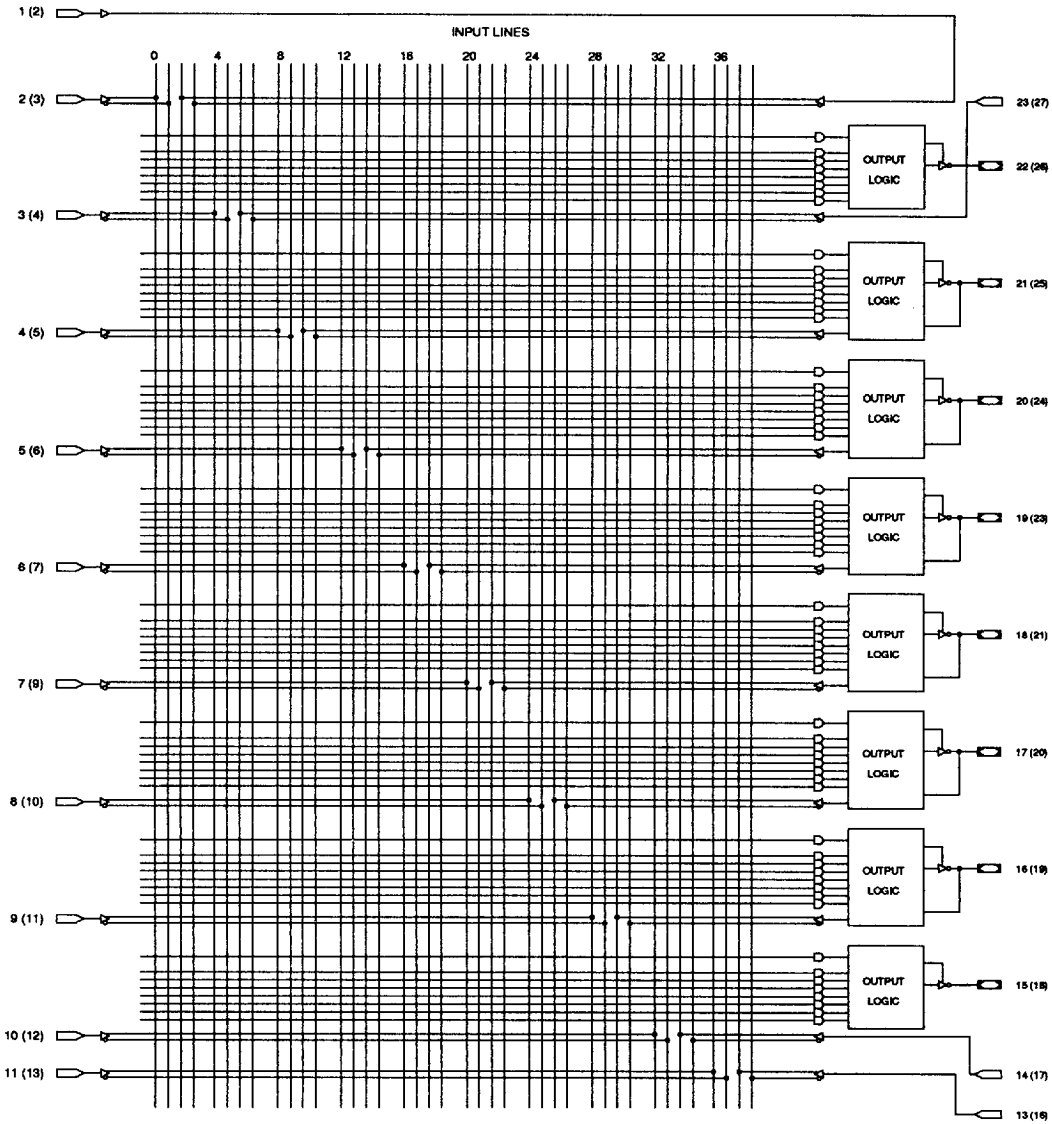
20H8

20P8

Complex Mode Option



Complex Mode Logic Diagram



ATF20V8B Simple Mode

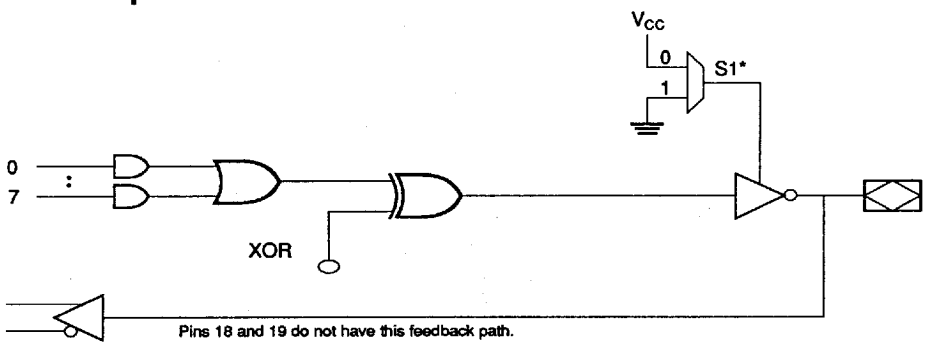
PAL Device Emulation / PAL Replacement

In the Simple Mode, 8 product terms are allocated to the sum term. Pins 18 and 19 (center macrocells) are permanently configured as combinatorial outputs. Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array. Pins 1 and 13 are regular inputs.

The compiler selects this mode when all outputs are combinatorial without OE control. The following simple PALs can be emulated using this mode:

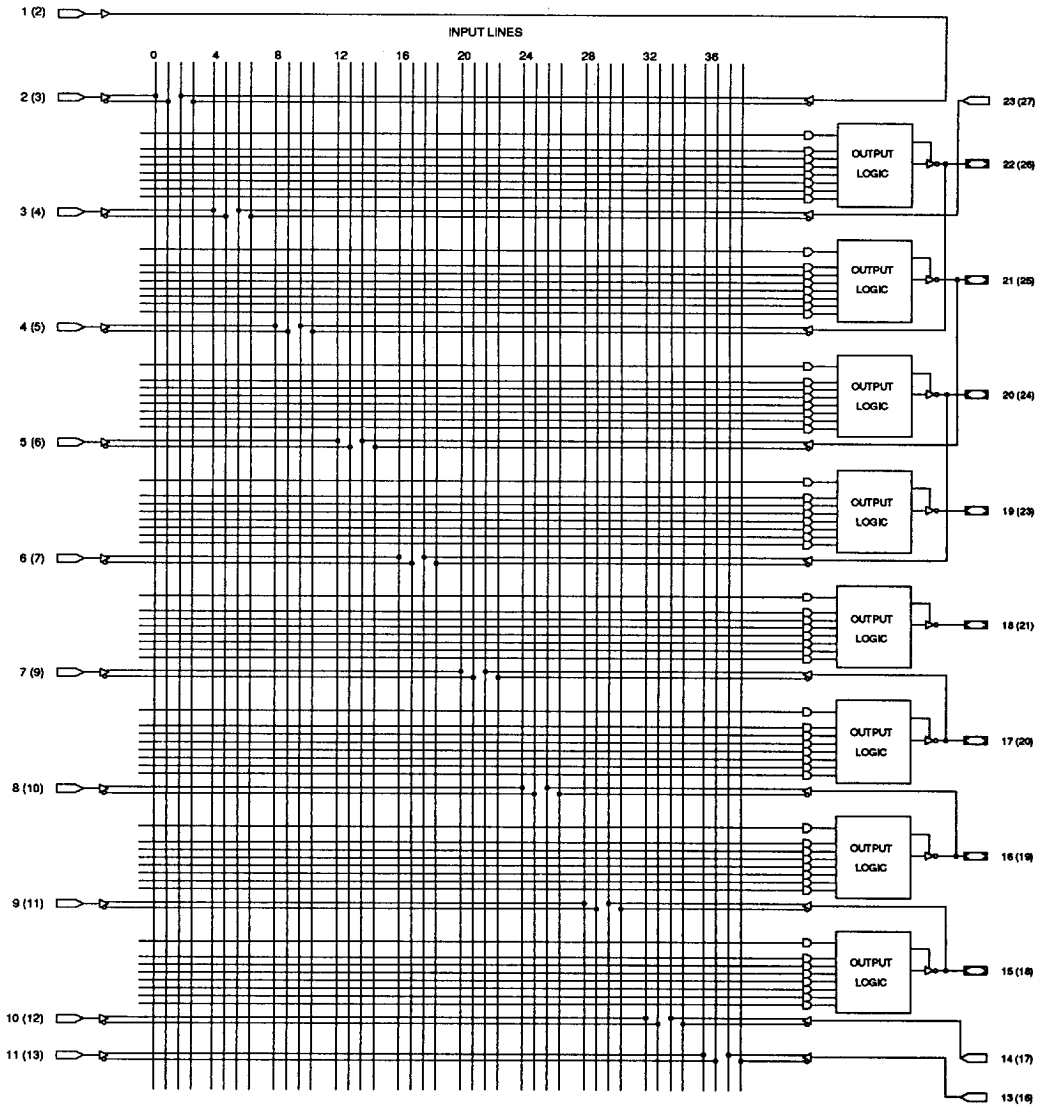
14L8	14H8	14P8
16L6	16H6	16P6
18L4	18H4	18P4
20L2	20H2	20P2

Simple Mode Option



* - Pins 18 and 19 are always enabled.

Simple Mode Logic Diagram



Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
7.5	5	5	ATF20V8B-7GC ATF20V8B-7JC ATF20V8B-7PC	24D3 28J 24P3	Commercial (0°C to 70°C)
10	7.5	7	ATF20V8B-10GC ATF20V8B-10JC ATF20V8B-10PC ATF20V8B-10SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF20V8B-10GI ATF20V8B-10JI ATF20V8B-10PI ATF20V8B-10SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF20V8B-10GM ATF20V8B-10NM	24D3 28L	Military (-55°C to 125°C)
			ATF20V8B-10GM/883 ATF20V8B-10NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
15	12	10	ATF20V8B-15GC ATF20V8B-15JC ATF20V8B-15PC ATF20V8B-15SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF20V8B-15GI ATF20V8B-15JI ATF20V8B-15PI ATF20V8B-15SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF20V8B-15GM ATF20V8B-15NM	24D3 28L	Military (-55°C to 125°C)
			ATF20V8B-15GM/883 ATF20V8B-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant
25	15	12	ATF20V8B-25GC ATF20V8B-25JC ATF20V8B-25PC ATF20V8B-25SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF20V8B-25GI ATF20V8B-25JI ATF20V8B-25PI ATF20V8B-25SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)

Ordering Information

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	12	10	ATF20V8BL-15GC ATF20V8BL-15JC ATF20V8BL-15PC ATF20V8BL-15SC	24D3 28J 24P3 24S	Commercial (0°C to 70°C)
			ATF20V8BL-15GI ATF20V8BL-15JI ATF20V8BL-15PI ATF20V8BL-15SI	24D3 28J 24P3 24S	Industrial (-40°C to 85°C)
			ATF20V8BL-15GM ATF20V8BL-15NM	24D3 28L	Military (-55°C to 125°C)
			ATF20V8BL-15GM/883 ATF20V8BL-15NM/883	24D3 28L	Military/883C (-55°C to 125°C) Class B, Fully Compliant

Package Type	
24D3	24 Lead, 0.300" Wide, Ceramic Dual Inline Package (Cerdip)
28J	28 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28L	28 Pad, Ceramic Leadless Chip Carrier (LCC)
24P3	24 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)