

# Am9114/Am91L14

1024x4 Static RAM

## DISTINCTIVE CHARACTERISTICS

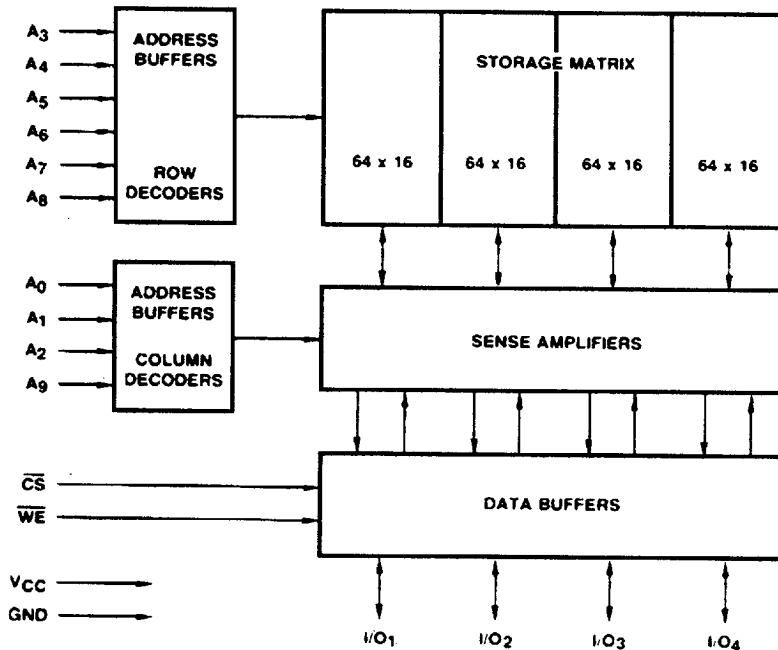
- Low operating and standby power
- Access times down to 200 ns
- Am9114 is a direct plug-in replacement for 2114
- High output drive: 3.2-mA sink current @ 0.4 V
- TTL-identical input/output levels

## GENERAL DESCRIPTION

The Am9114/Am91L14 Series are high-performance, static, N-Channel, read/write, random-access memories organized as 1024 x 4. Operation is from a single 5-V supply, and all input/output levels are identical to standard TTL specifications. Low-power version is available with power savings of over 30%.

Data readout is not destructive and the same polarity as data input.  $\overline{CS}$  provides for easy selection of an individual package when the outputs are OR-tied. The outputs of 3.2 mA for Am9114 provides increased short-circuit current for improved capacitive drive.

## BLOCK DIAGRAM



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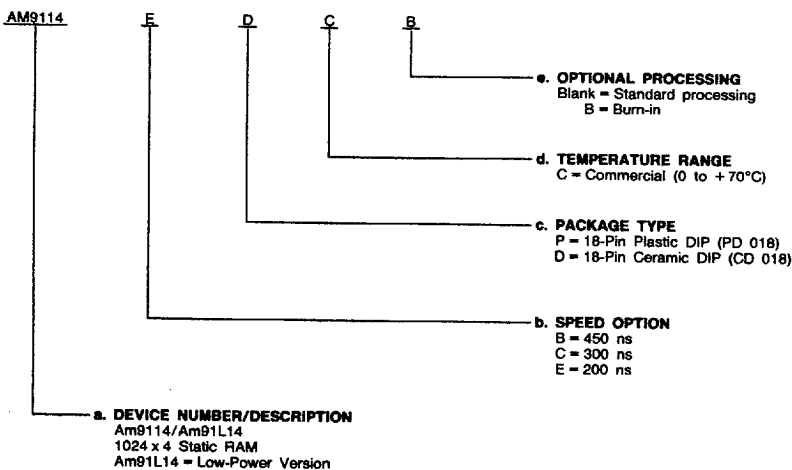


## ORDERING INFORMATION

### Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing



Valid Combinations	
AM9114B	PC, PCB, DC, DCB
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

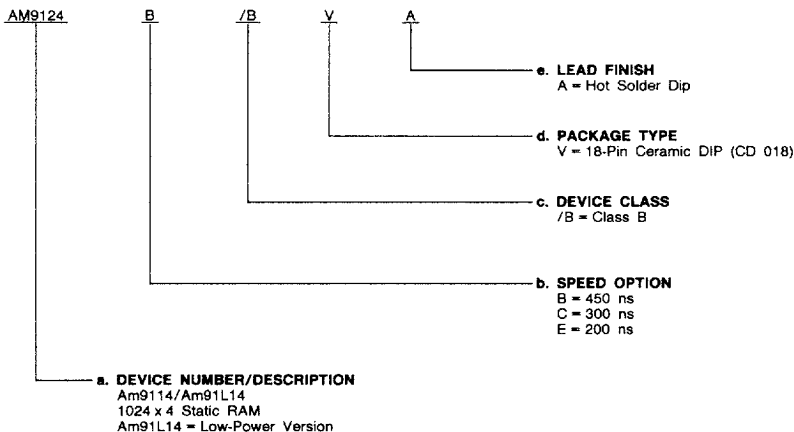
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## MILITARY ORDERING INFORMATION

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM9114B	/BVA
AM91L14B	
AM9114C	
AM91L14C	
AM9114E	
AM91L14E	

#### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult MSIS sales department to confirm availability of specific valid combinations, and to obtain additional data on MSIS's standard military grade products.

#### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

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## PIN DESCRIPTION

**A<sub>0</sub> - A<sub>9</sub> Address Inputs**

The address input lines select the memory location from which to read or write.

**$\overline{CS}$  Chip Select (Input, Active LOW)**

The  $\overline{CS}$  line selects the memory device for active operation.

**$\overline{WE}$  Write Enable (Input, Active LOW)**

When both  $\overline{CS}$  and  $\overline{WE}$  are LOW, data on the input lines is written to the location presented on the address input lines.

**I/O<sub>1</sub> - I/O<sub>4</sub> Data In/Out Bus (Bidirectional)**

These lines provide the path for data to be written to or read from the selected memory location.

**V<sub>CC</sub> Power Supply**

**V<sub>SS</sub> Ground**

**TABLE 1. SUPPLY CURRENT ADVANTAGE**

Configuration	Part Number	Worst Case Current (mA at 0°C)	
		100% Duty Cycle	50% Duty Cycle
2K x 8	9114	280	280
	91L14	200	200
4K x 12	9114	840	840
	91L14	600	600
8K x 16	9114	2240	2240
	91L14	1600	1600

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### ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage .....	-0.5 V to +7.0 V
Signal Voltages with Respect to Ground .....	-0.5 V to +7.0 V
Power Dissipation .....	1.0 W
DC Output Current .....	10 mA

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

### OPERATING RANGES (Note 2)

Commercial (C) Devices	
Ambient Temperature (T <sub>A</sub> ) .....	0°C to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5V to +5.5 V
Military (M) Devices*	
Case Temperature (T <sub>C</sub> ) .....	-55°C to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

\*Military products 100% tested at T<sub>C</sub> = +25°C, +125°C and -55°C.

### DC CHARACTERISTICS over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
I <sub>OH</sub>	Output HIGH Current	V <sub>CC</sub> = +4.5V V <sub>OH</sub> = 2.4V	91(L)14	-1.0		mA
I <sub>OL</sub>	Output LOW Current	V <sub>OL</sub> = 0.4V	T <sub>A</sub> = 70°C 91(L)14 T <sub>A</sub> = +125°C 91(L)14	3.2	2.4	
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage			-0.5	0.8	
I <sub>IX</sub>	Input Load Current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>			10	μA
I <sub>OZ</sub>	Output Leakage Current	V <sub>SS</sub> ≤ V <sub>O</sub> ≤ V <sub>CC</sub> Output Disabled	T <sub>A</sub> = 0 to +70°C T <sub>A</sub> = -55 to +125°C	-10	10	
I <sub>OS</sub>	Output Short Circuit Current	(Note 3)	91(L)14C 91(L)14M		75	mA
I <sub>CC</sub>	Operating Supply Current	V <sub>CC</sub> = Max. CS ≤ V <sub>IL</sub>	T <sub>A</sub> = 0°C T <sub>A</sub> = -55°C		70 50	
C <sub>IN</sub>	Input Capacitance	(Note 7)	f = 1.0 MHz, T <sub>A</sub> = 25°C, All pins at 0V		7	pF
C <sub>I/O</sub>	I/O Capacitance				7	

- Notes: 1. Absolute Maximum Ratings are intended for user guidelines and are not tested.  
 2. For test and correlation purposes, ambient temperature is defined as the "Instant-ON" case temperature.  
 3. For test purposes, not more than one output at a time should be shorted. Short-circuit test duration should not exceed 30 seconds. Actual testing is performed for only 5 ms.  
 4. Test conditions assume signal transition time of 10 ns or less, timing reference levels of 1.5 V, output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> plus 100 pF or plus 5 pF for T<sub>CX</sub>, T<sub>OTD</sub> and T<sub>OTW</sub>.  
 5. The internal write time of the memory is defined by the overlap of CS LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.  
 6. The specified address access time will be valid only when Chip Select is low soon enough for t<sub>CC</sub> to elapse.  
 7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.  
 8. Transition is measured from 1.5 V on the input to (V<sub>OH</sub> - 500 mV) and (V<sub>OL</sub> + 500 mV) on the output.

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**SWITCHING CHARACTERISTICS** over operating ranges unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Notes 4 – 6)

No.	Parameter Symbol	Parameter Description	B Devices		C Devices		E Devices		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>									
1	t <sub>RC</sub>	Address Valid to Address Do Not Care Time (Read Cycle Time)	450		300		200		ns
2	t <sub>A</sub>	Address Valid to Data Out Valid Delay (Address Access Time)		450		300		200	ns
3	t <sub>CO</sub>	Chip Select LOW to Data Out Valid (Note 6)		120		100		70	ns
4	t <sub>CX</sub>	Chip Select LOW to Data Out On (Notes 7, 8)	10		10		10		ns
5	t <sub>OTD</sub>	Chip Select HIGH to Data Out Off (Notes 7, 8)		100		80		60	ns
6	t <sub>OHA</sub>	Output hold after address change	50		50		50		ns
<b>WRITE CYCLE</b>									
7	t <sub>WC</sub>	Address Valid to Address Do Not Care Time (Write Cycle Time)	450		300		200		ns
8	t <sub>W</sub>	Write Enable LOW to Write Enable HIGH Time (Note 5)	200		150		120		ns
9	t <sub>WR</sub>	Write Enable HIGH to Address Do Not Care Time	0		0		0		ns
10	t <sub>OTW</sub>	Write Enable LOW to Data Out Off Delay (Notes 7, 8)		100		80		60	ns
11	t <sub>DW</sub>	Data In Valid to Write Enable HIGH Time	200		150		120		ns
12	t <sub>DH</sub>	Write Enable HIGH to Data In Do Not Care Time	0		0		0		ns
13	t <sub>AW</sub>	Address Valid to Write Enable LOW Time	0		0		0		ns
14	t <sub>CW</sub>	Chip Select LOW to Write Enable HIGH Time (Note 5)	200		150		120		90

Notes: See notes following DC Characteristics table.

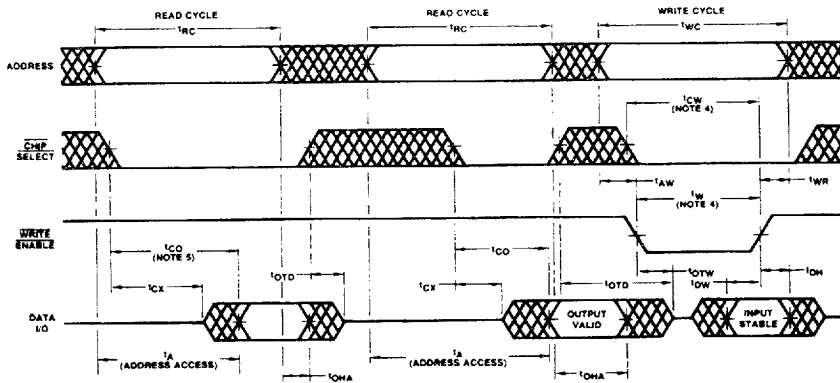
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# SWITCHING WAVEFORMS

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING, STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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WF000171

Notes: See notes following DC Characteristics table.

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Am9114/Am91L14

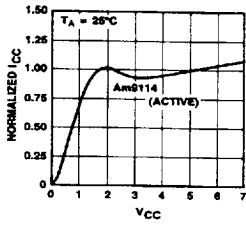
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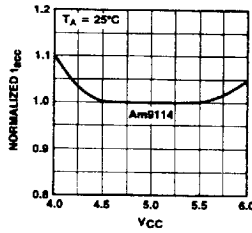
## TYPICAL PERFORMANCE CURVES

**Normalized Supply Current  
Versus Supply Voltage**



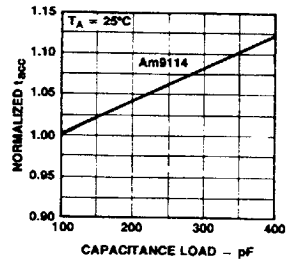
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**Normalized Access Time  
Versus Supply Voltage**



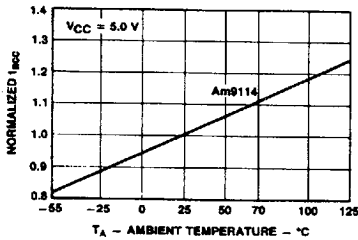
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**Normalized Access Time  
Versus Output Loading**



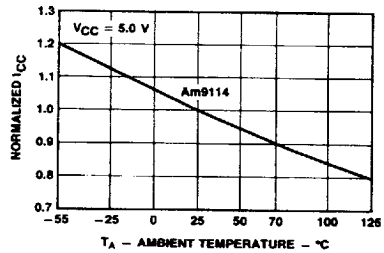
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**Normalized Access Time  
Versus Ambient Temperature**



OP000202

**Normalized Supply Current  
Versus Ambient Temperature**



OP000212

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