PRELIMINARY

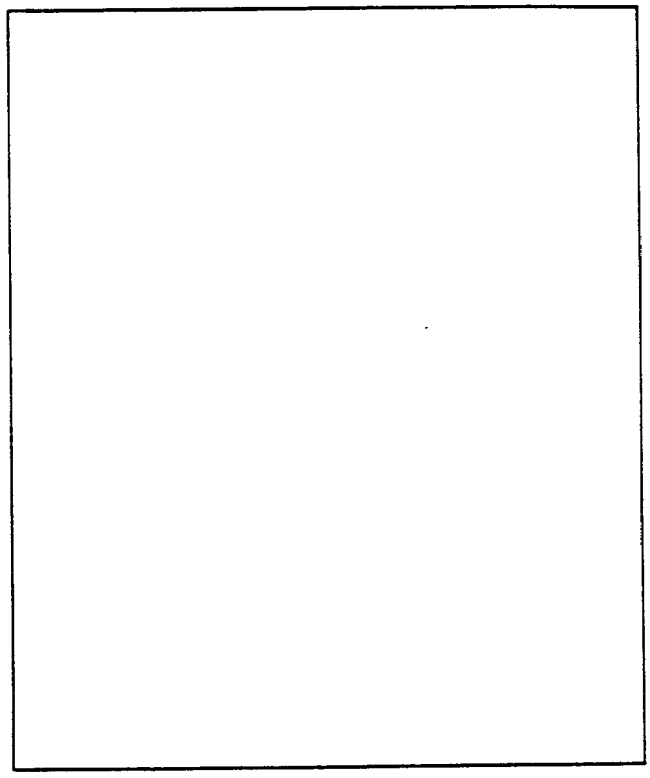
VADEM

VG-110 AND VG-210 MULTIFUNCTION PERIPHERAL CHIPS FOR THE NEC V-40 PROCESSOR

March 1989

FEATURES

- ☐ Provides IBM PC/XT compatibility
- ☐ Low power 1.5 micron CMOS technology
- ☐ Functionality includes
  - — Keyboard logic
  - — Printer port
  - — CPU and DMA bus control logic
  - — Speaker control logic
  - — System configuration registers
  - — Parity logic including parity generator
  - — DRAM controller and refresh logic
  - — Peripheral I/O address decoder
  - — Memory address decoder
  - — NMI control register
- ☐ Minimum component count for IBM PC/XT implementation
- ☐ Takes full advantage of on-board timers, DMA and interrupt logic on the V-40 CPU
- ☐ Operation to 10 Mhz with zero wait states
- ☐ Supports ROM DISK when used with Vadem BIOS
- ☐ Each chip in 64-pin QFP
- ☐ Includes parallel printer port and supports V-40 SIO, eliminating external logic



DESCRIPTION

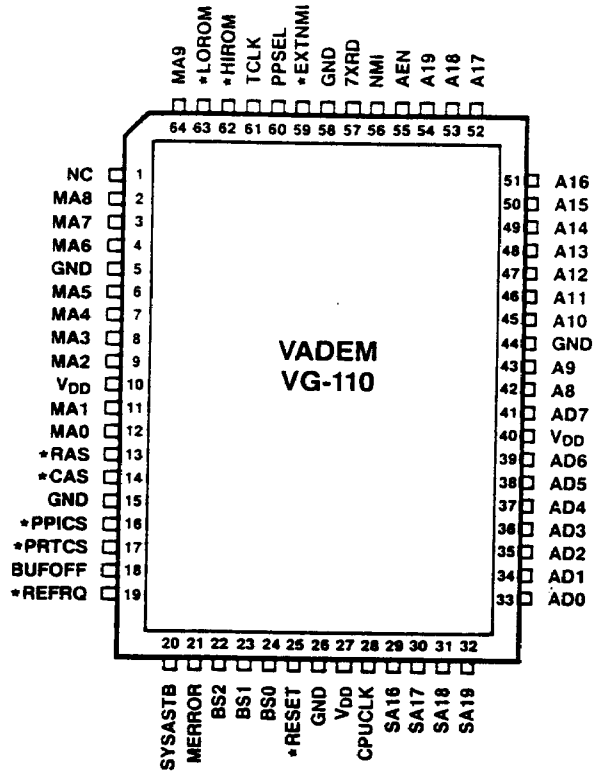
The Vadem VG-110 and VG-210 constitute a powerful two-chip set that, together with the NEC V-40 processor, enables OEMs and system designers to build low cost, high performance, compact IBM PC or PC/XT compatible systems with a minimum component count and hence, minimum size and cost. The VG-110/210 are ideal for embedded or dedicated PC applications because of their low power requirements, minimum component count, and their unique ability to work with Vadem's ROM DISK architecture enabling the easy design of a diskless PC compatible system.

The VG-110/210 are structured to provide PC compatibility for the V-40 CPU in the areas of DMA control, I/O control, keyboard and speaker interface, parallel printer port, RAM memory control and timing. The VG-110/210 provide a sophisticated emulation capability to allow the V-40's on board DMA controller to operate in a PC compatible manner. The emulation is achieved through interaction of the chip set with Vadem's BIOS and is transparent to any software. This emulation is done at no loss of performance. In fact, the VG-110/210, running with the V-40 at 10 Mhz with zero wait states, provide more than three times the performance level of a standard IBM PC/XT.

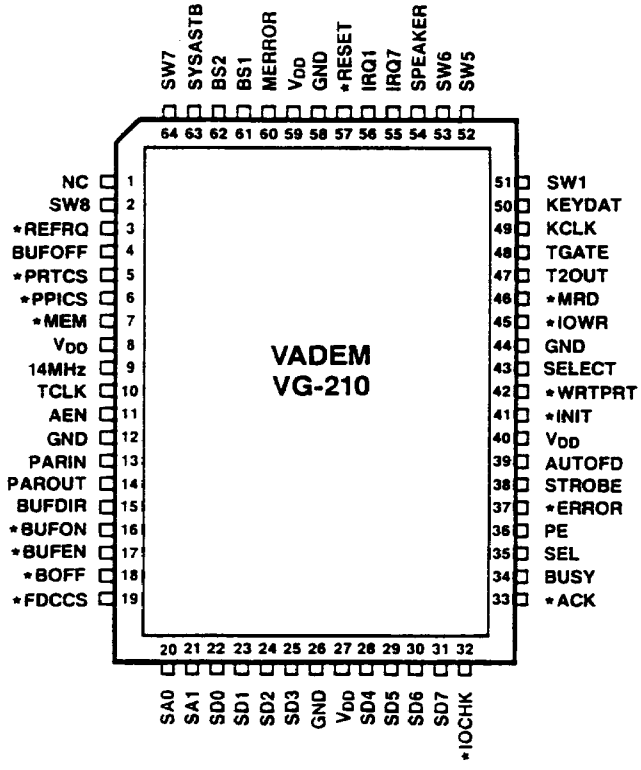
In combination with the V-40, the VG-110/210 provide an 80C88 compatible CPU, 8284 Clock Generator, 8288 Bus Controller, 8237 DMA Controller, 8259 Interrupt Controller, 8253 Timer, 8255 Peripheral Interface and Keyboard Controller and the glue logic required to interface all these elements with each other. The normal 640K of DRAM is addressable.

VG-110 AND VG-210 MULTIFUNCTION PERIPHERAL CHIPS FOR THE NEC V-40 PROCESSOR

VG-110 PIN CONFIGURATION



VG-210 PIN CONFIGURATION



VG-110 PIN DESCRIPTION

NAME	PIN	I/O	FUNCTION
BUFOFF	18	O	This active high output should be connected to the BUFOFF input of the VG-210. Signal goes high when I/O hex address 00–FF are accessed. A CPU access to F0000–FFFFF will also force BUFOFF high.
AD[0:7]	33–39, 41	I/O	V-40 address/data lines 0–7.
A[8:19]	42–43, 45–54	I	V-40 addresses 8–19.
MA[0:7] (Note 1)	3–4, 6–9, 11–12	O	Multiplexed *RAS/*CAS and refresh addresses for DRAM. During *RAS, CPU addresses A[0:7] are sent out; during *CAS, addresses A[9:16] are transmitted; during a refresh, addresses A[0:7] are sent.
MA8	2	O	Multiplexed *RAS/*CAS and refresh address for DRAM. During *RAS, CPU address A8 is sent out; during *CAS, address A17 is transmitted; during a refresh, refresh address A8 is sent.
MA9	64	O	Multiplexed *RAS/*CAS and refresh address for DRAM. During *RAS, CPU address A18 is sent out; during *CAS, address A19 is transmitted; during a refresh, MA9 is a don't care.
*REFRQ	19	I	Refresh request from V-40.
MERROR	21	I	Parity error output from VG-210. Includes error results for both on-board and expansion RAMs.
CPUCLK	28	I	V-40 CMOS clock output; actually system clock divided by 2.
*RAS	13	O	Active low row select. Goes low during memory cycles and refresh cycles. Active from 0 to 1 Mbyte. Should be connected to all RAMs directly without decoding.
*CAS (Note 2)	14	O	Active low column select. Goes low during memory cycles and high during refresh. Active from 0 to 1 Mbyte. External bank decoding required. CAS is delayed 2 clocks during DMA write.
7XRD	57	I/O	7XRD goes high when I/0 72 or 73 is read. I/O 72 can be used as an OEM configuration register. This is done with a XX244 buffer on the AD bus. The signal 7XRD must be qualified with A0 being low to enable the XX244. AD5 should not be driven since it is driven from the VG-110. If a register is present, the XX244 should drive AD7 low to indicate the data is valid. A high indicates (a pull-up) that a register isn't present. I/O 73 is an internal read/write register in the VG-110 that is used by the BIOS. The signal 7XRD must also be used to disable the AD to SD XX245 when reading I/O 72 or 73. This can be done by OR'ing 7XRD and the enable for the XX245.
NMI	56	O	Sent to V-40 NMI input pin. This is an OR'ing of RAM parity results, 8087 interrupt, EXTNMI, and other proprietary logic. A high indicates an NMI.
PPSEL	60	I	This directs one of two internally-decoded printer port addresses to appear on PRTCS. When low, I/O addresses 3BC-3BE will appear, and when high, addresses 378H-37FH. TTL input with internal pullup resistor.
*EXTNMI	59	I	Extra NMI input; TTL with internal pullup. OR'd with other NMI inputs, and not controlled by NMI register.
BS0	24	I	V-40 status.
BS1	23	I	V-40 CMOS bus status input. High = write; low = read.
BS2	22	I	V-40 CMOS bus status input. High = memory; low = I/O.
*LOROM	63	O	Active low. Decoded memory address from F0000 to F7FFF. Intended for OEM ROM.
*HIROM	62	O	Active low. Decoded memory address from F8000 to FFFFF. Intended for BIOS ROM.
*PRTCS	17	O	Active low. Decoded I/O address for printer. See PPSEL.
*PPICS	16	O	Active low. Decoded I/O address (60-6F — same as IBM) for 8255 controller or equivalent.
*RESET	25	I	Active low. TTL input.
SYSASTB	20	I	Active high. TTL. The result of the OR'ing of the V-40 ASTB and 8087 ASTB.
AEN	55	I	DMA cycle.
TCLK	61	I	1.9 MHz clock from VG-210.
SA[16:19]	29–32	O	System addresses. The result of input pins A[16:19] being latched internally by SYSASTB.

VG-210 PIN DESCRIPTION

NAME	PIN	I/O	FUNCTION
TGATE	48	O	Active high enable signal to V-40 timer channel 2.
SD[0:7]	22–25, 28–31	I/O	System data bus inputs.
SA0, SA1	20–21	I	System address inputs.
IRQ1	56	O	Keyboard interrupt; should be connected to Interrupt Channel 1 of V-40. A high on this pin causes an interrupt.
IRQ7	55	O	Printer interrupt; should be connected to Interrupt Channel 7 of V-40. Output is through a three-state driver. A high on this pin causes an interrupt.
SPEAKER	54	O	Active high speaker outputs. Must be buffered.
*IOCHK	32	I	Input to the parity logic from the expansion memory. TTL input with internal pull-up. A low on this pin indicates a parity error.
PARIN	13	I	TTL output signal from the parity RAM. If parity is not being used this pin should be tied to PAROUT.
*IOWR	45	I	Active low. I/O write control from the V-40.
MERROR	60	O	Parity error output to VG-110. A high indicates a parity error in either the on-board or expansion RAM.
PAROUT	14	O	Parity RAM input signal. During a memory write cycle, PAROUT will be written into the parity RAM on the falling edge of *CAS. Output level is generated by the internal parity generator.
*FDCCS	19	I	Indicates the DMA device is on the local data bus. Connect to DACK of local DMA device. Valid during DMA cycle only.
*BOFF	18	I	This is an extra input to the buffer control logic. Except when AEN is high, a low on this pin produces a high on *BUFON. This input can be used if additional hardware, such as a real-time clock, is added to the local bus, and if unused it can be left open.
*MEM (Note 3)	7	I	This is a TTL input to the buffer control logic, and should be decoded to act as an on-board memory chip select, going low only when the DRAM present on the local bus is accessed.
BUFDIR	15	O	This signal controls the direction for both CPU and DMA data cycles, and should be connected to the direction pin on the expansion bus data buffer. The control logic will adapt to the amount of memory on the local bus and the location of the floppy disk controller.
BUFOFF	4	I	This active high input should be connected to the BUFOFF output of the VG-110. Signal goes high when I/O address 00–FF is accessed. A CPU access to F0000–FFFFF will also force BUFOFF high.
SYSASTB	63	I	Active high TTL input. The result of the OR'ing of the V-40 ASTB and the 8087 ASTB.
AEN	11	I	A high on this TTL input indicates that there is a DMA address on the bus. Signal can be created by NAND'ing the V-40 *DACK signals together with the *REFRQ.
SW5, SW6	52–53	I	Indicates the type of display adapter being used. TTL inputs with internal pull-ups. SW6 SW5 Type L L Reserved L H CGA 320 x 200 H L CGA 640 x 200 H H Monochrome 80 x 25
*RESET	57	I	Active low TTL input.
SW7, SW8	64, 2	I	Sets the number of floppy disk drives installed. TTL inputs with internal pull-ups. SW8 SW7 Number L L 1 L H 2 H L 3 H H 4
*REFRQ	3	I	Refresh request from V-40.
BS1	61	I	Bus status from V-40.
*BUFEN	17	I	Buffer enable control from the V-40.
*ERROR (Note 4)	37	I	A low on this pin indicates a printer error.
SEL (Note 4)	35	I	A high means that the printer has been selected.
BUSY (Note 4)	34	I	A high indicates that the printer is busy and not ready for data.
PE (Note 4)	36	I	A high means that the printer is out of paper.

VG-210 PIN DESCRIPTION (continued)

NAME	PIN	I/O	FUNCTION
*ACK (Note 4)	33	I	A low indicates that the character has been received.
STROBE	38	O	Positive going pulse which strobes data into the printer. Should be inverted once.
AUTOFD	39	O	A high enables a line feed after each line of data is printed. Should be inverted once.
*INIT	41	O	A high resets the printer. Should be inverted once.
SELECT	43	O	A high selects the printer. Should be inverted once.
KEYDAT	50	I/O	Keyboard bidirectional serial data. TTL input with internal pull-up.
*PRTCS	5	I	Printer port chip select input. Active low TTL input with internal pull-up.
*PPICS	6	I	Chip select input for 8255 logic, including keyboard controller and configuration register. Active low TTL input with internal pull-up.
T2OUT	47	I	V-40 timer channel 2 clock output.
*MRD	46	I	V-40 memory read control.
*BUFON	16	O	This output should be connected to the enable pin of the expansion bus data buffer. It will disable the buffer when BUFOFF (VG-110) goes high; when FDCCS, PRTCS, PPICS, or BOFF inputs go low; or whenever the local RAM is accessed. This control logic adapts to the amount of memory on the system bus and the location of the floppy disk controller, and functions the same whether during a CPU or a DMA cycle.
14 MHz	9	I	From 14.31818 MHz source.
TCLK	10	O	1.19 MHz output.
SW1	51	I	Low = no floppies. TTL input with internal pull-up.
KCLK	49	I/O	Bidirectional keyboard clock
*WRTPRT	42	O	Output to latch printer data into external latch.

Notes:

(1) Address multiplexer is designed to use either 256K x 1 or 1M x 1 DRAMs.

(2) If three banks of 256K or 1M DRAMs are located on the local bus, caution must be used when decoding for CAS. The standard PC display adapter resides in B0000-BFFFF and the EGA adapter starts at A0000. Therefore, decoding for CAS must insure that the DRAM is disabled when the display adapter is addressed. If 1M DRAMs are used, care must be taken to avoid bus conflicts above C0000 as well.

(3) If three banks of 256K (or one bank of 1M) DRAMs are located on the local bus, caution must be used when decoding MEM. The standard PC display adapter resides in B0000–BFFFF and the EGA adapter starts at A0000. Therefore, decoding for MEM must insure that it is high when the display adapter is addressed. If 1M DRAMs are used, care must be taken to avoid bus conflicts above C0000 as well. If less than 640K of memory is present on the local bus, MEM must be active for only the amount of memory present.

(4) These five signals are printer status inputs. All are TTL inputs.

VG-110/210 FUNCTIONAL DESCRIPTION

The VG-110 and VG-210 Multifunctional Peripheral Chips are designed to work with the NEC V-40 processor to implement a PC/XT compatible system environment.

V-40

The V-40 integrates many peripheral circuits used in the PC with an 8088-compatible CPU on a single chip. The peripherals include a clock generator, bus controller, bus arbitrator, programmable wait state generator, DRAM Refresh Controller, three channel timer/counter, asynchronous SIO channel, eight channel interrupt controller and four channel direct memory access controller.

INTERRUPT CONTROLLER AND TIMER

The V-40 interrupt controller and timer are hardware and software compatible with the PC architecture.

DMA CONTROLLER

The V-40 DMA controller is faster than that used in a PC, is set up differently and provides a 20-bit DMA register. In all other areas, the V-40 DMA controller is functionally identical to the 8237 used in the PC. Systems built with the V-40 and VG-110/210 must connect PC DMA channel 0 to the V-40 memory refresh controller and remap the remaining channels to free up the V-40 DMA channel 3 as shown in the table below.

V-40	PC/XT
Refresh Controller	DMA Channel 0
DMA Channel 0	DMA Channel 1
DMA Channel 1	DMA Channel 2
DMA Channel 2	DMA Channel 3
DMA Channel 3	Not available

DMA Channel 3 on the V-40 can be used as an additional DMA channel in the system, or is selectable as an SIO which can be used as mouse port or simplified SIO. The Vadem BIOS supports the V-40 SIO option as COM3 or a mouse port.

This remapping is transparent to software running on the PC when the VG-110/210 are used with the Vadem BIOS. Full PC hardware compatibility is maintained. The VG-110 traps on all IO instructions related to the DMA Controller and DMA page register. When an "ill behaved" PC program accesses the hardware directly, the VG-110 generates an NMI to the V-40. The NMI interrupt routine in the Vadem BIOS will then perform a functionally equivalent task on the V-40 DMA controller. The normal PC usage of NMI for parity error generation still functions correctly.

RAM CONTROLLER

The VG-110 provides controller logic for both Dynamic and Static RAM. It contains a dynamic RAM controller which has a RAS/CAS generator and address MUX. Both RAS and CAS outputs are active from 0 to 1MB. The address multiplexer is designed for 256K x 1 or 256K x 4 or 1M x 1 DRAMs and is output on the MA bus. During a refresh cycle, RAS goes low, CAS remains high and the refresh address is output on the MA bus. Since RAS is active during a refresh cycle, it should be connected to all the RAMs without bank decoding.

CAS, however, needs address decoding to generate individual CAS for each memory bank. Whenever any CAS bank line is active, a signal must be input to the *MEM input of the VG-210. This *MEM signal indicates when the DRAM on the local CPU data bus is addressed. DRAM may overlap the video adapter address space and other ROMs (Hard Disk, etc). Care must be used to avoid the DRAM and other hardware being on simultaneously.

In Static RAM mode, MA0:7 output a latched version of AD0:7 which can be used as SA0:7.

ADDRESS DECODING

Additional decoding is provided by the VG-110 to eliminate external glue chips. Chip selects are provided for a printer port at addresses 3BC–3BF or 378–37F, an 8255 at 60–6F and for two ROMs. *LOROM is at address F0000–F7FFFF and *HIROM is at address F8000–F7FFF.

KEYBOARD/SPEAKER/CONFIGURATION REGISTER/PARITY

The VG-210 contains a PC/XT compatible keyboard controller, speaker logic and configuration register. These are the equivalent of an 8255. The VG-210 provides a parity generator for local RAM and an input (*IOCHK) for any expansion RAM. Results are output on the MERROR pin. The VG-210 MERROR pin should be connected to the VG-110 MERROR input pin so that the VG-110 will generate an NMI pulse when a parity error is detected.

PRINTER PORT

The VG-210 contains a full PC compatible printer port. It is a parallel port with 8 data bits, control outputs and status inputs. An external 8-bit latch is needed for the printer port data. This data is mirrored in the VG-110 to enable programs to read back printer data.

External open collector inverters are needed for the printer control outputs.

EXPANSION BUS FLOW CONTROL LOGIC

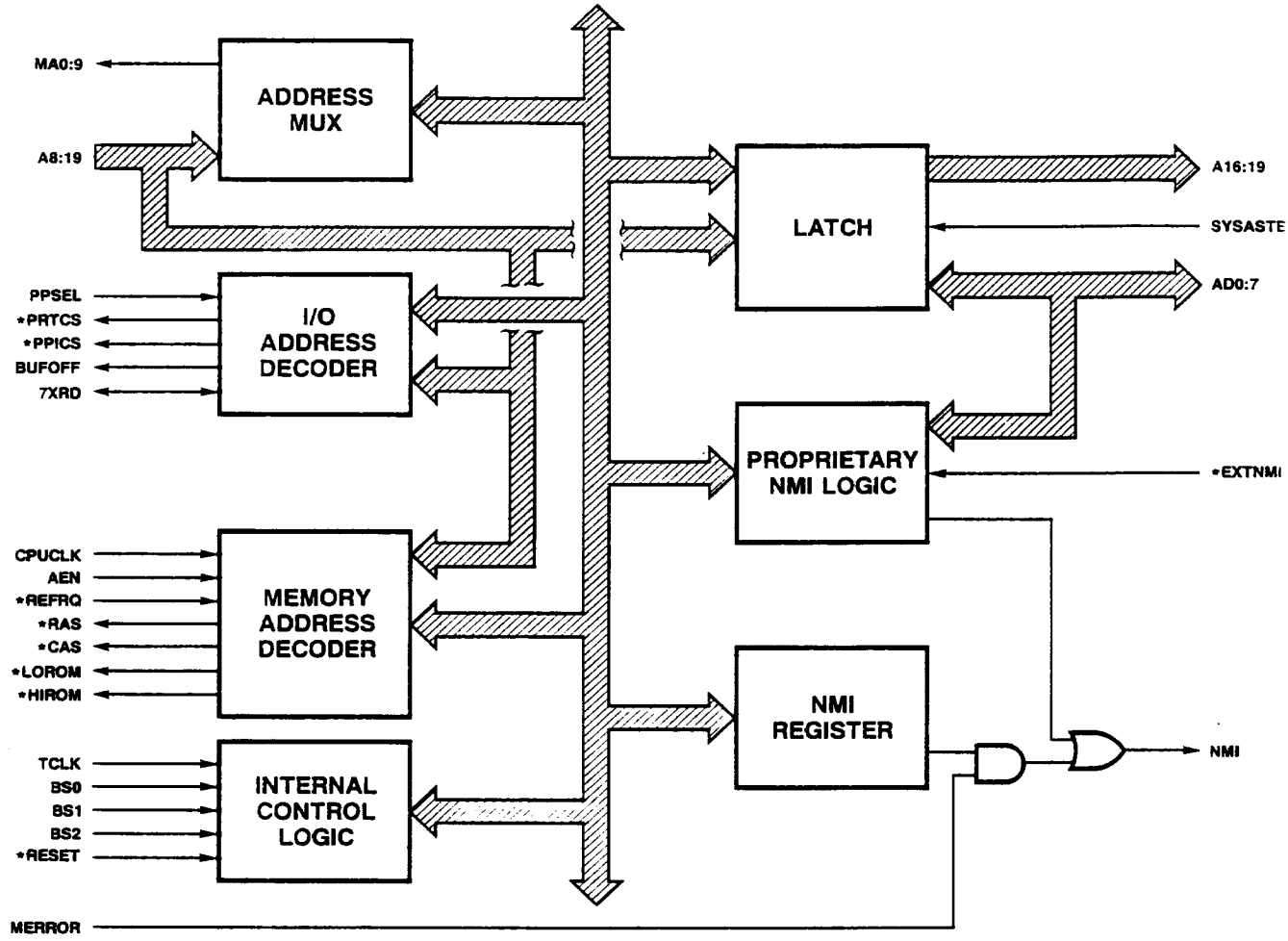
The VG-210 contains expansion bus data buffer control circuitry. This logic provides both a buffer enable and buffer direction output. These signals are active for both CPU and DMA cycles. Using the data provided by input pins *MEM, *FDCCS and *BOFF, this control circuit adapts to the size of the local RAM and the location of the floppy controller which can be on the local bus or expansions bus. For example, when there is a DMA read (*MRD, *IOWR) to local memory and the floppy disk controller is on the expansion bus, *BUFON will go low and BUFDIR will reverse direction. If the floppy disk controller is on the local data bus and local memory is addressed, *BUFON will be high.

An additional input to this control logic is provided by *BOFF. When *BOFF goes low during non-DMA (its a "don't care" during DMA), *BUFON will go high. This allows adding optional hardware on the local data bus (Real Time Clock, SIO, etc).

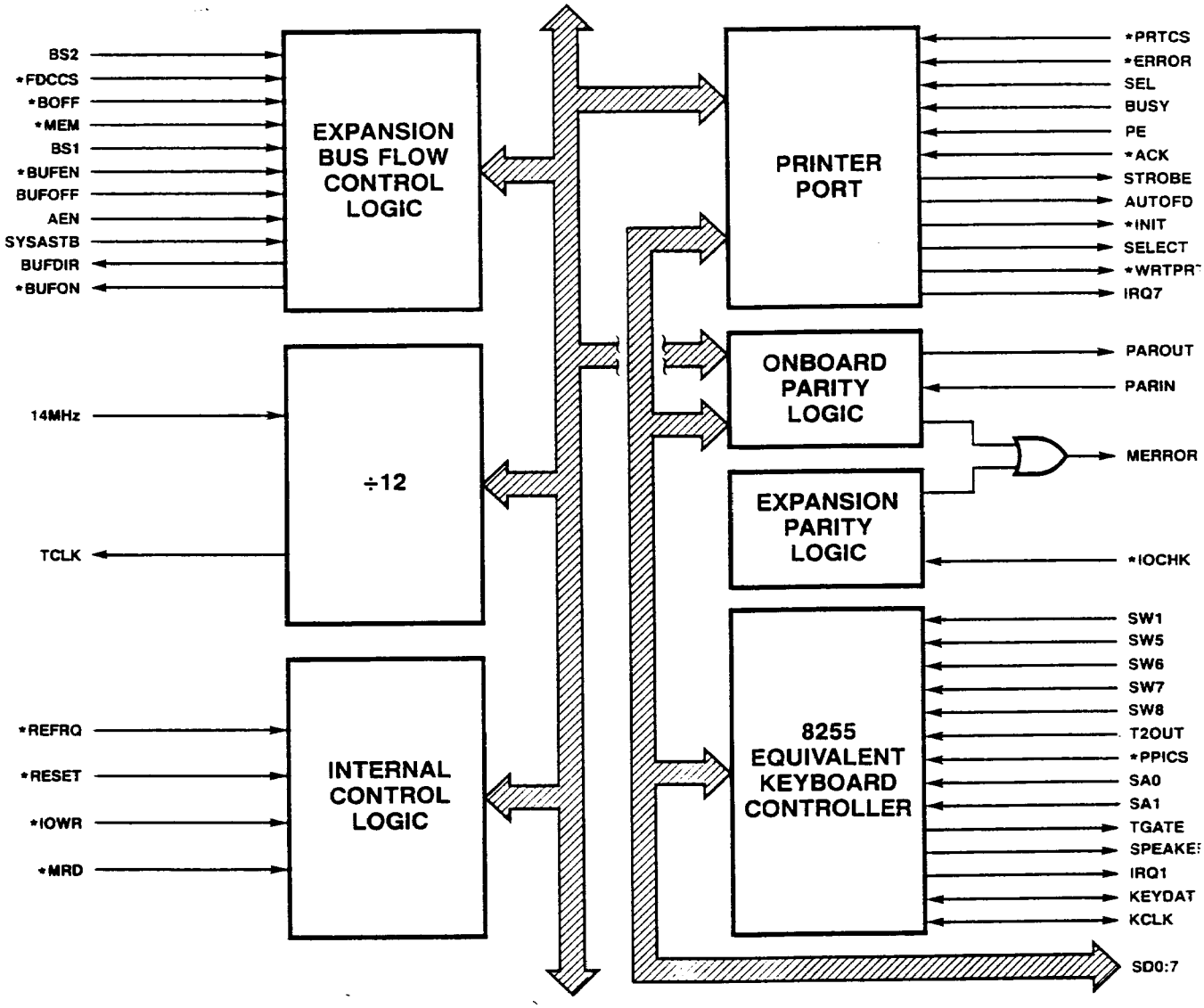
CLOCKING

The VG-210 divides the 14.31818 Mhz system clock by 12 to generate the 1.19 Mhz clock that is used as the timer clock inputs.

VG-110 BLOCK DIAGRAM



VG-210 BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$)

Parameter	Symbol	Min	Max	Unit
Supply Voltage		0	7.0	V
Input Voltage	V_{IN}	-0.5	5.5	V
Output Voltage	V_O	-0.5	V_{CC}	V
Operating Temperature	T_{op}	-25	85	°C
Storage Temperature	T_{stg}	-40	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions described under Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.75	5.25	V
Ambient Temperature	T_a	0	70	°C

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
TTL Input Low Voltage	V_{IL}	—	0.8	V
TTL Input High Voltage	V_{IH}	2.0	—	V
Clock Input Low Voltage	V_{ILC}	—	0.4	V
Clock Input High Voltage	V_{IHC}	4.0	—	V
Output Low Voltage (TTL and CMOS)	V_{OL}	—	0.45	V
Output High Voltage (TTL)	V_{OHt}	2.4	—	V
Output High Voltage (CMOS)	V_{OHc}	3.5	—	V
Output Short Circuit Current V_O=0V	I_{OS}	—	-100	mA
Input Clamp Voltage I_{IN}=-20mA, V_{CC}=4.5V	V_{IC}	—	-1.5	V
Output Leakage Current (Hi-Z)	I_{OLZ1}	-100	100	μA
Output Leakage Current (Bi-Dir)	I_{OLZ2}	-200	200	μA
Power Supply Current @ 10 MHz Clock	I_{CC}	—	20	mA
Standby Power Supply Current @ All Inputs=V_{CC} or GND	I_{STBY}		100	μA

VG-110
OUTPUT CURRENT DRIVING CAPABILITIES

Pin Name	Pin No.	I_{OL} (mA)	I_{OH} (mA)
AD0:7	33-39, 41	12	12
7XRD	57	4	4
MA0:9	2-4, 6-9, 11, 12, 64	12	12
SA16:19	29-32	12	12
*PRTCS	17	4	4
*PPICS	16	4	4
BUFOFF	18	4	4
*RAS	13	12	12
*CAS	14	12	12
*LOROM	63	4	4
*HIROM	62	4	4
NMI	56	4	4

VG-210
OUTPUT CURRENT DRIVING CAPABILITIES

Pin Name	Pin No.	I_{OL} (mA)	I_{OH} (mA)
SD0:7	22-25, 28-31	12	12
KEYDAT	50	12	12
KCLK	49	12	12
STROBE	38	4	4
AUTOFD	39	4	4
*INIT	41	4	4
SELECT	43	4	4
*WRTPRT	42	4	4
IRQ7	55	4	4
PAROUT	14	4	4
MERROR	60	4	4
TGATE	48	4	4
SPEAKER	54	4	4
IRQ1	56	4	4
BUFDIR	15	4	4
*BUFON	16	4	4
TCLK	10	4	4

VG-110/210 CAPACITANCE LOADING

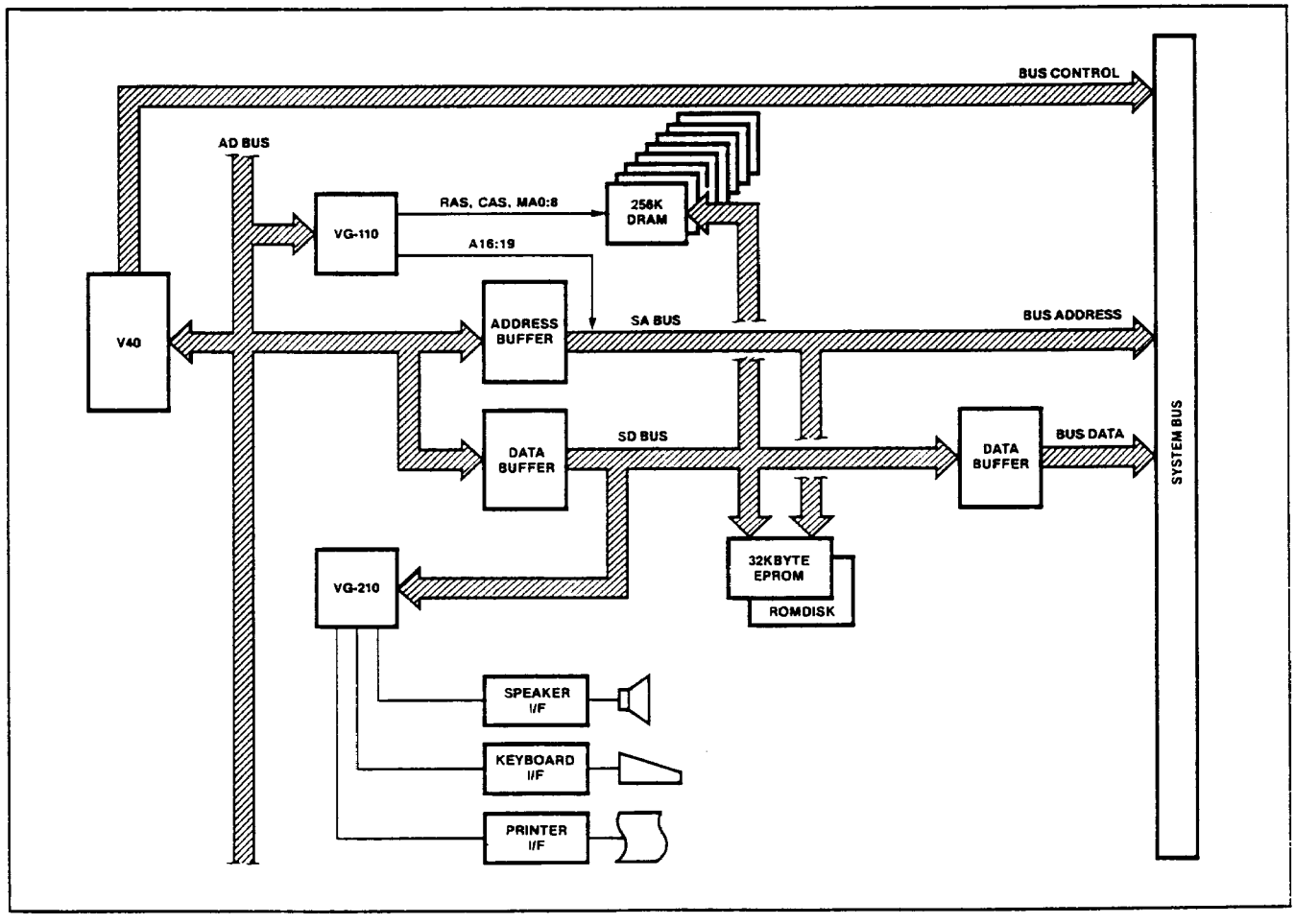
Input

All inputs have a maximum load of 10pF.

Output

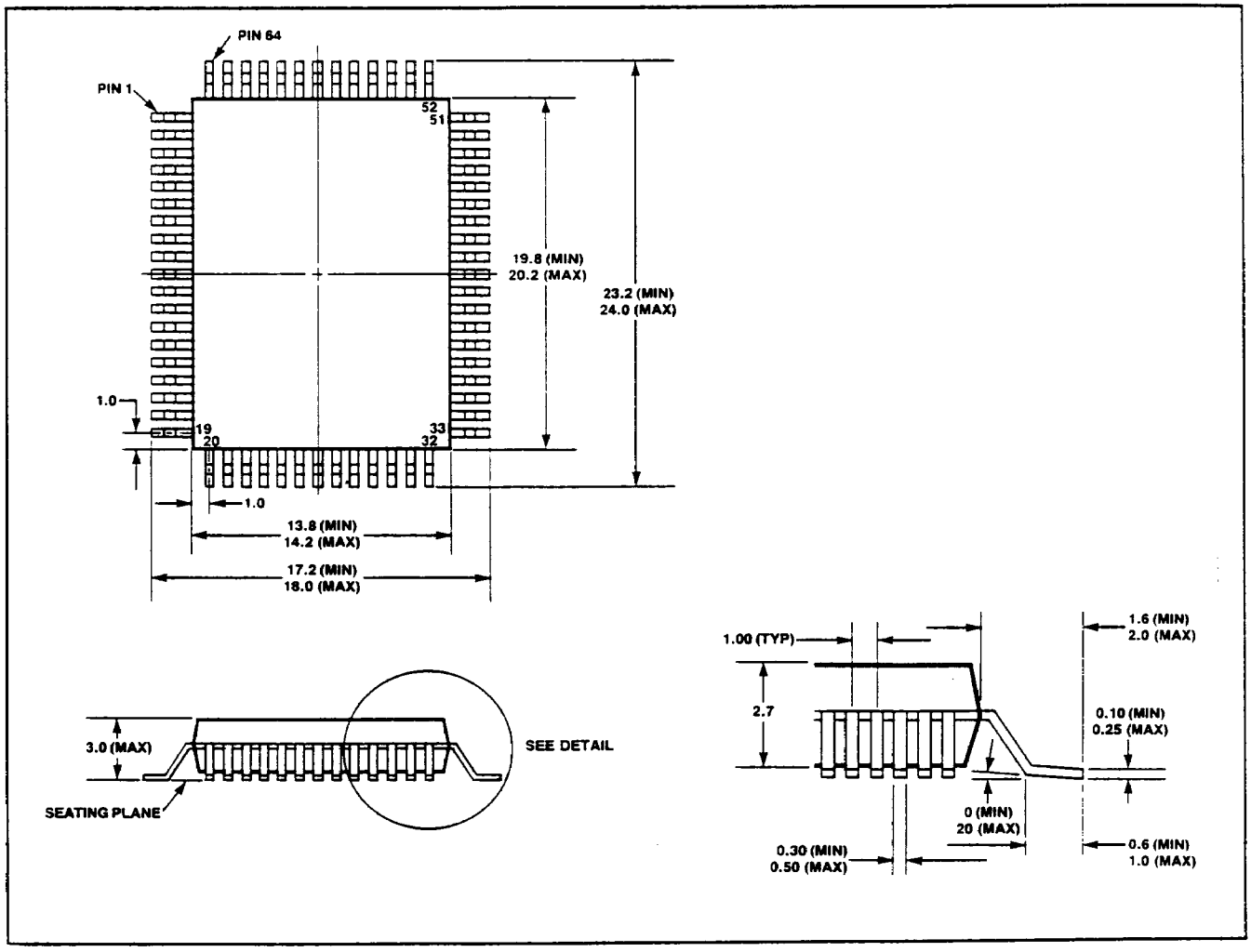
Load (C_{LOAD} Max)	VG-110 Pin	VG-210 Pin
50pF	7XRD, *PRTCS, *PPICS, BUFOFF, *LOROM, *HIROM, NMI	STROBE, AUTOFD, *INIT, SELECT, *WRTPRT, IRQ7, PAROUT, MERROR, TGATE, SPEAKER, IRQ1, BUFDIR, *BUFON, TCLK
200pF	AD[0:7], MA[0:9], SA[16:19], *RAS, *CAS	SD[0:7], KEYDAT, KCLK

SAMPLE APPLICATION



VG-110 AND VG-210 MULTIFUNCTION CHIPS FOR THE NEC V-40 PROCESSOR

PHYSICAL DIMENSIONS



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