# QuickSwitch® Products
# High-Speed CMOS βus Exchange Switches With Active Termination (βus Hold)

**QS3388**
**QS3L388**

3

## FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to $V_{CC}$
- 5Ω bidirectional switches connect inputs to outputs
- Active termination drives bus pins to rails when switches are off
- Zero propagation delay, zero ground bounce
- Undershoot clamp diodes on all switch and control pins
- Available in 24-pin QSOP
- Bus exchange allows nibble swap
- TTL-compatible input and output levels
- Bus-hold eliminates floating bus lines and reduces static power consumption

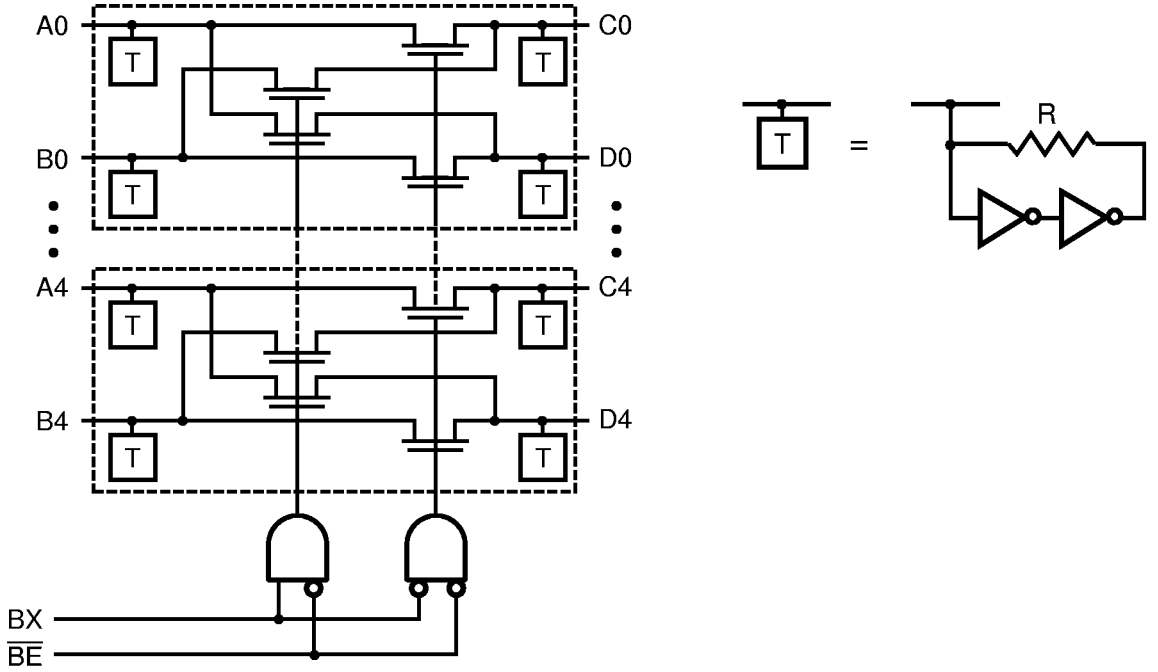
## APPLICATIONS

- Resource sharing
- Crossbar switching
- Last value latch (graphics and DSP)

## DESCRIPTION

The QS3388 (standard power) and QS3L388 (low power) provide ten high-speed CMOS TTL compatible bus switches with active terminators on the bus switch I/O pins. The low ON resistance (5Ω) of the 3388/3L388 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. When the switches are turned off, a low drive active terminator circuit drives the disconnected pins to $V_{CC}$ or ground, away from the TTL threshold. This prevents undriven buses from floating. The Bus Enable ($\overline{BE}$) signal turns the switches on. The Bus Exchange (BX) signal provides nibble swap of the AB and CD pairs of signals. This exchange configuration allows byte swapping of buses in systems. It can also be used as a five-wide 2-to-1 multiplexer and to create low delay barrel shifters, etc.

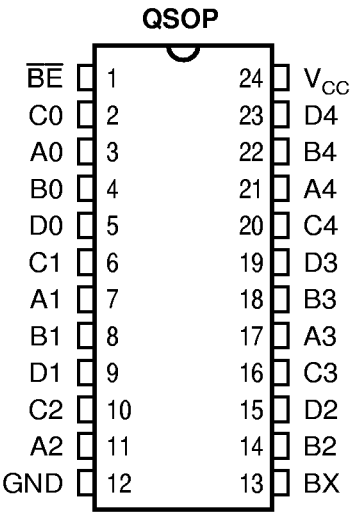
**Figure 1. Functional Block Diagram**



## Table 1. Pin Description

| Name | I/O | Function |
|---|---|---|
| A0-A4, B0-B4 | I/O | Buses A, B |
| C0-C4, D0-D4 | I/O | Buses C, D |
| $\overline{BE}$ | I | Bus Switch Enable |
| BX | I | Bus Exchange |

## Figure 2. Pin Configuration (All Pins Top View)




## Table 2. Function Table

| $\overline{BE}$ | BX | A0-A4 | B0-B4 | Function |
|---|---|---|---|---|
| H | X | Hi-Z | Hi-Z | Disconnect |
| L | L | C0-C4 | D0-D4 | Connect |
| L | H | D0-D4 | C0-C4 | Exchange |

## Table 3. Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage to Ground | –0.5V to +7.0V |
| DC Switch Voltage $V_S$ | –0.5V to +7.0V |
| DC Input Voltage $V_{IN}$ | –0.5V to +7.0V |
| AC Input Voltage (for a pulse width ≤ 20ns) | –3.0V |
| DC Output Current Max. Sink Current/Pin | 120mA |
| Maximum Power Dissipation | 0.5 watts |
| $T_{STG}$ Storage Temperature | –65° to +150°C |

**Note:** ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

## Table 4. Capacitance

$T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| Pins | QSOP Typ | QSOP Max | Unit |
|---|---|---|---|
| Control Inputs | 3 | 5 | pF |
| QuickSwitch Channels (Switch OFF) | 5 | 7 | pF |

**Note:** Capacitance is guaranteed, but not production tested. For total capacitance while the switch is ON, please see Section 1 under "Input and Switch Capacitance."

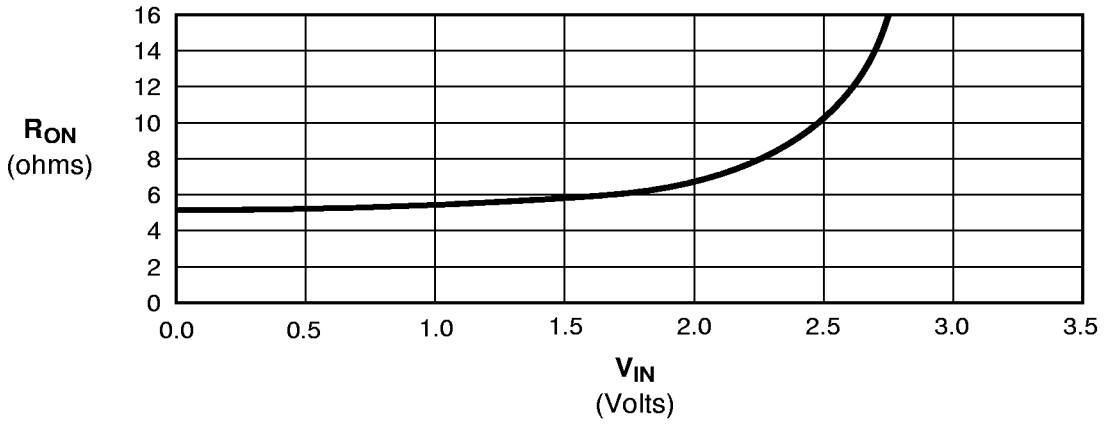
## Table 5. DC Electrical Characteristics Over Operating Range

$T_A$ = –40°C to 85°C, $V_{CC}$ = 5.0V ± 5%

| Symbol | Parameter | Test Conditions | | Min | Typ(1) | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Logic HIGH for Control Inputs | | 2.0 | — | — | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Logic LOW for Control Inputs | | — | — | 0.8 | V |
| $\lvert I_{IN} \rvert$ | Input Leakage Current (Control Inputs) | $0 \le V_{IN} \le V_{CC}$ | | — | .01 | 1 | µA |
| $R_{ON}$ | Switch ON Resistance(2) | $V_{CC}$ = Min., $V_{IN}$ = 0.0V $I_{ON}$ = 30mA | | — | 5 | 7 | Ω |
| $R_{ON}$ | Switch ON Resistance(2) | $V_{CC}$ = Min., $V_{IN}$ = 2.4V $I_{ON}$ = 15mA | | — | 10 | 15 | Ω |
| $\lvert I_{BH} \rvert$ | Input Current(3) Switch Pins | $V_{CC}$ = Max., $V_{IN}$ = 0V or $V_{IN}$ = $V_{CC}$ | | — | — | 20 | µA |
| | | $V_{CC}$ = Max., 0.8V < $V_{IN}$ < 2.0V | | — | — | 500(3) | µA |
| $\lvert I_{BHH} \rvert$ | Bus Hold Sustaining(4,5) Current | $V_{CC}$ = Min | $V_{IN}$ = 2.0V | –60 | — | — | µA |
| $\lvert I_{BHL} \rvert$ | | | $V_{IN}$ = 0.8V | +60 | — | — | µA |

**Notes**:
1. Typical values indicate $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. For a diagram explaining the procedure for $R_{ON}$ measurement, please see section 1 under "DC Electrical Characteristics."
3. $|I_{BH}|$ - Magnitude of the input current specified under two conditions:
   (a) Input voltage at GND or $V_{CC}$. This indicates the input current under steady-state conditions.
   (b) Input voltage between 0.8V and 2.0V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the Bus-hold circuit.
4. $I_{BHH}$ – Minimum sustaining 'source' current at the input for $V_{IN}$ = 2.0V. This parameter signifies the latching capability of the Bus-hold circuit in logic HIGH state.
5. $I_{BHL}$ – Minimum sustaining 'sink' current at the input for $V_{IN}$ = 0.8V. This parameter signifies the latching capability of the Bus-hold circuit in logic LOW state.

## Figure 3. Typical ON Resistance vs $V_{IN}$ at $V_{CC}$ = 5.0V



## Table 6. Power Supply Characteristics Over Operating Range

$T_A$ = –40°C to 85°C, $V_{CC}$ = 5.0V ± 5%

| Symbol | Parameter | Test Conditions[1] | | Max | Unit |
|---|---|---|---|---|---|
| $I_{CCQ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$, f = 0 | 3388 | 1.5 | mA |
| | | | 3L388 | 3.0 | µA |
| $\Delta I_{CC}$ | Power Supply Current per Input HIGH[2] | $V_{CC}$ = Max., $V_{IN}$ = 3.4V, f = 0 per Control Input | | 2.5 | mA |
| $Q_{CCD}$ | Dynamic Power Supply Current per MHz[3] | $V_{CC}$ = Max., A, B, C, D Pins Open, Control Inputs Toggling @ 50% Duty Cycle | | 0.25 | mA/ MHz |

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN}$ = 3.4V, control inputs only). A, B, C, D pins do not contribute to $\Delta I_{CC}$.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A, B, C, D inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not production tested.

## Table 7. Switching Characteristics Over Operating Range

$T_A$ = –40°C to 85°C, $V_{CC}$ = 5.0V ± 5%
$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description[1] | QS3388, QS3L388 Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{PLH}$ $t_{PHL}$ | Data Propagation Delay[2,3] AiBi to CiDi, CiDi to AiBi | — | — | 0.25[3] | ns |
| $t_{PZL}$ $t_{PZH}$ | Switch Turn-on Delay $\overline{BE}$ to Ai, Bi, Ci, Di | 1.5 | — | 6.5 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Switch Turn-off Delay[2] $\overline{BE}$ to Ai, Bi, Ci, Di | 1.5 | — | 5.5 | ns |
| $t_{BX}$ | Switch Multiplex Delay BX to Ai, Bi, Ci, Di | 1.5 | — | 6.5 | ns |

**Notes:**

1. See Test Circuit and Waveforms. Minimums guaranteed, but not production tested.
2. This parameter is guaranteed, but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 50pF. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

## ACTIVE TERMINATOR OR 'BUS-HOLD' CIRCUIT

The Active Terminator circuit, also known as the Bus-hold circuit, is configured as a 'weak latch' with positive feedback. When connected to a TTL or CMOS input port, the Bus-hold circuit holds the last logic state at the input when the input is 'disconnected' from the driver. When the output of a device connected to such an input attempts a logic level transition, it will overdrive the Bus-hold circuit. The primary benefit of a Bus-hold circuit is that it prevents CMOS inputs from floating, a situation which should be avoided to prevent spurious switching of inputs and unnecessary power dissipation. Bus-hold is a better solution than the traditional approach of using resistive termination to $V_{CC}$ or GND to prevent bus floating, because the Bus-hold circuit does not consume any static power.



### Figure 4. V-I Characteristics of Bus-hold Circuit

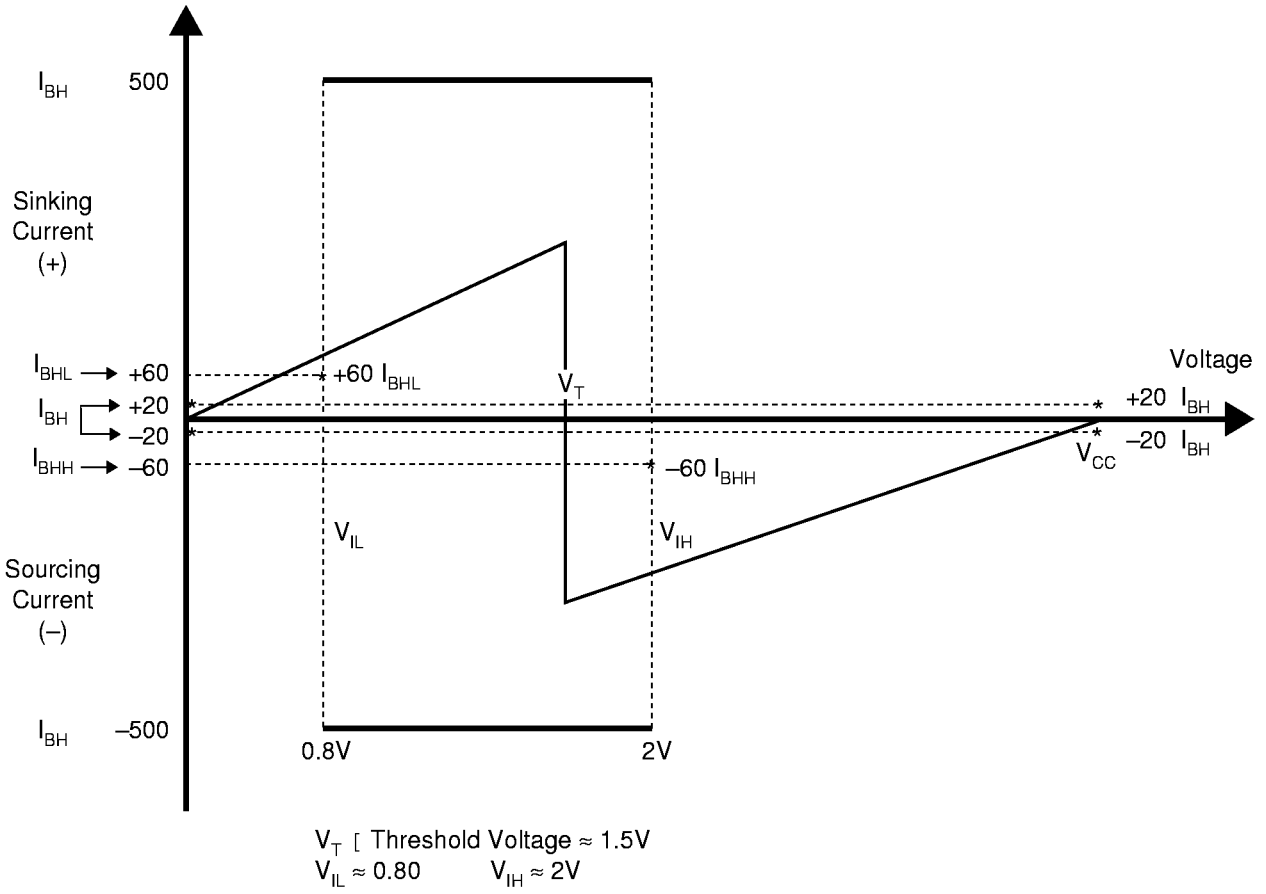
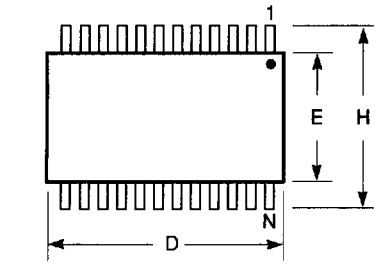


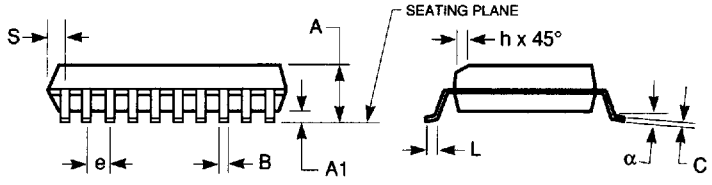

Figure 4 shows the input V-I characteristics of a typical Bus-hold implementation. The input characteristics resemble a resistor. As the input voltage is increased from 0 volts, the input 'sink' current increases linearly. When the TTL threshold of the circuit is reached (typically 1.5 volts), the latch changes the logic state due to positive feedback and the direction of current is reversed. As the input voltage is further increased towards $V_{CC}$, the input 'source' current begins to decrease, reaching the lowest level at $V_{IN} = V_{CC}$.

# 150-MIL QSOP - Package Code Q

**Quarter-Size Outline Package**
**Plastic Small Outline Gull-Wing**

**Notes:**
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006in. per side.
5. Lead coplanarity is 0.004in. maximum.




| JEDEC# | MO-137AB | | | MO-137AD | | | MO-137AE | | | MO-137AF | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DWG# | PSS-16A | | | PSS-20A | | | PSS-24A | | | PSS-28A | | |
| Symbol | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| A | 0.060 | 0.064 | 0.068 | 0.060 | 0.064 | 0.068 | 0.060 | 0.064 | 0.068 | 0.060 | 0.064 | 0.068 |
| A1 | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 | 0.004 | 0.006 | 0.008 |
| B | 0.009 | 0.010 | 0.012 | 0.009 | 0.010 | 0.012 | 0.009 | 0.010 | 0.012 | 0.009 | 0.010 | 0.012 |
| C | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 | 0.007 | 0.008 | 0.010 |
| D | 0.189 | 0.193 | 0.197 | 0.337 | 0.341 | 0.344 | 0.337 | 0.341 | 0.344 | 0.386 | 0.390 | 0.394 |
| E | 0.150 | 0.154 | 0.157 | 0.150 | 0.154 | 0.157 | 0.150 | 0.154 | 0.157 | 0.150 | 0.154 | 0.157 |
| e | 0.025 BSC | | | 0.025 BSC | | | 0.025 BSC | | | 0.025 BSC | | |
| H | 0.230 | 0.236 | 0.244 | 0.230 | 0.236 | 0.244 | 0.230 | 0.236 | 0.244 | 0.230 | 0.236 | 0.244 |
| h | 0.010 | 0.013 | 0.016 | 0.010 | 0.013 | 0.016 | 0.010 | 0.013 | 0.016 | 0.010 | 0.013 | 0.016 |
| L | 0.016 | 0.025 | 0.035 | 0.016 | 0.025 | 0.035 | 0.016 | 0.025 | 0.035 | 0.016 | 0.025 | 0.035 |
| N | 16 | | | 20 | | | 24 | | | 28 | | |
| α | 0° | 5° | 8° | 0° | 5° | 8° | 0° | 5° | 8° | 0° | 5° | 8° |
| S | 0.006 | 0.009 | 0.010 | 0.056 | 0.058 | 0.060 | 0.031 | 0.033 | 0.035 | 0.031 | 0.033 | 0.035 |