PowerNP™ NPe405L Embedded Processor Data Sheet

Features

- IBM PowerPC™ 405 32-bit RISC processor core operating up to 266 MHz
- PC-100 Synchronous DRAM (SDRAM) interface operating up to 133 MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, or 16-bit SRAM and external peripherals
  - Up to 4 banks
- DMA support for external peripherals, internal UARTs and memory
  - Scatter-gather chaining supported
  - Four channels
- 2 Ethernet 10/100 Mbps (full-duplex) units with a choice of MII, RMII, or SMII interfaces.
- HDLC interface with 32 channels through 2 ports
- Programmable Interrupt Controllers supports interrupts from a variety of sources
  - Seven external and 29 internal
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector for faster vector processing
- Programmable Timers
- Two serial ports (16550 compatible UART)
- One IIC (I^2C) interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency

Description

Designed specifically to address embedded applications, the NPe405L provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and intrinsically lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, Ethernet interfaces, HDLC interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS 6SF 0.25 µm (0.18 µm L_{eff})

Package: 324-ball (23 mm) enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 1.1W, Maximum ?.?W

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

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Ordering, PVR, and JTAG Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
NPe405L		200 MHz	23 mm, 324 E-PBGA		0x416100C0	0x????????
NPe405L		200 MHz	23 mm, 324 E-PBGA		0x416100C0	0x????????
NPe405L		266 MHz	23 mm, 324 E-PBGA		0x416100C0	0x????????
NPe405L		266 MHz	23 mm, 324 E-PBGA		0x416100C0	0x????????

Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.

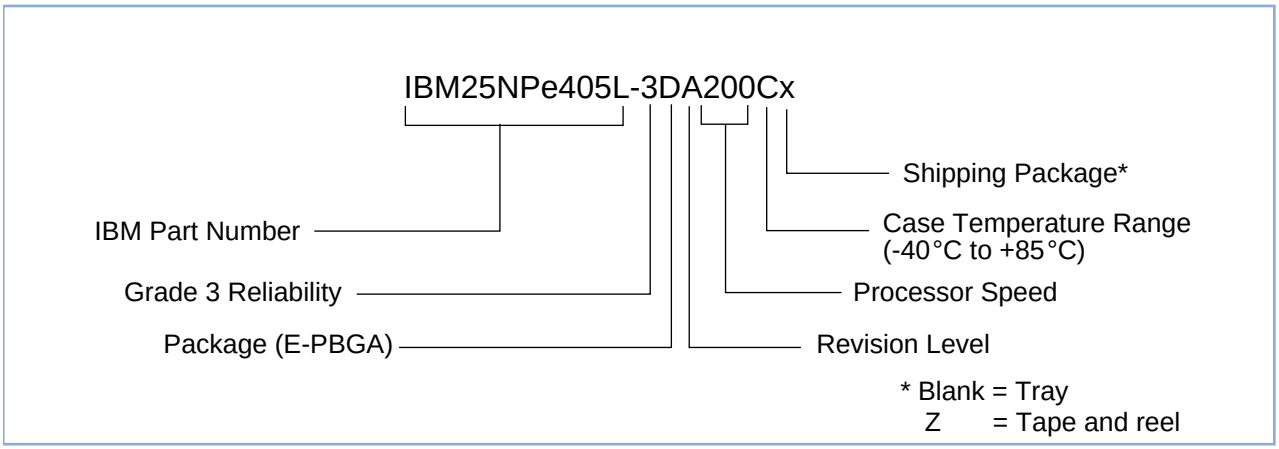
This section provides the part numbering nomenclature for the NPe405L. For availability, contact your local IBM sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the NPe405L User's Manual for details on the register content.

IBM Part Number Key



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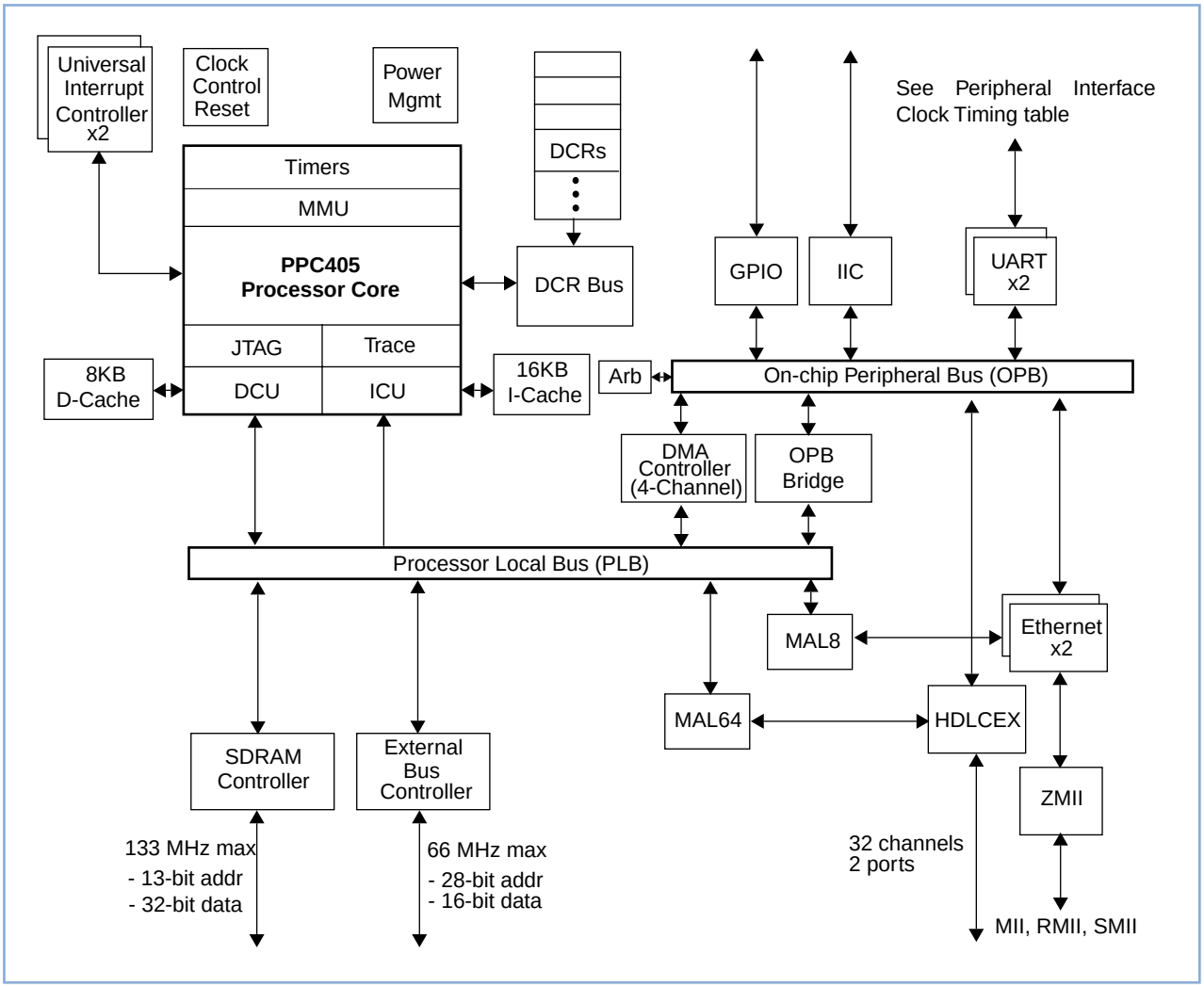
NPe405L Embedded Controller Functional Block Diagram



The NPe405L is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated to create an application-specific ASIC product. This approach provides a consistent way to generate complex ASICs using IBM CoreConnect™ Bus Architecture.

Note: IBM CoreConnect busses provide:

- 64-bit PLB interfaces up to 133MHz
- 32-bit OPB interfaces up to 66MHz

Address Map Support

The NPe405L incorporates two simple and separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCR). This address map is accessed by software running on the NPe405L processor through the use of **mtdcr** and **mfdcr** commands.

SysMem Memory Address Map 4GB System Memory

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals[1]		00000000	7FFFFFFF	2GB
Reserved		80000000	EF5FFFFF	1.74GB
Internal Peripherals	Total	EF600000	EFFFFFFF	10MB
	UART0	EF600300	EF600307	8B
	Reserved	EF600308	EF6003FF	
	UART1	EF600400	EF600407	8B
	Reserved	EF600408	EF6004FF	
	IIC0	EF600500	EF60051F	32B
	Reserved	EF600520	EF6005FF	
	OPB Arbiter	EF600600	EF60063F	64B
	Reserved	EF600640	EF6006FF	
	GPIO Controller Registers	EF600700	EF60077F	128B
	Reserved	EF600780	EF6007FF	
	Ethernet 0 Controller Registers	EF600800	EF6008FF	256B
	Ethernet 1 Controller Registers	EF600900	EF6009FF	256B
	Reserved	EF600A00	EF600C0F	.
	ZMII	EF600C10	EF600C1F	16B
	Reserved	EF600C20	EF60FFFF	
	HDLCEX	EF610000	EF61FFFF	64KB
	Reserved	EF620000	EFFFFFFF	
Expansion ROM[2]		F0000000	FFDFFFFF	254MB
Boot ROM[2,]		FFE00000	FFFFFFFF	2MB

Notes:

1. The Local Memory/Peripheral area of the memory map can be configured for SDRAM, ROM or Peripherals.
2. The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space[1]		000	3FF	1KW (4KB)[1]
Reserved		000	00F	16W
Memory Controller Registers		010	011	2W
External Bus Controller Registers		012	013	2W
Reserved		014	07F	108W
PLB Registers		080	08F	16W
Reserved		090	09F	16W
OPB Bridge Out Registers		0A0	0A7	8W
Reserved		0A8	0AF	8W
Clock, Control and Reset		0B0	0B7	8W
Power Management		0B8	0BF	8W
Interrupt Controller 0		0C0	0CF	16W
Interrupt Controller 1		0D0	0DF	16W
Reserved		0E0	0EF	16W
Miscellaneous		0F0	0FF	16W
DMA Controller Registers		100	13F	64W
Reserved		140	17F	64W
MAL8 Registers (Ethernet)		180	1FF	128W
MAL64 Registers (HDLCEX)		200	27F	128W
Reserved		280	3FF	384W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

SDRAM Memory Controller

The NPe405L Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256 MB per bank are supported, up to a maximum of 1 GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address compare for each bank of memory
  - 4 GB of address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 133 MHz Memory, includes PC133 support
- 4 MB to 256 MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Sync DRAM configuration via mode set command
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging
  - Mixed ECC/non-ECC banks
  - Bypass mode

External Peripheral Bus Controller (EBC)

- Up to four ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 66 MHz operation
- Burst and non-burst devices
- 8-, 16-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous

- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)
- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

UART

- Two 8-pin UART interfaces provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with 16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

HDLCEX Interface

- Multichannel HDLC controller core
- Two full-duplex Pulse Code Modulation (PCM) Highway ports at speeds up to 8 Mbps
- 32 transmit and 32 receive channels
- Supports HDLC protocol as well as a Transparent mode
- One channel per port, autonomous management of the I-Frame and S-Frame of the Normal Response mode (NRM) protocol
- Software emulation of NRM mode

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- Most GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. The GPIO function has 32 I/Os.
- Each GPIO output is separately programmable to emulate an open-drain driver (drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

Two cascaded Universal Interrupt Controllers (UICs) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports 7 external and 29 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

10/100 Mbps Ethernet MAC

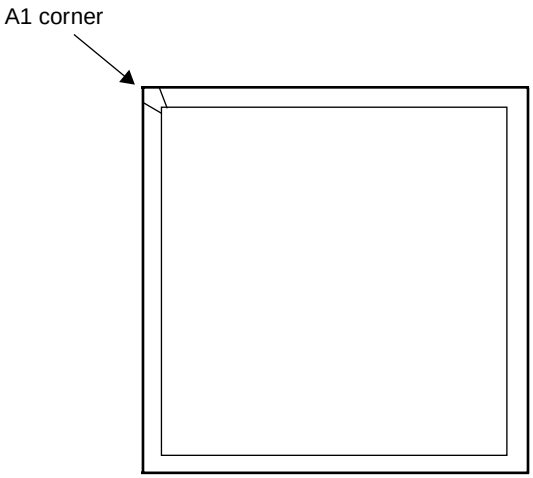
- Two units capable of full- or half-duplex operation at up to 100 Mbps
- ZMII Bridge to external Ethernet PHYs that support
  - Reduced Media Independent Interface (RMII) or Serial Media Independent Interface (SMII) for multiple PHY applications
  - Media Independent Interface (MII) for single PHY applications
- Dedicated DMA channel

JTAG

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

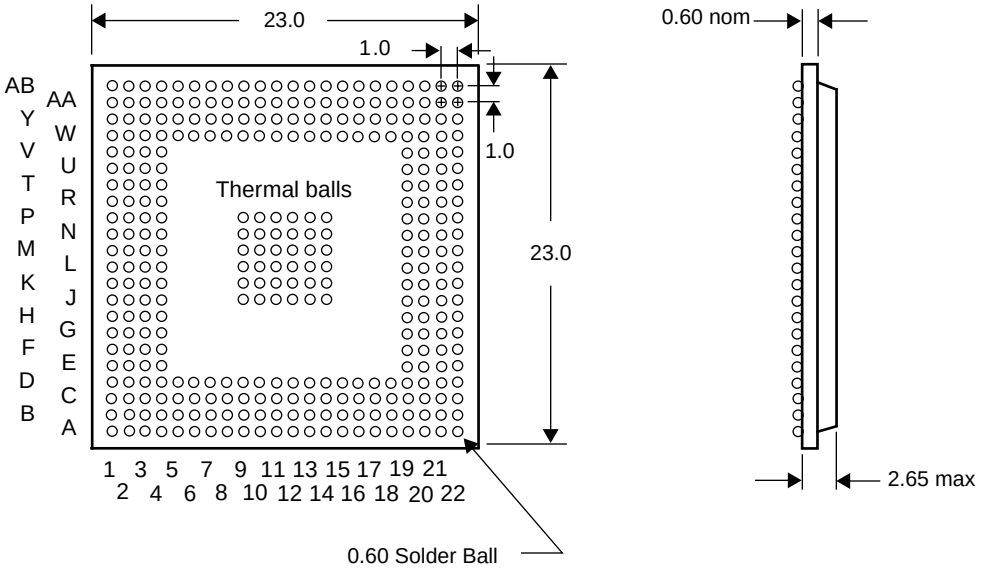
23mm, 324-Ball E-PBGA Package

Top View



Note: All dimensions are in mm.

Bottom View



Pin Lists

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown with the default signal (following reset) *not* in brackets and the alternate signal in brackets. The page number listed gives the page in “Signal Functional Description” on page 28 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 8)

Signal Name	Ball	Interface Group	Page
AV_{DD}	H21	Power	33
BA0 BA1	AB15 Y14	SDRAM	29
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	AA07 Y08 AB06 AA06	SDRAM	29
$\overline{\text{CAS}}$	AA12	SDRAM	29
ClkEn0 ClkEn1	Y13 AA13	SDRAM	29
[$\overline{\text{DMAAck0}}$]GPIO13 [$\overline{\text{DMAAck1}}$]GPIO14 [$\overline{\text{DMAAck2}}$]GPIO15 [$\overline{\text{DMAAck3}}$]GPIO16	U22 U21 T20 D17	External Slave Peripheral	30
[$\overline{\text{DMAReq0}}$]GPIO9 [$\overline{\text{DMAReq1}}$]GPIO10 [$\overline{\text{DMAReq2}}$]GPIO11 [$\overline{\text{DMAReq3}}$]GPIO12	P19 T22 T21 R20	External Slave Peripheral	30
DQM0 DQM1 DQM2 DQM3	U03 U01 R02 L01	SDRAM	29
DQMCB	AA04	SDRAM	29
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	AA05 Y06 AB04 AA03 Y05 AB03 Y04 W06	SDRAM	29
EMC0MDClk	AB16	Ethernet	28
EMC0MDIO	AA16	Ethernet	28
[EMC0Sync]EMC0TxEn[EMC0Tx0En]	AB21	Ethernet	28
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0] EMC0TxD3[EMC0Tx1D1]	AA22 U19 W20 Y22	Ethernet	28
EMC0TxEn[EMC0Tx0En][EMC0Sync]	AB21	Ethernet	28
EMC0TxErr[EMC0Tx1En]	AB20	Ethernet	28
[EMC0Tx0En]EMC0TxEn[EMC0Sync]	AB21	Ethernet	28

Signals Listed Alphabetically (Part 2 of 8)

Signal Name	Ball	Interface Group	Page
[EMC0Tx1En]EMC0TxErr	AB20	Ethernet	28
[$\overline{\text{EOT0}}$][$\overline{\text{TC0}}$]GPIO24 [$\overline{\text{EOT1}}$][$\overline{\text{TC1}}$]GPIO25 [$\overline{\text{EOT2}}$][$\overline{\text{TC2}}$]GPIO26 [$\overline{\text{EOT3}}$][$\overline{\text{TC3}}$]GPIO27	B19 B18 C16 B17	External Slave Peripheral	30
GND	A01 A05 A09 A14 A18 A22 B02 B21 C03 C20 D04 D08 D11 D12 D15 D19 E01 E22 H04 H19 J01 J09-J14 J22 K09-K14 L04 L09-L14 L19 M04 M09-M14 M19 N09-N14 P01 P09-P14 P22 R04 R19 V01 V22 W04 W08 W11 W12 W15 W19 Y03 Y20	Power **Notes:** 1. J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	33

Signals Listed Alphabetically (Part 3 of 8)

Signal Name	Ball	Interface Group	Page
GND	AA02 AA21 AB01 AB05 AB09 AB14 AB18 AB22	Power	33
GPIO0[TrcClk]	B20	System	32
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6]	C18 A20 N20 N22 P21 P20 R22 R21	System	32
GPIO9[$\overline{\text{DMAReq0}}$] GPIO10[$\overline{\text{DMAReq1}}$] GPIO11[$\overline{\text{DMAReq2}}$] GPIO12[$\overline{\text{DMAReq3}}$]	P19 T22 T21 R20	System	32
GPIO13[$\overline{\text{DMAAck0}}$] GPIO14[$\overline{\text{DMAAck1}}$] GPIO15[$\overline{\text{DMAAck2}}$] GPIO16[$\overline{\text{DMAAck3}}$]	U22 U21 T20 D17	System	32
GPIO17[IRQ0] GPIO18[IRQ1] GPIO19[IRQ2] GPIO20[IRQ3] GPIO21[IRQ4] GPIO22[IRQ5] GPIO23[IRQ6]	F20 J20 L21 M21 AA17 AB17 W14	System	32
GPIO24[$\overline{\text{EOT0}}$][$\overline{\text{TC0}}$] GPIO25[$\overline{\text{EOT1}}$][$\overline{\text{TC1}}$] GPIO26[$\overline{\text{EOT2}}$][$\overline{\text{TC2}}$] GPIO27[$\overline{\text{EOT3}}$][$\overline{\text{TC3}}$]	B19 B18 C16 B17	System	32
GPIO28[$\overline{\text{UART1\_DCD}}$][HDLCEXTxEnA] GPIO29[$\overline{\text{UART1\_RI}}$][HDLCEXTxEnB]	AA15 T01	System	32
GPIO30 GPIO31[$\overline{\text{PerWE}}$]	T03 A13	System	32
$\overline{\text{Halt}}$	F22	System	32
HDLCEXRxClk	L20	HDLC 32-Channel	28
HDLCEXRxDataA HDLCEXRxDataB	M22 N21	HDLC 32-Channel	28
HDLCEXRxFS	M20	HDLC 32-Channel	28
HDLCEXTxClk	K20	HDLC 32-Channel	28
HDLCEXTxDataA HDLCEXTxDataB	K21 L22	HDLC 32-Channel	28
[HDLCEXTxEnA]GPIO28[$\overline{\text{UART1\_DCD}}$] [HDLCEXTxEnB]GPIO29[$\overline{\text{UART1\_RI}}$]	AA15 T01	HDLC 32-Channel	

Signals Listed Alphabetically (Part 4 of 8)

Signal Name	Ball	Interface Group	Page
HDLCEXTxFS	K22	HDLC 32-Channe	28
IICSCL[IECSCL] IICSDA[IECSDA]	C17 A19	Internal Peripheral	31
[IRQ0]GPIO17 [IRQ1]GPIO18 [IRQ2]GPIO19 [IRQ3[GPIO20 [IRQ4[GPIO21 [IRQ5]GPIO22 [IRQ6[GPIO23	F20 J20 L21 M21 AA17 AB17 W14	Interrupts	32
MemAddr0 MemAddr1 MemAddr2 MemAddr3 MemAddr4 MemAddr5 MemAddr6 MemAddr7 MemAddr8 MemAddr9 MemAddr10 MemAddr11 MemAddr12	Y12 Y11 AB11 AA11 AA10 Y10 AB10 AA09 Y09 AB08 AA08 W09 AB07	SDRAM	29
MemClkOut0 MemClkOut1	AA14 AB13	SDRAM	29

Signals Listed Alphabetically (Part 5 of 8)

Signal Name	Ball	Interface Group	Page
MemData0	AB02		
MemData1	AA01		
MemData2	U04		
MemData3	W03		
MemData4	Y01		
MemData5	V03		
MemData6	Y02		
MemData7	W01		
MemData8	W02		
MemData9	V02		
MemData10	U02		
MemData11	R03		
MemData12	T02		
MemData13	P04		
MemData14	R01	SDRAM	
MemData15	P03	**Notes:**	
MemData16	P02	1. MemData00 is the most significant bit (msb).	29
MemData17	N01	2. MemData31 is the least significant bit (lsb)	
MemData18	N03		
MemData19	N02		
MemData20	M02		
MemData21	M01		
MemData22	M03		
MemData23	L03		
MemData24	L02		
MemData25	K02		
MemData26	K03		
MemData27	K01		
MemData28	J02		
MemData29	J03		
MemData30	H01		
MemData31	H02		
OV_{DD}	D05 D07 D16 D18 E04 E19 G04 G19 T19 T04 V04 V19 W05 W07 W16 W18	Power	33

Signals Listed Alphabetically (Part 6 of 8)

Signal Name	Ball	Interface Group	Page
PerAddr4	D06	External Slave Peripheral	30
PerAddr5	C04		
PerAddr6	A03		
PerAddr7	C05		
PerAddr8	B03		
PerAddr9	A04		
PerAddr10	C06		
PerAddr11	B04		
PerAddr12	B05		
PerAddr13	C07		
PerAddr14	B06		
PerAddr15	C08		
PerAddr16	B07		
PerAddr17	A07		
PerAddr18	D09		
PerAddr19	B08		
PerAddr20	A08		
PerAddr21	C09		
PerAddr22	B09		
PerAddr23	A10		
PerAddr24	C10		
PerAddr25	B10		
PerAddr26	B11		
PerAddr27	A11		
PerAddr28	C11		
PerAddr29	C12		
PerAddr30	A12		
PerAddr31	B12		
$\overline{\text{PerBLast}}$	C15	External Slave Peripheral	30
PerClk	A17	External Slave Peripheral	30
$\overline{\text{PerCS0}}$	B14	External Slave Peripheral	30
$\overline{\text{PerCS1}}$	C14		
$\overline{\text{PerCS2}}$	A15		
$\overline{\text{PerCS3}}$	B15		
PerData0	J04	External Slave Peripheral **Note:** PerData00 is the most significant bit (msb) on this bus.	30
PerData1	G01		
PerData2	G02		
PerData3	H03		
PerData4	F01		
PerData5	F02		
PerData6	G03		
PerData7	E02		
PerData8	D02		
PerData9	F03		
PerData10	D01		
PerData11	C02		
PerData12	E03		
PerData13	C01		
PerData14	D03		
PerData15	F04		
PerErr	J21	External Slave Peripheral	30
$\overline{\text{PerOE}}$	D14	External Slave Peripheral	30

Signals Listed Alphabetically (Part 7 of 8)

Signal Name	Ball	Interface Group	Page
PerPar0 PerPar1	B01 A02	External Slave Peripheral	30
PerR/$\overline{W}$	A16	External Slave Peripheral	30
PerReady	B16	External Slave Peripheral	30
$\overline{PerWBE0}$ $\overline{PerWBE1}$	B13 C13	External Slave Peripheral	30
[$\overline{PerWE}$]GPIO31	A13	External Slave Peripheral	30
PHY0Col[PHY0Rx1Er]	W17	Ethernet	28
PHY0CrS[PHY0CrS0DV]	Y18	Ethernet	28
[PHY0CrS1DV]PHY0RxDV	Y17	Ethernet	28
PHY0RxClk	AB19	Ethernet	28
[PHY0RefClk]PHY0TxClk	Y19	Ethernet	28
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D] PHY0RxD1[PHY0Rx0D1][PHY0Rx1D] PHY0RxD2[PHY0Rx1D0] PHY0RxD3[PHY0Rx1D1]	Y15 Y16 AA18 AA19	Ethernet	28
PHY0RxDV[PHY0CrS1DV]	Y17	Ethernet	28
PHY0RxErr[PHY0Rx0Er]	AA20	Ethernet	28
[PHY0Rx0Er]PHY0RxErr	AA20	Ethernet	28
PHY0TxClk[PHY0RefClk]	Y19	Ethernet	28
$\overline{RAS}$	AB12	SDRAM	29
Reserved		Other	33
SysClk	G22	System	32
SysErr	C21	System	32
$\overline{SysReset}$	A21	System	32
TCK	J19	JTAG	32
[$\overline{TC0}$][$\overline{EOT0}$]GPIO24 [$\overline{TC1}$][$\overline{EOT1}$]GPIO25 [$\overline{TC2}$][$\overline{EOT2}$]GPIO26 [$\overline{TC3}$][$\overline{EOT3}$]GPIO27	B19 B18 C16 B17	External Slave Peripheral	30
TDI	G21	JTAG	32
TDO	F21	JTAG	32
TestEn	H20	System	32
TmrClk	D20	System	32
TMS	E21	JTAG	32
[TrcClk]GPIO0	B20	Trace	33
$\overline{TRST}$	H22	JTAG	32
[TS1E]GPIO1 [TS2E]GPIO2 [TS1O]GPIO3 [TS2O]GPIO4 [TS3]GPIO5 [TS4]GPIO6 [TS5]GPIO7 [TS6]GPIO8	C18 A20 N20 N22 P21 P20 R22 R21	Trace	33

Signals Listed Alphabetically (Part 8 of 8)

Signal Name	Ball	Interface Group	Page
$\overline{\text{UART0\_CTS}}$	B22	Internal Peripheral	31
$\overline{\text{UART0\_DCD}}$	C19		
$\overline{\text{UART0\_DSR}}$	A06		
$\overline{\text{UART0\_DTR}}$	G20		
$\overline{\text{UART0\_RI}}$	D22		
$\overline{\text{UART0\_RTS}}$	D21		
UART0_Rx	C22		
UART0_Tx	F19		
$\overline{\text{UART1\_CTS}}$	W22	Internal Peripheral	31
[$\overline{\text{UART1\_DCD}}$]GPIO28[HDLCEXTxEnA]	AA15		
$\overline{\text{UART1\_DSR}}$	W21		
$\overline{\text{UART1\_DTR}}$	U20		
[$\overline{\text{UART1\_RI}}$]GPIO29[HDLCEXTxEnB]	T01		
$\overline{\text{UART1\_RTS}}$	V21		
UART1_Rx	V20		
UART1_Tx	Y21		
UARTSerClk	E20	Internal Peripheral	31
V_{DD}	D10 D13 K19 K04 N19 N04 W10 W13	Power	33
$\overline{\text{WE}}$	Y07	SDRAM	29

Signals Listed by Ball Assignment (Part 1 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A01	GND	B01	PerPar0	C01	PerData13	D01	PerData10
A02	PerPar1	B02	GND	C02	PerData11	D02	PerData8
A03	PerAddr6	B03	PerAddr8	C03	GND	D03	PerData14
A04	PerAddr9	B04	PerAddr11	C04	PerAddr5	D04	GND
A05	GND	B05	PerAddr12	C05	PerAdd7	D05	OV_{DD}
A06	$\overline{\text{UART0\_DSR}}$	B06	PerAddr14	C06	PerAddr10	D06	PerAddr4
A07	PerAddr17	B07	PerAddr16	C07	PerAddr13	D07	OV_{DD}
A08	PerAddr20	B08	PerAddr19	C08	PerAddr15	D08	GND
A09	GND	B09	PerAddr22	C09	PerAddr21	D09	PerAddr18
A10	PerAddr23	B10	PerAddr25	C10	PerAddr24	D10	V_{DD}
A11	PerAddr27	B11	PerAddr26	C11	PerAddr28	D11	GND
A12	PerAddr30	B12	PerAddr31	C12	PerAddr29	D12	GND
A13	GPIO31[$\overline{\text{PerWE}}$]	B13	$\overline{\text{PerWBE0}}$	C13	$\overline{\text{PerWBE1}}$	D13	V_{DD}
A14	GND	B14	$\overline{\text{PerCS0}}$	C14	$\overline{\text{PerCS1}}$	D14	$\overline{\text{PerOE}}$
A15	$\overline{\text{PerCS2}}$	B15	$\overline{\text{PerCS3}}$	C15	$\overline{\text{PerBLas}}$	D15	GND
A16	PerR/$\overline{\text{W}}$	B16	PerReady	C16	GPIO26[$\overline{\text{EOT2}}$][$\overline{\text{TC2}}$]	D16	OV_{DD}
A17	PerClk	B17	GPIO27[$\overline{\text{EOT3}}$][$\overline{\text{TC3}}$]	C17	IICSCL[IECSCL]	D17	GPIO16[$\overline{\text{DMAAck3}}$]
A18	GND	B18	GPIO25[$\overline{\text{EOT1}}$][$\overline{\text{TC1}}$]	C18	GPIO1[TS1E]	D18	OV_{DD}
A19	IICSDA[IECSDA]	B19	GPIO24[$\overline{\text{EOT0}}$][$\overline{\text{TC0}}$]	C19	$\overline{\text{UART0\_DCD}}$	D19	GND
A20	GPIO2[TS2E]	B20	GPIO0	C20	GND	D20	TmrClk
A21	$\overline{\text{SysReset}}$	B21	GND	C21	SysErr	D21	$\overline{\text{UART0\_RTS}}$
A22	GND	B22	$\overline{\text{UART0\_CTS}}$	C22	UART0_Rx	D22	$\overline{\text{UART0\_RI}}$

Signals Listed by Ball Assignment (Part 2 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
E01	GND	F01	PerData4	G01	PerData1	H01	MemData30
E02	PerData7	F02	PerData5	G02	PerData2	H02	MemData31
E03	PerData12	F03	PerData9	G03	PerData6	H03	PerData3
E04	OV_{DD}	F04	PerData15	G04	OV_{DD}	H04	GND
E05	No ball	F05	No ball	G05	No ball	H05	No ball
E06	No ball	F06	No ball	G06	No ball	H06	No ball
E07	No ball	F07	No ball	G07	No ball	H07	No ball
E08	No ball	F08	No ball	G08	No ball	H08	No ball
E09	No ball	F09	No ball	G09	No ball	H09	No ball
E10	No ball	F10	No ball	G10	No ball	H10	No ball
E11	No ball	F11	No ball	G11	No ball	H11	No ball
E12	No ball	F12	No ball	G12	No ball	H12	No ball
E13	No ball	F13	No ball	G13	No ball	H13	No ball
E14	No ball	F14	No ball	G14	No ball	H14	No ball
E15	No ball	F15	No ball	G15	No ball	H15	No ball
E16	No ball	F16	No ball	G16	No ball	H16	No ball
E17	No ball	F17	No ball	G17	No ball	H17	No ball
E18	No ball	F18	No ball	G18	No ball	H18	No ball
E19	OV_{DD}	F19	UART0_Tx	G19	OV_{DD}	H19	GND
E20	UARTSerClk	F20	GPIO17[IRQ0]	G20	$\overline{\text{UART0\_DTR}}$	H20	TestEn
E21	TMS	F21	TDO	G21	TDI	H21	AV_{DD}
E22	GND	F22	$\overline{\text{Halt}}$	G22	SysClk	H22	$\overline{\text{TRST}}$

Signals Listed by Ball Assignment (Part 3 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J01	GND	K01	MemData27	L01	DQM3	M01	MemData21
J02	MemData28	K02	MemData25	L02	MemData24	M02	MemData20
J03	MemData29	K03	MemData26	L03	MemData23	M03	MemData22
J04	PerData0	K04	V_{DD}	L04	GND	M04	GND
J05		K05	No ball	L05	No ball	M05	No ball
J06		K06	No ball	L06	No ball	M06	No ball
J07		K07	No ball	L07	No ball	M07	No ball
J08		K08	No ball	L08	No ball	M08	No ball
J09	GND	K09	GND	L09	GND	M09	GND
J10	GND	K10	GND	L10	GND	M10	GND
J11	GND	K11	GND	L11	GND	M11	GND
J12	GND	K12	GND	L12	GND	M12	GND
J13	GND	K13	GND	L13	GND	M13	GND
J14	GND	K14	GND	L14	GND	M14	GND
J15		K15	No ball	L15	No ball	M15	No ball
J16		K16	No ball	L16	No ball	M16	No ball
J17		K17	No ball	L17	No ball	M17	No ball
J18		K18	No ball	L18	No ball	M18	No ball
J19	TCK	K19	V_{DD}	L19	GND	M19	GND
J20	GPIO18[IRQ1]	K20	HDLCEXTxClk	L20	HDLCEXRxClk	M20	HDLCEXRxFS
J21	PerErr	K21	HDLCEXTxDataA	L21	GPIO19[IRQ2]	M21	GPIO20[IRQ3]
J22	GND	K22	HDLCEXTxFS	L22	HDLCEXTxDataB	M22	HDLCEXRxDataA

Signals Listed by Ball Assignment (Part 4 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
N01	MemData17	P01	GND	R01	MemData14	T01	GPIO29[$\overline{\text{UART1\_RI}}$] [HDLCEXTxEnB]
N02	MemData19	P02	MemData16	R02	DQM2	T02	MemData12
N03	MemData18	P03	MemData15	R03	MemData11	T03	GPIO30
N04	V_{DD}	P04	MemData13	R04	GND	T04	OV_{DD}
N05	No ball	P05	No ball	R05	No ball	T05	No ball
N06	No ball	P06	No ball	R06	No ball	T06	No ball
N07	No ball	P07	No ball	R07	No ball	T07	No ball
N08	No ball	P08	No ball	R08	No ball	T08	No ball
N09	GND	P09	GND	R09	No ball	T09	No ball
N10	GND	P10	GND	R10	No ball	T10	No ball
N11	GND	P11	GND	R11	No ball	T11	No ball
N12	GND	P12	GND	R12	No ball	T12	No ball
N13	GND	P13	GND	R13	No ball	T13	No ball
N14	GND	P14	GND	R14	No ball	T14	No ball
N15	No ball	P15	No ball	R15	No ball	T15	No ball
N16	No ball	P16	No ball	R16	No ball	T16	No ball
N17	No ball	P17	No ball	R17	No ball	T17	No ball
N18	No ball	P18	No ball	R18	No ball	T18	No ball
N19	V_{DD}	P19	GPIO9[$\overline{\text{DMAReq0}}$]	R19	GND	T19	OV_{DD}
N20	GPIO3[TS1O]	P20	GPIO6[TS4]	R20	GPIO12[$\overline{\text{DMAReq3}}$]	T20	GPIO15[$\overline{\text{DMAAck2}}$]
N21	HDLCEXRxDataB	P21	GPIO5[TS3]	R21	GPIO8[TS6]	T21	GPIO11[$\overline{\text{DMAReq2}}$]
N22	GPIO4[TS2O]	P22	GND	R22	GPIO7[TS5]	T22	GPIO10[$\overline{\text{DMAReq1}}$]

Signals Listed by Ball Assignment (Part 5 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
U01	DQM1	V01	GND	W01	MemData7	Y01	MemData4
U02	MemData10	V02	MemData9	W02	MemData8	Y02	MemData6
U03	DQM0	V03	MemData5	W03	MemData3	Y03	GND
U04	MemData2	V04	OV_{DD}	W04	GND	Y04	ECC6
U05	No ball	V05	No ball	W05	OV_{DD}	Y05	ECC4
U06	No ball	V06	No ball	W06	ECC7	Y06	ECC1
U07	No ball	V07	No ball	W07	OV_{DD}	Y07	$\overline{WE}$
U08	No ball	V08	No ball	W08	GND	Y08	$\overline{BankSel1}$
U09	No ball	V09	No ball	W09	MemAddr11	Y09	MemAddr8
U10	No ball	V10	No ball	W10	V_{DD}	Y10	MemAddr5
U11	No ball	V11	No ball	W11	GND	Y11	MemAddr1
U12	No ball	V12	No ball	W12	GND	Y12	MemAddr0
U13	No ball	V13	No ball	W13	V_{DD}	Y13	ClkEn0
U14	No ball	V14	No ball	W14	GPIO23[IRQ6]	Y14	BA1
U15	No ball	V15	No ball	W15	GND	Y15	PHY0RxD0 [PHY0Rx0D0] [PHY0Rx0D]
U16	No ball	V16	No ball	W16	OV_{DD}	Y16	PHYRxD1 [PHY0Rx0D1] [PHY0Rx1D]
U17	No ball	V17	No ball	W17	PHY0Col[PHY0Rx1Er]	Y17	PHY0RxDV [PHY0CrS1DV]
U18	No ball	V18	No ball	W18	OV_{DD}	Y18	PHY0CrS [PHY0CrS0DV]
U19	EMC0TxD1 [EMC0Tx0D1] [EMC0Tx1D]	V19	OV_{DD}	W19	GND	Y19	PHY0TxClk [PHY0RefClk]
U20	$\overline{UART1\_DTR}$	V20	UART1_Rx	W20	EMC0TxD2 [EMC0Tx1D0]	Y20	GND
U21	GPIO14[$\overline{DMAAck1}$]	V21	$\overline{UART1\_RTS}$	W21	$\overline{UART1\_DSR}$	Y21	UART1_Tx
U22	GPIO13[$\overline{DMAAck0}$]	V22	GND	W22	$\overline{UART1\_CTS}$	Y22	EMC0TxD3 [EMC0Tx1D1]

Signals Listed by Ball Assignment (Part 6 of 6)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA01	MemData1	AB01	GND				
AA02	GND	AB02	MemData0				
AA03	ECC3	AB03	ECC5				
AA04	DQMCB	AB04	ECC2				
AA05	ECC0	AB05	GND				
AA06	$\overline{\text{BankSel3}}$	AB06	$\overline{\text{BankSel2}}$				
AA07	$\overline{\text{BankSel0}}$	AB07	MemAddr12				
AA08	MemAddr10	AB08	MemAddr9				
AA09	MemAddr7	AB09	GND				
AA10	MemAddr4	AB10	MemAddr6				
AA11	MemAddr3	AB11	MemAddr2				
AA12	$\overline{\text{CAS}}$	AB12	$\overline{\text{RAS}}$				
AA13	ClkEn1	AB13	MemClkOut1				
AA14	MemClkOut0	AB14	GND				
AA15	GPIO28[$\overline{\text{UART1\_DCD}}$] [HDLCEXTxEnA]	AB15	BA0				
AA16	EMC0MDIO	AB16	EMC0MDClk				
AA17	GPIO21[IRQ4]	AB17	GPIO22[IRQ5]				
AA18	PHY0RxD2 [PHY0Rx1D0]	AB18	GND				
AA19	PHY0RxD3 [PHY0Rx1D1]	AB19	PHY0RxClk				
AA20	PHY0RxErr [PHY0Rx0Er]	AB20	EMC0TxErr [EMC0Tx1En]				
AA21	GND	AB21	EMC0TxEn [EMC0Tx0En] [EMC0Sync]				
AA22	EMC0TxD0 [EMC0Tx0D0] [EMC0Tx0D]	AB22	GND				

Signal List

The table following table provides a summary of the number of package pins associated with each functional interface group.

Pin Summary

Group	No. of Pins
Nonmultiplexed Signals	167
Multiplexed Signals	48
Total Signal Pins	**215**
AV_{DD}	1
OV_{DD}	16
V_{DD}	8
Gnd	48
Thermal (and Gnd)	36
Reserved	0
Total Pins	**324**

In the table “Signal Functional Description” on page 28, each external signal is listed along with a short description of the signal function. The signals are grouped together according to their function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. In most cases, the signal name is shown in this table without any multiplexed signal names that may be associated with it. In cases where multiplexed signals are in the same functional group, the names appear as a default signal followed by secondary signals in square brackets (for example, PCIC0:3[$\overline{BE0:3}$]). Active-low signals such as $\overline{BE0:3}$ are marked with an overline. Any signal that is not the primary (default) signal on a multiplexed pin is shown in square backets.

The active signal on a multiplexed pin is controlled by programming. It is expected that in any single application, a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, EMC0TxErr[EMC0Tx1En] functions as an error output when the Ethernet interface operates in MII mode, or as a transmit enable output when operating in RMII mode.

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Initialization” on page 47). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

The following table lists all of the I/O signals provided by the NPe405L. Please refer to “Signals Listed Alphabetically” on page 13 for the pin number to which each signal is assigned.

Signal Functional Description (Part 1 of 6)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
HDLCEX Interface				
HDLCEXTxClk	Transmit Clock	I	3.3V LVTTL	
HDLCEXTxFS	Transmit Frame Synchronization	I	3.3V LVTTL	
HDLCEXTxDataA	Transmit Data port A	O	3.3V LVTTL	
HDLCEXTxDataB	Transmit Data port B	O	3.3V LVTTL	
HDLCEXRxClk	Receive Clock	I	3.3V LVTTL	
HDLCEXRxFS	Receive Frame Synchronization	I	3.3V LVTTL	
HDLCEXRxDataA	Receive Data port A	I	3.3V LVTTL	
HDLCEXRxDataB	Receive Data port B	I	3.3V LVTTL	
[HDLCEXTxEnA]	Transmit Enable port A	O	5V tolerant 3.3V LVTTL	
[HDLCEXTxEnB]	Transmit Enable port B	O	5V tolerant 3.3V LVTTL	
Ethernet Interface				
EMC0MDClk	Management Data Clock. The MDClk is sourced to the PHY. Management information is transferred synchronously with respect to this clock (MII, RMII, and SMII).	O	5V tolerant 3.3V LVTTL	
EMC0MDIO	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information (MII, RMII, and SMII).	I/O	5V tolerant 3.3V LVTTL	1, 4
EMC0TxD0[EMC0Tx0D0][EMC0Tx0D] EMC0TxD1[EMC0Tx0D1][EMC0Tx1D] EMC0TxD2[EMC0Tx1D0] EMC0TxD3[EMC0Tx1D1]	Transmit Data. A nibble wide data bus towards the net. The data is synchronous with PHY0TxClk (MII 0[RMII 0 and 1][SMII 0, 1, 2, and 3]).	O	3.3V LVTTL	
EMC0TxEn[EMC0Tx0En][EMC0Sync]	Transmit Enable. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous with PHYTxClk (MII 0[RMII 0]). or SMII Sync.	O	3.3V LVTTL	
EMC0TxErr[EMC0Tx1En]	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHY0TxClk. It informs the PHY that an error was detected (MII 0). or Transmit Enable [RMII 1].	O	5V tolerant 3.3V LVTTL	

Signal Functional Description (Part 2 of 6)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PHY0Col[PHY0Rx1Er]l	Collision [receive error] signal from the PHY. This is an asynchronous signal (MII 0). or Receive Error ([RMII 1]).	I	5V tolerant 3.3V LVTTL	
PHY0CrS[PHY0CrS0DV]	Carrier Sense signal from the PHY. This is an asynchronous signal (MII 0). or Carrier sense data valid ([RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxClk	Receiver medium clock. This signal is generated by the PHY (MII 0).	I	5V tolerant 3.3V LVTTL	1, 4
PHY0RxD0[PHY0Rx0D0][PHY0Rx0D] PHY0RxD1[PHY0Rx0D1][PHY0Rx1D] PHY0RxD2[PHY0Rx1D0] PHY0RxD3[PHY0Rx1D1]	Received Data. This is a nibble wide bus from the PHY. The data is synchronous with PHY0RxClk (MII 0[RMII 0 and 1][SMII 0, 1, 2, and 3]).	I	5V tolerant 3.3V LVTTL	1, 4
PHY0RxDV[PHY0CrS1DV]	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception (MII 0). or Carrier sense data valid ([RMII 1])	I	5V tolerant 3.3V LVTTL	1, 5
PHY0RxErr[PHY0Rx0Er]	Receive Error. This signal comes from the PHY and is synchronous with PHY0RxClk (MII 0 [RMII 0]).	I	5V tolerant 3.3V LVTTL	1, 5
PHY0TxClk[PHY0RefClk]	Transmit medium clock. This signal is generated the PHY ([MII 0]). or Reference Clock [RMII and SMII].	I	5V tolerant 3V LVTTL	1, 4
SDRAM Interface				
MemData0:31	Memory Data bus **Notes:** 1. MemData0 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	4
MemAddr12:0	Memory Address bus. **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr0 is the least significant bit (lsb).	O	3.3V LVTTL	
BA1:0	Bank Address supporting up to 4 internal banks	O	3.3V LVTTL	
$\overline{RAS}$	Row Address Strobe.	O	3.3V LVTTL	
$\overline{CAS}$	Column Address Strobe.	O	3.3V LVTTL	
DQM0:3	DQM for byte lanes 0 (MemData0:7), 1 (MemData8:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits.	O	3.3V LVTTL	
ECC0:7	ECC check bits 0:7.	I/O	3.3V LVTTL	4

Signal Functional Description (Part 3 of 6)

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{BankSel0:3}}$	Select up to four external SDRAM banks.	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable.	O	3.3V LVTTL	
ClkEn0:1	SDRAM Clock Enable.	O	3.3V LVTTL	
MemClkOut0:1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attachment without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	
External Slave Peripheral Interface				
PerData0:15	Peripheral data bus used by NPe405L. **Note:** PerData00 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerAddr4:31	Peripheral Address bus used by NPe405L.	O	5V tolerant 3.3V LVTTL	
PerPar0:1	Peripheral byte parity signals.	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0:1}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or DMA controller depending upon the type of transfer involved.	O	5V tolerant 3.3V LVTTL	2
$\overline{\text{PerWE}}$	Peripheral Write Enable. Low when any of the two $\overline{\text{PerWBE}}$ signals are low.	I/O	5V tolerant 3.3V LVTTL	
[$\overline{\text{PerCS0:3}}$]	Peripheral Chip Selects	O	5V tolerant 3.3V LVTTL	2
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the NPe405L is the bus master, it enables the selected SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2
PerR/$\overline{\text{W}}$	Used by the NPe405L as an output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory.	O	5V tolerant 3.3V LVTTL	
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerBLast}}$	Used by the NPe405L to indicate the last transfer of a memory access.	O	5V tolerant 3.3V LVTTL	4
PerClk	Peripheral Clock to be used by synchronous peripheral slaves.	O	5V tolerant 3.3V LVTTL	
PerErr	Used as an input to record external slave peripheral errors.	I	5V tolerant 3.3V LVTTL	1, 5
[$\overline{\text{DMAReq0:3}}$]	Used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 4 of 6)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
[$\overline{\text{DMAAck0:3}}$]	Used by the NPe405L to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{EOT0:3}}$][$\overline{\text{TC0:3}}$]	End Of Transfer[Terminal Count].	I/O	5V tolerant 3.3V LVTTL	1, 5
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either or both UART0 and UART1.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Transmit data.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_DCD}}$]	UART0 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_DSR}}$]	UART0 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_CTS}}$]	UART0 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART0\_DTR}}$]	UART0 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RTS}}$]	UART0 Request To Send.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART0\_RI}}$]	UART0 Ring Indicator.	I	5V tolerant 3.3V LVTTL r	1, 4
UART1_Rx	UART1 Receive data.	I	5V tolerant 3.3V LVTTL	1, 4
UART1_Tx	UART1 Transmit data.	O	5V tolerant 3.3V LVTTL	
[$\overline{\text{UART1\_DCD}}$]	UART1 Data Carrier Detect.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DSR}}$]	UART1 Data Set Ready.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_CTS}}$]	UART1 Clear To Send.	I	5V tolerant 3.3V LVTTL	1, 4
[$\overline{\text{UART1\_DTR}}$]	UART1 Data Terminal Ready.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART1\_RTS}}$]	UART1 Request To Send.	O	5V tolerant 3.3V LVTTL	6
[$\overline{\text{UART1\_RI}}$]	UART1 Ring Indicator.	I	5V tolerant 3.3V LVTTL	1, 4

Signal Functional Description (Part 5 of 6)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
IICSCL	IIC Serial Clock.	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA	IIC Serial Data.	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
[IRQ0:6]	Interrupt Requests.	I	5V tolerant 3.3V LVTTL	1, 5
JTAG Interface				
TDI	Test Data In.	I	5V tolerant 3.3V LVTTL	1, 4
TMS	Test Mode Select.	I	5V tolerant 3.3V LVTTL	1, 4
TDO	Test Data Out.	O	5V tolerant 3.3V LVTTL	
TCK	Test Clock.	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TRST}}$	Test Reset.	I	5V tolerant 3.3V LVTTL	2, 5
System Interface				
SysClk	Main System Clock input.	I	3.3V Analog Wire w/ESD	
$\overline{\text{SysReset}}$	Main System Reset.	I/O	5V tolerant 3.3V LVTTL	1, 2
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL	1, 4
GPIO0	General Purpose I/O. To access this function, software must toggle a DCR bit.	I/O	5V tolerant 3.3V LVTTL	1, 6
GPIO1:31	General Purpose I/O. To access this function, software must toggle a DCR bit.	I/O	5V tolerant 3.3V LVTTL	1
TestEn	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	3.3V LVTTL Rcvr w/ PD	3
TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range).	I	5V tolerant 3.3V LVTTL	1, 4

Signal Functional Description (Part 6 of 6)

Notes:
1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Trace Interface				
[TS1E] [TS2E]	Even Trace execution status.To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS1O] [TS2O]	Odd Trace execution status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TS3:6]	Trace Status. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	
[TrcClk]	Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR bit.	O	5V tolerant 3.3V LVTTL	1, 6
Power Pins				
GND	Ground **Note:** J09-J14, K09-K14, L09-L14, M09-M14, N09-N14, and P09-P14 are also thermal balls.	I	Hardwire	
V_{DD}	Logic voltage—2.5V	I	Hardwire	
OV_{DD}	Output driver voltage—3.3V	I	Hardwire	
AV_{DD}	Filtered PLL voltage—2.5V	I	3.3V DC Wire w/ESD	
Other Pins				
Reserved	Do not connect signals, voltage, or ground to these pins.	n/a	n/a	

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.7	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6	V
PLL Supply Voltage	AV_{DD}	0 to 2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to 5.5	V
Storage Temperature Range	T_{STG}	-55 to 150	°C
Case temperature under bias	T_C	-40 to +120	°C

Package Thermal Specifications

The NPe405L is designed to operate within a case temperature range of -40˚C to 120˚C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
23mm, 324-balls—Junction-to-Case	θ_{JC}				°C/W
23mm, 324-balls—Case-to-Ambient[1]	θ_{CA}				°C/W

Notes:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	2.3	2.5	2.7	V	
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	
PLL Supply Voltage	AV_{DD}	2.3	2.5	2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		400 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–250 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Capacitance

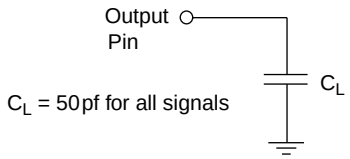
Parameter	Symbol	Maximum	Unit	Notes
Input Capacitance Group 1 (3.3V LVTTL //O)	C_{IN1}	2.5	pF	
Input Capacitance Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	3.5	pF	
Input Capacitance Group 1 (RX only pins)	C_{IN4}	0.75	pF	

DC Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})	I_{DD}		390	600	mA
Active Operating Current (OV_{DD})	I_{ODD}		35	100	mA
PLL Voltage (AV_{DD})	V_{PLL}	2.3	2.5	2.7	V
PLL V_{DD} Input current	I_{PLL}		16	23	mA

Test Conditions

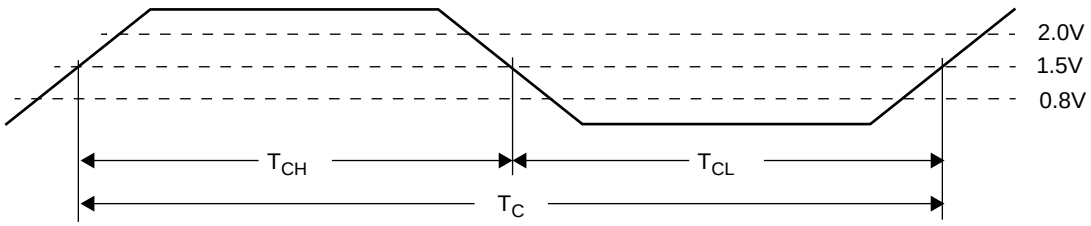
Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at V_{DD} = 3.14V and T_J = 100˚C with the 50pF test load (C_L) shown in the figure at right.



SysClk and MemClk Timing

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.6	MHz
T_C	SysClk clock period	15	40	ns
T_{CS}	Clock edge stability		0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClk Output				
F_C	MemClk clock output frequency–200MHz		100	MHz
T_C	MemClk clock period–200MHz	10		ns
F_C	MemClk clock output frequency–266MHz		133	MHz
T_C	MemClk clock period–266MHz	7.5		ns
T_{CH}	Clock output high time	35% of nominal period	65% of nominal period	ns
T_{CL}	Clock output low time	35% of nominal period	65% of nominal period	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the NPe405L. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the NPe405L the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the NPe405L with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40 kHz. In some cases, on-board NPe405L peripherals impose more stringent requirements (see Note 1).
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClk since it also tracks the modulation.

Notes:

1. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation

2. Ethernet operation is unaffected.

3. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the NPe405L meets the above requirements and does not adversely affect other aspects of the system.

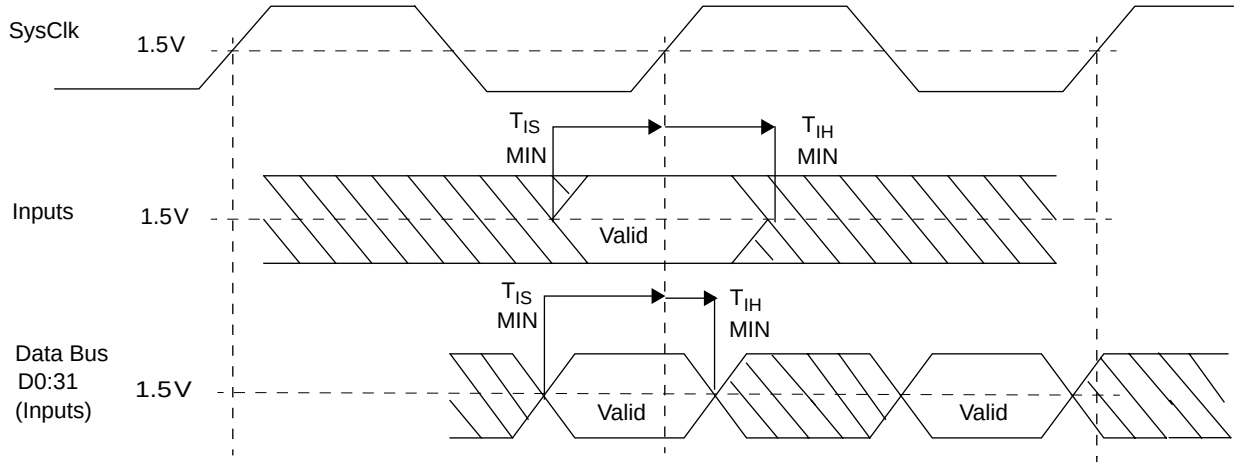
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
EMC0MDClk output frequency	–	2.5	MHz
EMC0MDClk period	400	–	ns
EMC0MDClk output high time	160	–	ns
EMC0MDClk output low time	160	–	ns
PHY0TxClk input frequency	2.5	25	MHz
PHY0TxClk period	40	400	ns
PHY0TxClk input high time	35% of nominal period	–	ns
PHY0TxClk input low time	35% of nominal period	–	ns
PHY0RxClk input frequency	2.5	25	MHz
PHY0RxClk period	40	400	ns
PHY0RxClk input high time	35% of nominal period	–	ns
PHY0RxClk input low time	35% of nominal period	–	ns
PerClk output frequency–200MHz (for synchronous slaves)	–	50	MHz
PerClk period–200MHz	20	–	ns
PerClk output frequency–266MHz (for synchronous slaves)	–	66	
PerClk period–266MHz	15	–	
PerClk output high time	50% of nominal period	66% of nominal period	ns
PerClk output low time	33% of nominal period	50% of nominal period	ns
UARTSerClk input frequency (Note 1)	–	$1000/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency–200MHz	–	50	MHz
TmrClk period–200MHz	20	–	ns
TmrClk input frequency–266MHz	–	66	
TmrClk period–266MHz	15	–	
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

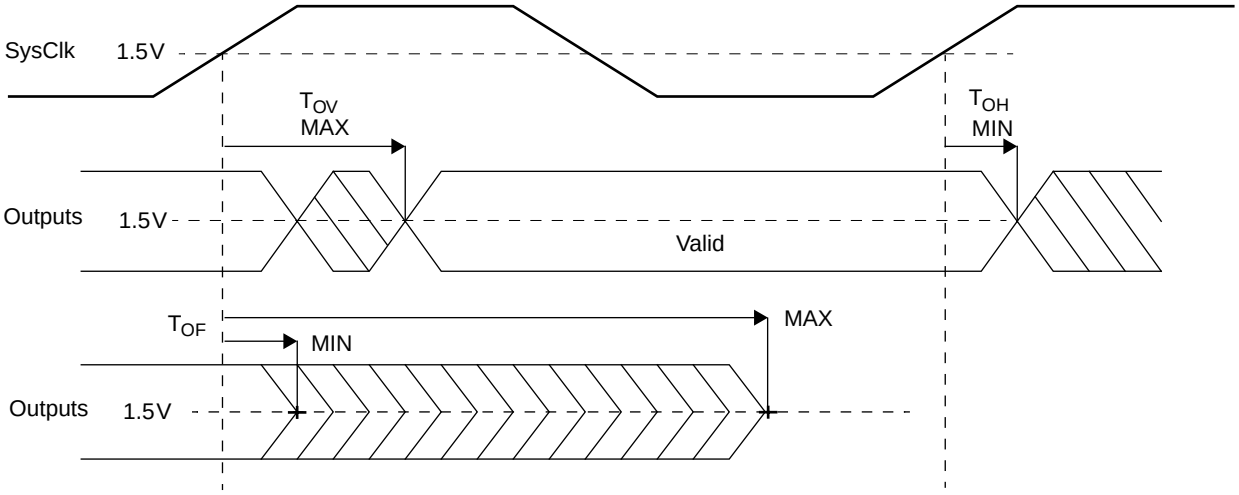
Notes:

1. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 50 MHz for 200MHz parts and 66MHz.for 266MHz parts.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—200MHz (Part 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	8.8	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1 [EMC0Tx0:1D]	n/a	n/a	10.5 [7.3] [5.0]	3.0 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	11.8 [7.2] [5.6]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr [EMC0Tx1En]	n/a	n/a	11.8[7.4]	2.9[2.4]	12	8	PHYTX	1
PHY0Col[PHY0Rx1Er]l	async[0.2]	async[1.7]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.9]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:1D]	1.5 [0.8] [0.9]	1.7 [1.7] [0.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV [PHY0CRS1DV]	1.3[0.7]	1.7[1.7]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.8[1.9]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.8	2.1	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	1.1	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	10.5	3.3	12	8		
HDLCEXTxFS	20.3	1.0	n/a	n/a	n/a	n/a		
HDLCEXTxEnA [GPIO28][$\overline{\text{UART1\_DCD}}$]	n/a	n/a	11.3	3.5	12	8		
HDLCEXTxEnB [GPIO29][$\overline{\text{UART1\_RI}}$]	n/a	n/a	11.8	3.8	12	8		
Internal Peripheral Interface								
IICSCL	async	async	async	async	17	11		
IICSDA	async	async	async	async	17	11		
[$\overline{\text{UART0\_CTS}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DCD}}$]	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—200MHz (Part 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
[$\overline{\text{UART0\_DSR}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DTR}}$]	n/a	n/a	async	async	12	8		
[$\overline{\text{UART0\_RI}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_RTS}}$]	n/a	n/a	async	async	12	8		
UART0_Rx	async	async	n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_CTS}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DCD}}$]GPIO28 [HDLCEXTxEnA]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DSR}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_DTR}}$]	n/a	n/a	async	async	12	8		
[$\overline{\text{UART1\_RI}}$]GPIO29 [HDLCEXTxEnB]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART1\_RTS}}$]	n/a	n/a	async	async	12	8		
UART1_Rx	async	async	n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a	async	async	12	8		
UARTSerClk	async	async	n/a	n/a	n/a	n/a		
Interrupts Interface								
[IRQ0:6]GPIO17:23	async	async	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	async	async	n/a	n/a	n/a	n/a		
TDI	async	async	n/a	n/a	n/a	n/a		
TDO	n/a	n/a	async	async	12	8		
TMS	async	async	n/a	n/a	n/a	n/a		
$\overline{\text{TRST}}$	async	async	n/a	n/a	n/a	n/a		
System Interface								
[TrcClk]GPIO0	n/a	n/a	11.2	1.2	12	8		
[TS1E]GPIO1	n/a	n/a	7.0	1.2	12	8		
[TS2E]GPIO2	n/a	n/a	7.0	1.2	12	8		
[TS1O]GPIO3	n/a	n/a	6.5	1.0	12	8		
[TS2O]GPIO4	n/a	n/a	6.4	1.0	12	8		
[TS3]GPIO5	n/a	n/a	6.4	1.0	12	8		
[TS4]GPIO6	n/a	n/a	6.4	1.0	12	8		
[TS5]GPIO7	n/a	n/a	6.6	1.0	12	8		
[TS6]GPIO8	n/a	n/a	6.4	1.0	12	8		
GPIO30	async	async	async	async	12	8		
$\overline{\text{Halt}}$	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—200MHz (Part 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SysClk	n/a	n/a	n/a	n/a	n/a	n/a		
SysErr	n/a	n/a	5.3	1.7	12	8		
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	12	8		
TestEn	dc	dc	n/a	n/a	n/a	n/a		
TmrClk	n/a	n/a	async	async	n/a	n/a		
SDRAM Interface								
BA1:0	n/a	n/a	7.2	1.5	19	12	SysClk	2, 3
$\overline{\text{BankSel3:0}}$	n/a	n/a	5.8	1.0	19	12	SysClk	3
$\overline{\text{CAS}}$	n/a	n/a	7.0	1.4	19	12	SysClk	2, 3
ClkEn0:1	n/a	n/a	4.9	1.0	40	25	SysClk	3
DQM3:0	n/a	n/a	5.9	1.0	19	12	SysClk	3
DQMCB	n/a	n/a	5.9	1.0	19	12	SysClk	3
ECC7:0	2.0	0.3	5.7	1.0	19	12	SysClk	3
MemAddr12:0	n/a	n/a	7.2	1.4	19	12	SysClk	2, 3
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	3, 4
MemData31:0	2.0	0.3	5.6	1.0	19	12	SysClk	3
$\overline{\text{RAS}}$	n/a	n/a	7.4	1.6	19	12	SysClk	2, 3
$\overline{\text{WE}}$	n/a	n/a	7.1	1.4	19	12	SysClk	2, 3
External Slave Peripheral Interface								
$\overline{\text{DMAReq0:3}}$[GPIO9:12]	4.8	0.0	7.0	1.1	n/a	n/a	PerClk	
$\overline{\text{DMAAck0:3}}$[GPIO13:16]	n/a	n/a	7.5	1.1	12	8	PerClk	
$\overline{\text{EOT0:3}}$[$\overline{\text{TC0:3}}$] [GPIO24:27]	4.3	-0.1	8.5	1.2	12	8	PerClk	
PerAddr4:31	n/a	n/a	8.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	7.4	1.4	12	8	PerClk	
$\overline{\text{PerCS0:3}}$	n/a	n/a	7.2	1.3	12	8	PerClk	
PerData0:15	4.8	1.0	9.3	1.0	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	7.6	1.4	12	8	PerClk	
PerPar0:1	3.1	0.0	8.3	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	7.5	1.4	12	8	PerClk	
PerReady	7.5	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:1}}$	n/a	n/a	7.5	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	5
PerErr	4.0	-0.6	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWE}}$[GPIO31]	n/a	n/a	8.3	1.3	12	8		

I/O Specifications—266MHz (Part 1 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
Ethernet Interface								
EMC0MDClk	n/a	n/a	7.4	1.5	12	8		1, async
EMC0MDIO	n/a	n/a	6.7	1.2	12	8	EMC0MDClk	1
EMC0TxD0:3 [EMC0Tx0:1D0:1 [EMC0Tx0:1D]	n/a	n/a	7.7 [5.6] [4.6]	3.0 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxEn [EMC0Tx0En] [EMC0Sync]	n/a	n/a	9.4 [5.5] [4.2]	2.9 [2.3] [1.7]	12	8	PHYTX	1
EMC0TxErr [EMC0Tx1En]	n/a	n/a	9.4[5.7]	2.9[2.4]	12	8	PHYTX	1
PHY0Col[PHY0Rx1Er]l	async[0.1]	async[1.4]	n/a	n/a	n/a	n/a		1
PHY0CrS[PHY0CrS0DV]	async[0.1]	async[1.5]	n/a	n/a	n/a	n/a		1
PHY0RxClk	n/a	n/a	n/a	n/a	n/a	n/a		1, async
PHY0RxD0:3 [PHY0Rx0:1D0:1] [PHY0Rx0:1D]	1.5 [0.8] [0.8]	1.4 [1.3] [0.2]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxDV [PHY0CRS1DV]	1.3[0.7]	1.3[1.3]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0RxErr[PHY0Rx0Er]	1.3[0.7]	1.4[1.5]	n/a	n/a	n/a	n/a	PHYRX	1
PHY0TxClk[PHY0RefClk]	n/a	n/a	n/a	n/a	n/a	n/a		1, async
HDLCEX Interface								
HDLCEXRxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXRxDataA:B	23.8	1.5	n/a	n/a	n/a	n/a		
HDLCEXRxFS	24.2	0.8	n/a	n/a	n/a	n/a		
HDLCEXTxClk	n/a	n/a	n/a	n/a	n/a	n/a		
HDLCEXTxDataA:B	n/a	n/a	7.6	3.3	12	8		
HDLCEXTxFS	24.2	0.8	n/a	n/a	n/a	n/a		
HDLCEXTxEnA [GPIO28][$\overline{\text{UART1\_DCD}}$]	n/a	n/a	8.5	3.5	12	8		
HDLCEXTxEnB [GPIO29][$\overline{\text{UART1\_RI}}$]	n/a	n/a	8.9/	3.8	12	8		
Internal Peripheral Interface								
IICSCL	async	async	async	async	17	11		
IICSDA	async	async	async	async	17	11		
[$\overline{\text{UART0\_CTS}}$]	async	async	n/a	n/a	n/a	n/a		
[$\overline{\text{UART0\_DCD}}$]	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—266MHz (Part 2 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
[UART0_DSR]	async	async	n/a	n/a	n/a	n/a		
[UART0_DTR]	n/a	n/a	async	async	12	8		
[UART0_RI]	async	async	n/a	n/a	n/a	n/a		
[UART0_RTS]	n/a	n/a	async	async	12	8		
UART0_Rx	async	async	n/a	n/a	n/a	n/a		
UART0_Tx	n/a	n/a	async	async	12	8		
[UART1_CTS]	async	async	n/a	n/a	n/a	n/a		
[UART1_DCD]GPIO28 [HDLCEXTxEnA]	async	async	n/a	n/a	n/a	n/a		
[UART1_DSR]	async	async	n/a	n/a	n/a	n/a		
[UART1_DTR]	n/a	n/a	async	async	12	8		
[UART1_RI]GPIO29 [HDLCEXTxEnB]	async	async	n/a	n/a	n/a	n/a		
[UART1_RTS]	n/a	n/a	async	async	12	8		
UART1_Rx	async	async	n/a	n/a	n/a	n/a		
UART1_Tx	n/a	n/a	async	async	12	8		
UARTSerClk	async	async	n/a	n/a	n/a	n/a		
Interrupts Interface								
[IRQ0:6]GPIO17:23	async	async	n/a	n/a	n/a	n/a		
JTAG Interface								
TCK	async	async	n/a	n/a	n/a	n/a		
TDI	async	async	n/a	n/a	n/a	n/a		
TDO	n/a	n/a	async	async	12	8		
TMS	async	async	n/a	n/a	n/a	n/a		
TRST	async	async	n/a	n/a	n/a	n/a		
System Interface								
[TrcClk]GPIO0	n/a	n/a	8.7	1.2	12	8		
[TS1E]GPIO1	n/a	n/a	5.8	1.2	12	8		
[TS2E]GPIO2	n/a	n/a	5.7	1.2	12	8		
[TS1O]GPIO3	n/a	n/a	5.3	1.0	12	8		
[TS2O]GPIO4	n/a	n/a	5.3	1.0	12	8		
[TS3]GPIO5	n/a	n/a	5.3	1.0	12	8		
[TS4]GPIO6	n/a	n/a	5.3	1.0	12	8		
[TS5]GPIO7	n/a	n/a	5.4	1.0	12	8		
[TS6]GPIO8	n/a	n/a	5.3	1.0	12	8		
GPIO30	async	async	async	async	12	8		
Halt	async	async	n/a	n/a	n/a	n/a		

I/O Specifications—266MHz (Part 3 of 3)

Notes:

1. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.
2. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
3. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
4. SDRAM MemClkOut0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
5. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SysClk	n/a	n/a	n/a	n/a	n/a	n/a		
SysErr	n/a	n/a	5.3	1.7	12	8		
$\overline{\text{SysReset}}$	n/a	n/a	n/a	n/a	12	8		
TestEn	dc	dc	n/a	n/a	n/a	n/a		
TmrClk	n/a	n/a	async	async	n/a	n/a		
SDRAM Interface								
BA1:0	n/a	n/a	5.5	1.5	19	12	SysClk	1, 2
$\overline{\text{BankSe3:0}}$	n/a	n/a	4.6	1.0	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	5.3	1.4	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	3.9	1.0	40	25	SysClk	2
DQM3:0	n/a	n/a	4.7	1.0	19	12	SysClk	2
DQMCB	n/a	n/a	4.7	1.0	19	12	SysClk	2
ECC7:0	1.8	0.3	4.5	1.0	19	12	SysClk	2
MemAddr12:0	n/a	n/a	5.5	1.4	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0.4	-1.2	19	12	SysClk	2, 3
MemData31:0	1.8	0.3	4.4	1.0	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	5.7	1.6	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	5.4	1.4	19	12	SysClk	1, 2
External Slave Peripheral Interface								
$\overline{\text{DMAReq0:3}}$[GPIO9:12]	4.1	0.0	5.5	1.1	n/a	n/a	PerClk	
$\overline{\text{DMAAck0:3}}$[GPIO13:16]	n/a	n/a	5.8	1.1	12	8	PerClk	
$\overline{\text{EOT0:3}}$[$\overline{\text{TC0:3}}$] [GPIO24:27]	3.7	-0.1	6.7	1.2	12	8	PerClk	
PerAddr4:31	n/a	n/a	6.5	0.9	17	11	PerClk	
$\overline{\text{PerBLast}}$	n/a	n/a	5.6	1.4	12	8	PerClk	
$\overline{\text{PerCS0:3}}$	n/a	n/a	5.5	1.3	12	8	PerClk	
PerData0:15	3.9	1.0	7.1	1.0	17	11	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerPar0:1	2.7	0.0	6.4	0.9	17	11	PerClk	
PerR/$\overline{\text{W}}$	n/a	n/a	5.7	1.4	12	8	PerClk	
PerReady	6.2	-0.5	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:1}}$	n/a	n/a	5.7	1.3	12	8	PerClk	
PerClk	n/a	n/a	0.5	-0.9	17	11	PLB Clk	4
PerErr	3.5	-0.6	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWE}}$[GPIO31]	n/a	n/a	7.0	1.3	12	8		

Initialization

The following describes the method by which initial chip settings are established when a system reset occurs.

Pin Strapping

While the $\overline{\text{SysReset}}$ input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to NPe405L start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options.

Strapping Pin Assignments

Function	Option	Ball Strapping	
Width of boot device on EBC data bus		**Y21**	
	8 bits	0	
	16 bits	1	
Ethernet ZMII mode		**V21**	**U20**
	MII mode	0	0
	SMII mode	0	1
	RMII 10 Mbps mode	1	0
	RMII 100 Mbps mode	1	1

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IBM Microelectronics Division
1580 Route 52
Hopewell Junction, NY 12533-6351

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