

MV8804

8 x 4 BIDIRECTIONAL ANALOG SWITCH ARRAY

The MV8804 is a CMOS/LSI 8 x 4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. The circuit has digitally-controlled analog switches having very low 'ON' resistance and very low 'OFF' leakage current. The switches will operate with analog signals at frequencies up to 40MHz and up to 13.0V peak-to-peak. A 'HIGH' on the Master Reset input switches all channels 'OFF' and clears the memory. The MV8804 is ideal for crosspoint switching applications.

FEATURES

- Microprocessor Compatible Control Inputs
- On-Chip Control Memory And Address Decoding
- Row Addressing
- Master Reset
- 32 Crosspoint Switches in 8 x 4 Array
- 5.0V to 13.0V Operation
- Low Crosstalk Between Switches
- Low On Resistance: 90Ω (typ.) At 10V
- Matched Switch Characteristics
- Switches Frequencies Up To 40MHz

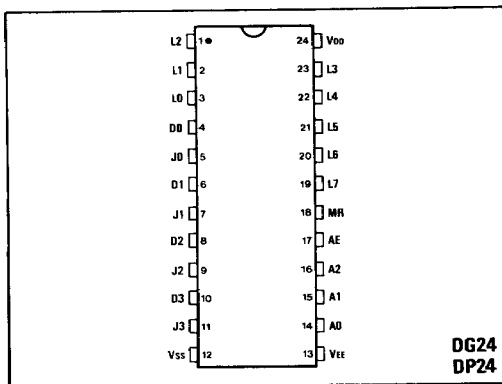


Fig.1 Pin connections - top view

APPLICATIONS

- PABX And Key Systems
- Data Acquisition Systems
- Test Equipment/Instrumentation
- Analog/Digital Multiplexers

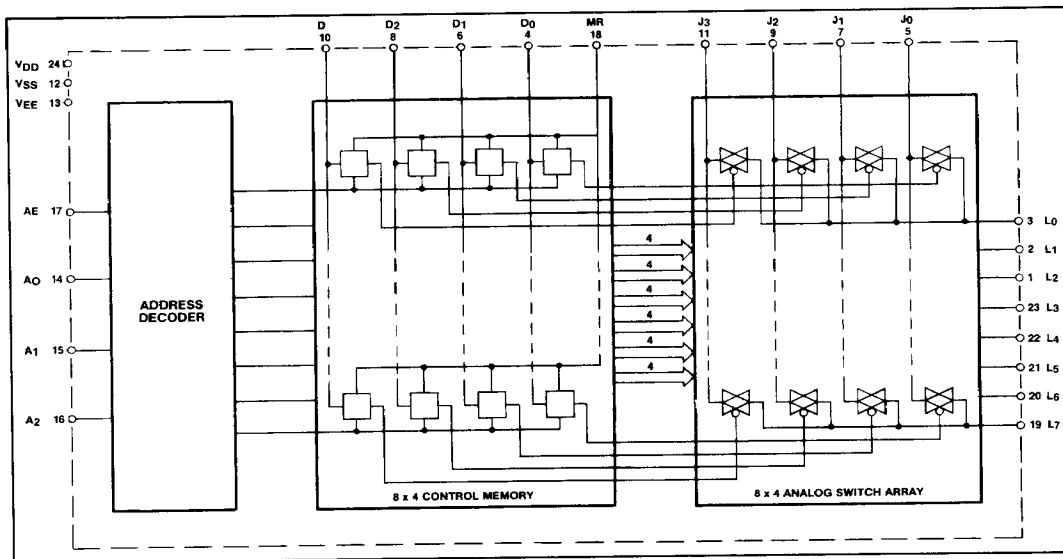


Fig.2 MV8804 functional block diagram

ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

	Min.	Max.		Min.	Max.
$V_{DD} - V_{SS}$	-0.3V	16V	Storage temperature	-65°C	+125°C
$V_{DD} - V_{EE}$	-0.3V	16V	(DP package)		
$V_{SS} - V_{EE}$	-0.3V	16V	Power dissipation		1200mW*
Voltage on any logic pin	$V_{SS} - 0.3V$	$V_{DD} + 0.3V$	(DG package)		
Voltage on any line (V_L) or junctor (V_J)	$V_{EE} - 0.3V$	$V_{DD} + 0.3V$	Power dissipation		600mW**
Current at any logic pin		10mA	(DP package)		
Operating temperature (all packages)	-40°C	+85°C			
Storage temperature (DG package)	-65°C	+150°C			

* Derate 16mW/°C above 75°C. All leads soldered to PC board.

** Derate 6.3mW/°C above 25°C. All leads soldered to PC board.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = +25^\circ\text{C}$, $V_{SS} - V_{EE} = 0V$, $V_{is} = 5V$ p-p, $C_L = 50pF$, $R_L = 10k\Omega$, $t_r = t_f = 20ns$ (input signal)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Sine wave response (distortion)			0.1 0.2 1.0		%	$V_{DD} = 13V$ } $V_{DD} = 10V$ } $f_{in} = 1kHz$ $V_{DD} = 5V$ }
Frequency response channel 'ON' (sine wave input)			40		MHz	$V_C = V_{DD} = 10V$, $\frac{V_o}{V_i} = -3dB$
Feedthrough channel 'OFF'			-40		dB	$V_{DD} = 10V$, $V_C = V_{EE}$, $R_L = 1k\Omega$, $f_{in} = 1MHz$
Crosstalk between any two channels			-40 -90		dB	$f_{in} = 1.0MHz$ } $V_{DD} = 10V$, Switch A $f_{in} = 3.4kHz$ } 'ON', Switch B 'OFF'
Propagation delay Signal input to signal output	t_{PS}		10		ns	$V_{DD} = 10V$, Switch 'ON'
Turn 'ON' propagation delay Data input to signal output	t_{PLH} t_{PHL}		200 400		ns	$V_{DD} = 10V$ $V_{DD} = 5V$
Address enable to signal output	t_{PAE}		300 600		ns	$V_{DD} = 10V$ $V_{DD} = 5V$
Minimum address enable (AE) Pulse width	t_{AE}		90 225		ns	$V_{DD} = 10V$ $V_{DD} = 5V$
Minimum set-up time Address to AE	t_s	0	50		ns	$V_{DD} = 10V$
		0	90		ns	$V_{DD} = 5V$
Data in to AE	t_s		50 90		ns	$V_{DD} = 10V$ $V_{DD} = 5V$
Minimum Hold Time Address or data in to address enable	t_h		50 90		ns	$V_{DD} = 10V$ $V_{DD} = 5V$
Memory reset time	t_{MR}		175		ns	$V_{DD} = 10V$, $R_L = 1k\Omega$
Memory reset recovery time	T_{MRR}		150 250		ns	$V_{DD} = 10V$ } $V_{DD} = 5V$ } $R_L = 1k\Omega$

DC ELECTRICAL CHARACTERISTICS**Test conditions (unless otherwise stated):**

$$T_{amb} = +25^{\circ}\text{C}, V_{SS} = V_{EE} = 0\text{V}$$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Operating voltage range						
Digital	$V_{DD} - V_{SS}$	5	5	13	V	
Analog	$V_{DD} - V_{EE}$	5	10	13	V	
Logic level converter	$V_{SS} - V_{EE}$	0	5	12	V	
On state resistance	R_{ON}		75	108	Ω	$V_{DD} = 13\text{V}$
			90		Ω	$V_{DD} = 10\text{V}$
			240		Ω	$V_{DD} = 5\text{V}$
Difference in On state	R_{ON}		20		Ω	$V_{DD} = 13\text{V}$
Resistance between any switches			30		Ω	$V_{DD} = 10\text{V}$
Off state leakage current (any line to any junctor)	I_{OFF}		± 0.01	± 500	nA	$V_{DD} = 13\text{V}$, selected crosspoint in Off state
Input logic '0' level	V_{IL}		4.5		V	$V_{DD} = 10\text{V}$
			2.25	1.5	V	$V_{DD} = 5\text{V}$
Input logic '1' level	V_{IH}		5.5		V	$V_{DD} = 10\text{V}$
		3.5	2.75		V	$V_{DD} = 5\text{V}$
Quiescent device current (per package)	I_Q		0.1	500	μA	$V_{DD} = 13\text{V}$
Maximum current through crosspoint switch	I_{MAX}		± 8.0		mA	$V_{DD} = 13\text{V}$
Switch input capacitance	C_{is}		5		pF	$V_{DD} = 10\text{V}$, $V_{in} = 0\text{V}$
Switch output capacitance	C_{os}		20		pF	$V_{DD} = 10\text{V}$, $V_{in} = 0\text{V}$
Feedthrough capacitance	C_{ios}		0.2		pF	$V_{DD} = 10\text{V}$, $V_{in} = 0\text{V}$
Digital input capacitance	C_{in}		5		pF	$V_{DD} = 10\text{V}$, $V_{in} = 0\text{V}$

NOTES

1. Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing.
2. V_{is} is the analog switch input voltage. V_{in} is digital input voltage.

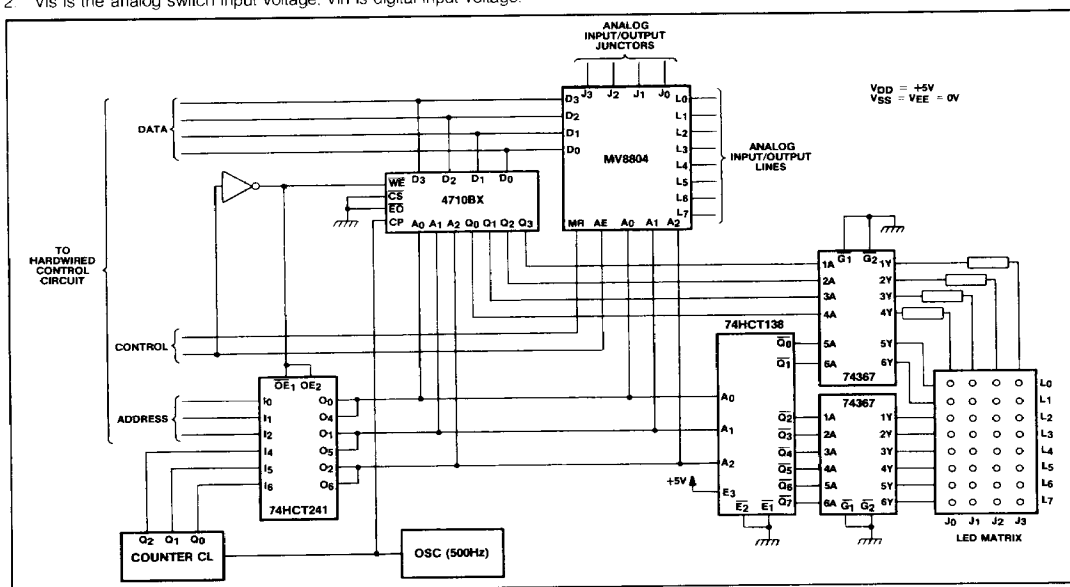


Fig.3 Visual indication of MV8804 control memory status

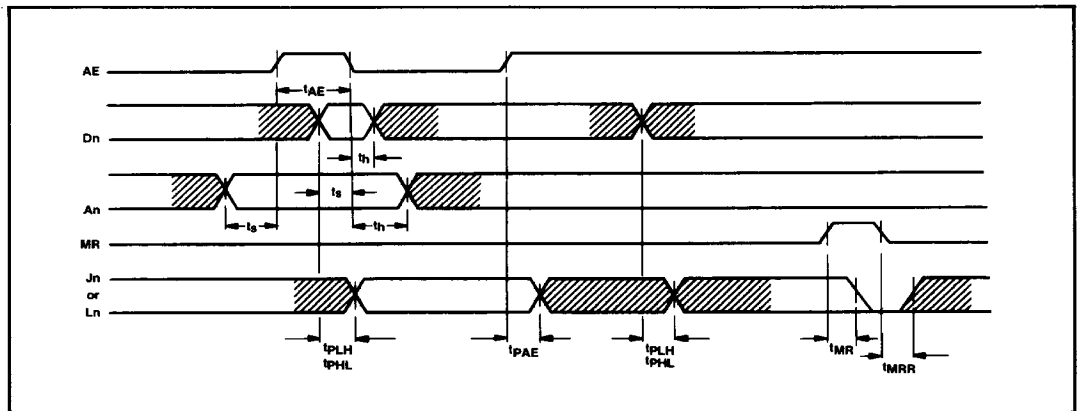


Fig.4 Timing waveforms

PIN DESCRIPTION

Pin	Name	Description
1	L ₂	Analog Switch Array Input/Output Line
2	L ₁	Analog Switch Array Input/Output Line
3	L ₀	Analog Switch Array Input/Output Line
4	D ₀	Control Memory Data Line Input
5	J ₀	Analog Switch Array Input/Output Junctor
6	D ₁	Control Memory Data Line Input
7	J ₁	Analog Switch Array Input/Output Junctor
8	D ₂	Control Memory Data Line Input
9	J ₂	Analog Switch Array Input/Output Junctor
10	D ₃	Control Memory Data Line Input
11	J ₃	Analog Switch Input/Output Junctor
12	V _{SS}	Negative Digital Power Supply
13	V _{EE}	Negative Analog Power Supply
14	A ₀	Control Memory Address Input
15	A ₁	Control Memory Address Input
16	A ₂	Control Memory Address Input
17	AE	Control Memory Address Enable Input (Strobe)
18	MR	Master Reset
19	L ₇	Analog Switch Array Input/Output Line
20	L ₆	Analog Switch Array Input/Output Line
21	L ₅	Analog Switch Array Input/Output Line
22	L ₄	Analog Switch Array Input/Output Line
23	L ₃	Analog Switch Array Input/Output Line
24	V _{DD}	Positive Analog/Digital Power Supply

FUNCTIONAL DESCRIPTION

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as LINES (L₀-L₇) and the column input/outputs as JUNCTORS (J₀-J₃). The crosspoint analog switches interconnect the lines and junctors when turned 'ON' and provide a high degree of isolation when turned 'OFF'. Interchannel crosstalk is minimal despite the high density of the analog switch array.

The control memory of the MV8804 can be treated as an 8-word by 4-bit random access memory. The 8 words are selected by the ADDRESS (A₀-A₂) inputs through the on-chip address decoder. Data is presented to the memory via the 4 DATA inputs (D₀-D₃). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is high. A high level written into a memory cell turns the corresponding crosspoint switch 'ON'

while a low level causes the crosspoint to turn 'OFF'.

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A high level on the MASTER RESET (MR) input returns all memory locations to a low level and turns all crosspoint switches 'OFF', effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with V_{DD} = 5V, V_{SS} = 0V and V_{EE} = -6V, the control inputs can be driven by a 5V system while the analog voltages through the crosspoint switches can swing from +5V to -6V.

LOGIC TRUTH TABLE

Master Reset	Address enable	Address			Addressed line	Input data to control memory				Junctions connected to addressed line			
MR	AE	A ₂	A ₁	A ₀		D ₃	D ₂	D ₁	D ₀	J ₃	J ₂	J ₁	J ₀
H L	X L	X X	X X	X X	All None	X X	X X	X X	X X	All switches 'Off' No change of state			
L	H	L	L	L	L ₀	L	L	L	L	•	•	•	•
L	H	L	L	L	L ₀	L	L	L	H	•	•	•	+
L	H	L	L	L	L ₀	L	L	H	L	•	•	+	•
L	H	L	L	L	L ₀	L	L	H	H	•	•	+	+
L	H	L	L	L	L ₀	L	H	L	L	•	+	•	•
L	H	L	L	L	L ₀	L	H	L	H	•	+	•	+
L	H	L	L	L	L ₀	L	H	H	L	•	+	+	•
L	H	L	L	L	L ₀	L	H	H	H	•	+	+	+
L	H	L	L	L	L ₀	H	L	L	L	+	•	•	•
L	H	L	L	L	L ₀	H	L	L	H	+	•	•	+
L	H	L	L	L	L ₀	H	L	H	L	+	•	+	•
L	H	L	L	L	L ₀	H	L	H	H	+	•	+	+
L	H	L	L	L	L ₀	H	H	L	L	+	+	•	•
L	H	L	L	L	L ₀	H	H	L	H	+	+	•	+
L	H	L	L	L	L ₀	H	H	H	L	+	+	+	•
L	H	L	L	L	L ₀	H	H	H	H	+	+	+	+
L	H	L	L	H	L ₁	Each addressed line may have 16 different combinations of junctions connected to it by inputting data to the control memory as shown for L ₀ .							
L	H	L	H	L	L ₂								
L	H	L	H	H	L ₃								
L	H	H	L	L	L ₄								
L	H	H	L	H	L ₅								
L	H	H	H	L	L ₆								
L	H	H	H	H	L ₇								

NOTES

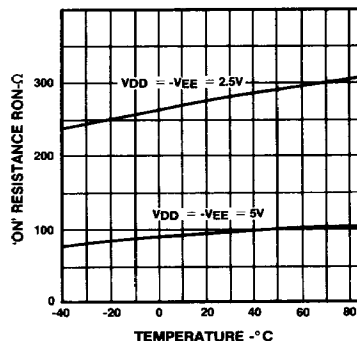
L = Low Logic Level
H = High Logic Level
X = Don't Care Condition
+ = Indicates Connection Between Junctor and Addressed Line
● = Indicates No Connection Between Junctor and Addressed Line

8 x 8 ANALOG/DIGITAL SWITCH

Two MV8804s configured as shown in Fig.7, implement an 8 x 8 analog/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the N dimension is as shown and connecting the lines (L0-L7) from the MV8804s in common.

Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MV8804 junctors (J0-J3) in common. The address and data control inputs of the MV8804s can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually, for example by a 74HCT515 programmable AND gate.

A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.



**Fig.5 ON resistance vs temperature
(input signal voltage = supply voltage/2)**

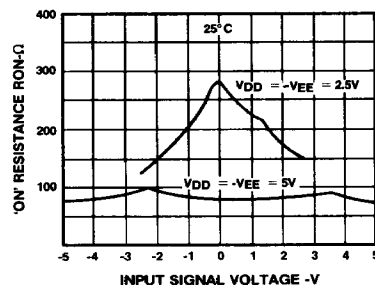


Fig.6 ON resistance vs input signal voltage

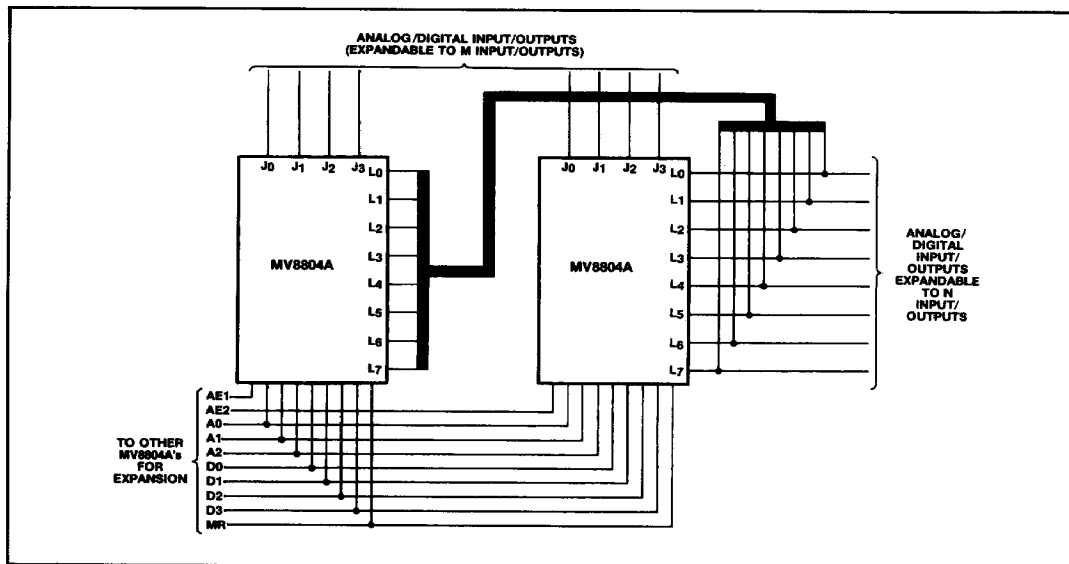


Fig.7 Expanding MV8804s