LZ22250G Color CCD Area Sensor

Description

LZ22250G is a 2/3 inch solid-state image sensor composed of PN photodiodes and CCDs (charge-coupled device). With its approximately 250,000 pixels (530 horizontal×490 vertical), it provides a high-resolution stable color image.

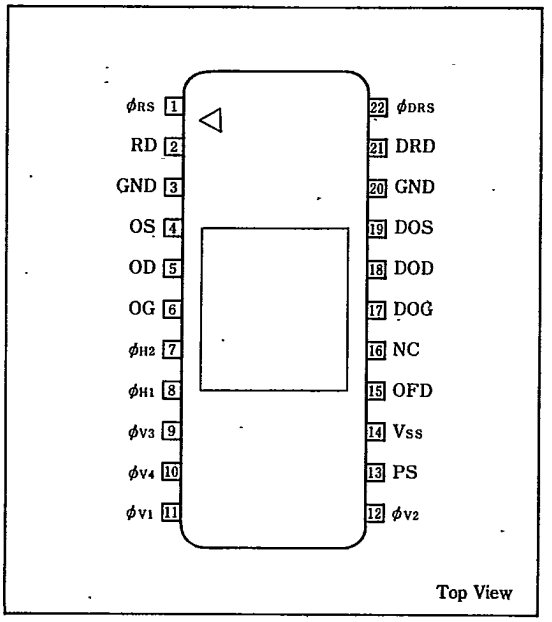
Features

1. The number of pixels of 530 horizontal×490 vertical
   Pixel pitch of 17.2 μm (H)×13.5 μm (V)
   (530 horizontal pixels consists of 510 effective pixels+20 optical black reference pixels)
2. Ye, Cy, Mg, G color filter array
3. Low fixed pattern noise and lag
4. No geometric distortion and burn-in
5. Anti-blooming structure
6. Built-in output amplifier and compensation amplifier
7. 22-pin dual-in-line package (ceramic)

Applications

1. Camera (for consumer use, for industrial supervision)
2. Shape recognition

Pin Connections



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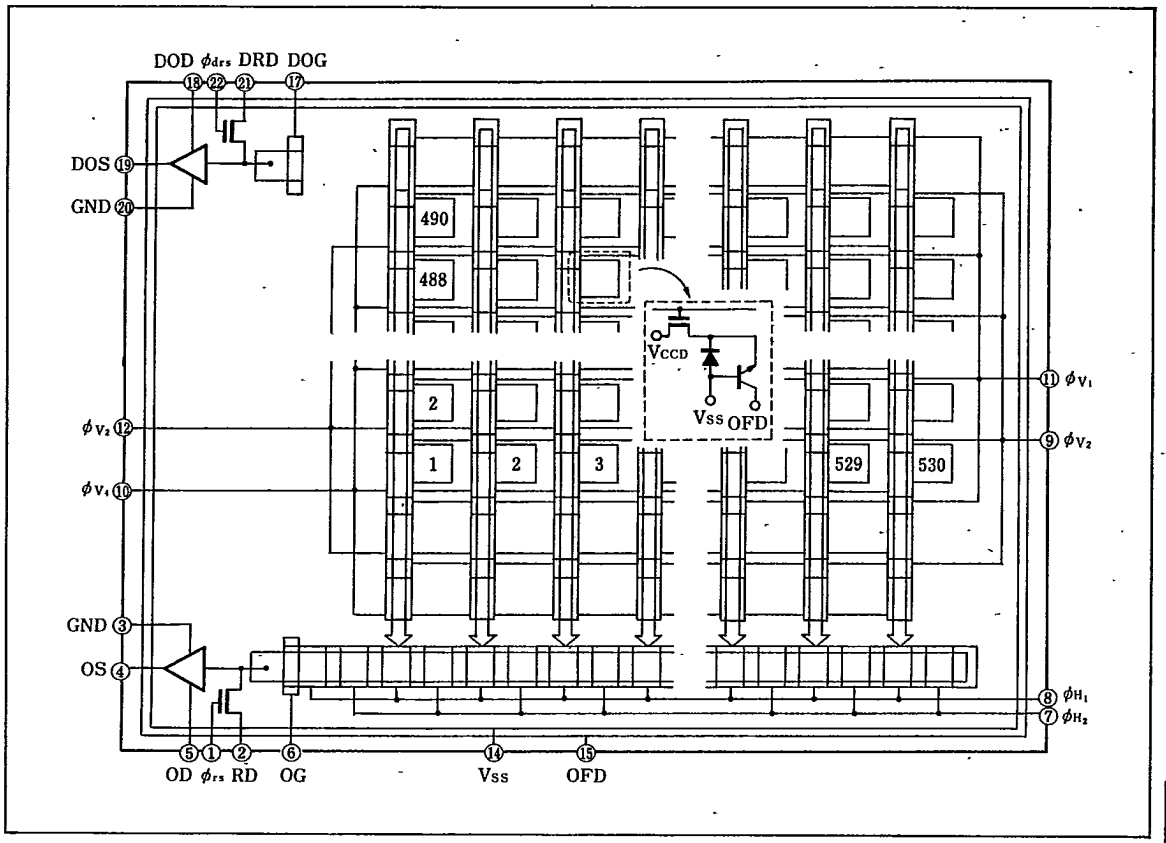
■ Block Diagram



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■ Pin Description

Pin name	Name
DRD	(Dummy) Reset Transister Drain
DOG	(Dummy) Output Gate
DOD	(Dummy) Output Transister Drain
DOS	(Dummy) Video Output
ϕ_{DRS}	(Dummy) Reset Transister Gate Clock
ϕ_{V1}, ϕ_{V2}, ϕ_{V3}, ϕ_{V4}	Vertical Shift Register Clock
ϕ_{H1}, ϕ_{H2}	Horizontal Shift Register Clock
OFD	Overflow Drain
PS	Photoshield
V_{SS}	Substrate
GND	Ground
NC	Non Connection

■ Absolute Maximum Ratings

(Ta=25℃)

Parameter	Symbol	Conditions	Rating	Unit	Note
Applied voltages	V_{TE} ①	V_{SS}=0V	−6.0 to +20	V	1
	V_{TE} ②	V_{SS}=0V	−0.3 to +20	V	2
	V_{TE} ③	V_{SS}=0V	−0.3 to +18	V	3
	V_{TE} ④	V_{SS}=0V	0 to +22	V	4
Storage temperature	T_{stg}		−20 to +70	℃	
Operating temperature	T_{opr}		−10 to +55	℃	

Note 1 : Applied to pins ϕ_{V1}, ϕ_{V2}, ϕ_{V3} and ϕ_{V4}.
Note 2 : Applied to pins ϕ_{H1}, ϕ_{H2}, ϕ_{RS} ϕ_{DRS}, OG, DOG, and PS.
Note 3 : Applied to pins OD, DOD, RD and DRD.
Note 4 : Applied to OFD pin.

■ Recommended Operating Conditions

(Field-Integration Mode)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
DC Conditions					
Reset transistor drain voltage	V_{RD}	13.0	13.5	14.0	V
Dummy reset transistor drain voltage	V_{DRD}	13.0	13.5	14.0	V
Output gate voltage	V_{OG}	2.0	2.5	3.0	V
Dummy output gate voltage	V_{DOG}	2.0	2.5	3.0	V
Output transistor drain voltage	V_{OD}	13.0	13.5	14.0	V
Dummy output transistor drain voltage	V_{DOD}	13.0	13.5	14.0	V
Overflow drain voltage	V_{OFD}	4.0		20.0	V
Photoshield voltage	V_{PS}		0		V
Substrate voltage	V_{SS}		0		V
Ground voltage	GND		0		V
AC Conditions					
Vertical shift register clock "Low" level	$V\phi_{V1L}$, $V\phi_{V2L}$ $V\phi_{V3L}$, $V\phi_{V4L}$	−5.5	−5.0	−4.5	V
Vertical shift register clock INTERMEDIATE level	$V\phi_{V1I}$, $V\phi_{V2I}$ $V\phi_{V3I}$, $V\phi_{V4I}$	1.0	1.5	2.0	V
Vertical shift register clock "High" level	$V\phi_{V1H}$, $V\phi_{V2H}$ $V\phi_{V3H}$, $V\phi_{V4H}$	5.5	6.0	6.5	V
Horizontal shift register clock "Low" level	$V\phi_{H1L}$, $V\phi_{H2L}$	−0.2	0	0.35	V
Horizontal shift register clock "High" level	$V\phi_{H1H}$, $V\phi_{H2H}$	8.5	9.0	9.5	V
Reset gate clock Dummy reset gate clock "Low" level	$V\phi_{RSL}$, $V\phi_{DRSL}$	−0.2	0	0.50	V
Reset gate clock Dummy reset gate clock "High" level	$V\phi_{RSH}$, $V\phi_{DRSH}$	8.5	9.0	9.5	V
Vertical shift register clock frequency	$f\phi_{V1}$, $f\phi_{V2}$ $f\phi_{V3}$, $f\phi_{V4}$		15.734		kHz
Horizontal shift register frequency	$f\phi_{H1}$, $f\phi_{H2}$		9.58		MHz
Reset gate clock Dummy reset gate clock frequency	$f\phi_{RS}$, $f\phi_{DRS}$		9.58		MHz

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■ Electrical Characteristics

Ta=25℃ (* : Ta=+55℃)

Operating conditions : Use typical values for the recommended operating conditions.

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Saturation output voltage	V_{sat}	250			mV	
Photo response non-uniformity	PRNU			10	%	1, 2
Dark output voltage	V_{dark}			30*	mV	
Dark signal non-uniformity	DSNU		4	7*	mV	1, 3
Responsivity	R	15	20		mV/Lx	4, 5
Gamma	γ		1			
Signal/Noise ratio	S/N	47	50		dB	6
Smear ratio	SMR	65	75		−dB	7, 8
Dissipation current	I_{OD}+ I_{DOD}	11	14	17	mA	9
Lag	AI		6	8	%	10
Antiblooming	ABL	14				11

Note 1 : The image area is sectioned into 10×10 small areas. The signal on the small area is calculated by averaging pixel signals over the small area.

Note 2 : Defined by $V_{MAX.}$-$V_{MIN.}$ under standard-exposure (V_{sig}=150mV), where $V_{MAX.}$ and $V_{MIN.}$ are the maximum and the minimum of the signals on the small areas.

Note 3 : Defined by $V_{MAX.}$-$V_{MIN.}$ under non-exposure, where $V_{MAX.}$ and $V_{MIN.}$ are the maximum and the minimum of the signals on the small areas.

Note 4 : The light source is 3200K tungsten illumination with the IR-absorbing filter (HOYA CM500 1mm thick).

Note 5 : Defined by the signal voltage at 1 lux.

Note 6 : Defined by Vo/V_{rms}, where V_{rms} is the temporal r.m.s output noise (50k-3MHz) in the dark.

Note 7 : Defined by the ratio of the maximum signal (Mg+Ye) to the V/10 smear level that is detected during the vertical blanking period.

Note 8 : The light source is 3200°K halogen illumination with the IR-absorbing filter (HOYA CM500, 1mm thick).

Note 9 : Defined by the total current flowing to OD and DOD pins.

Note 10 : Defined by the ratio of the maximum signal (Mg+Ye) to the lag that is detected after 3-field under 1/3 standard-exposure.

Note 11 : Judged by the image of V/10 square under 14 times exposure of the knee point, where V represents the picture height.

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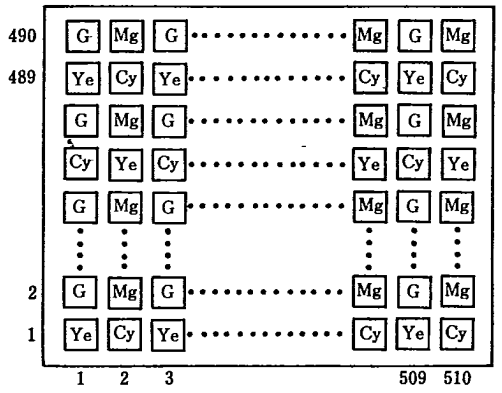
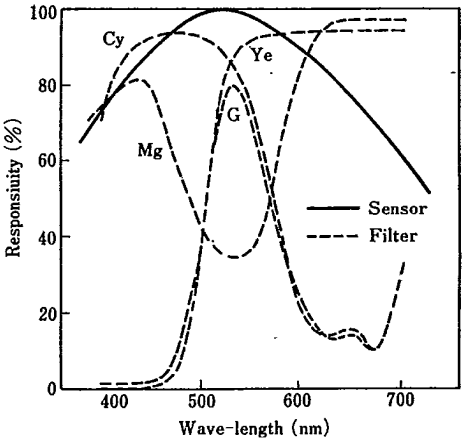
■ Color Filter Array



■ Spectral Response



■ Specification of Blemish

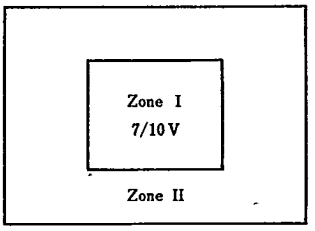
	Total	Zone Ⅰ	Zone Ⅱ
Number of Blemishes	6	4	※
Number of Compensation Blemishes	3	2	※

Blemish	White blemish	Black blemish
Blemish Level	Over+5mV	Under−7mV
Compensation Blemish Level	Over+5mV	Under−13mV

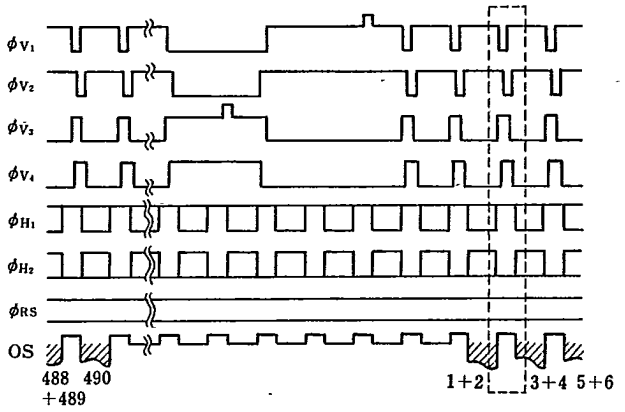
※ Less than total number of blemishes.

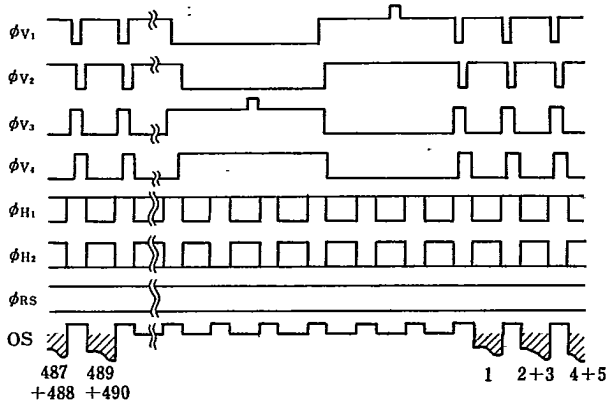
■ Conditions

1. Operating temperature : 40℃
2. Measurement exposure : Signal level is 85mV
3. Effective zone : Measurement excludes the outer 2-pixels



■ Clock Timing Chart





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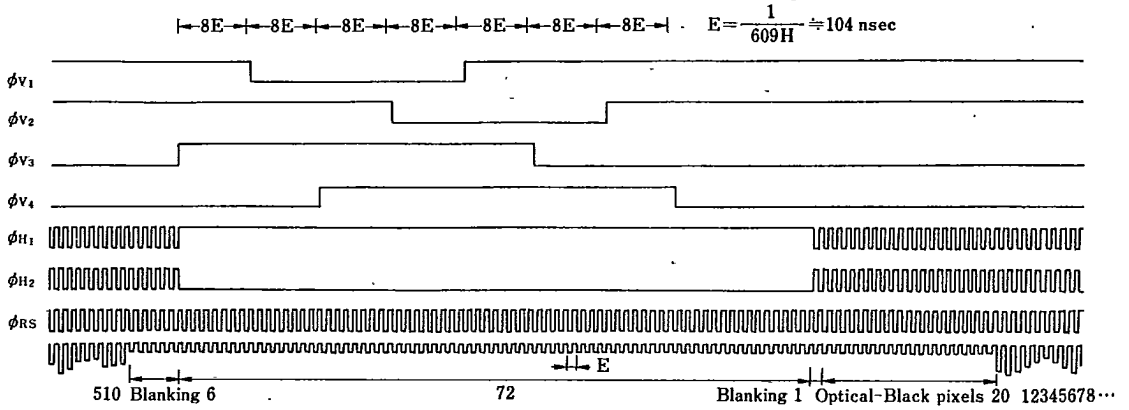

Handling Precautions

1. Caution should be exercised against a possible damage to the cap caused by a mechanical stress as it uses glass building material.
2. Keep as much as you can from touching the glass surface as the charged glass surface may destroy elements inside.
3. As in the ordinary MOS or LSI, electrically conductive material should be provided for protection against an electrostatic destruction when it is not in use.
4. When handling device, make sure that you and the tools are grounded for the static electricity to be discharged.
   A human body shall be grounded through a register of approximately 1MΩ. Keep always in mind, the electrostatic voltage be lower than the ordinary MOSs or LSIs withstand.
5. To clean the glass surface use an applicator with a small amount of iso-propyl alcohol on the tip, stroke the glass-surface gently in one direction.
6. Do not expose the device to light except in operation when the device is mounted on a camera.

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Standard Operating Circuit

(Color video camera for NTSC TV in the field-integration mode)