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IIT-IGA
Integrated Graphics Array

A single chip combines IBM personal graphic standards into a high-end, fully backward-compatible graphics solution that provides the following benefits:

- 1/5 the board space
- Full software backward-compatibility
- Low power consumption
- Fast, non-interlaced, flicker-free performance
- High resolution graphics

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Introduction

GENERAL DESCRIPTION

The IGA™ is a 1.2 micron, custom-designed, CMOS VLSI chip utilizing a RISC processor that implements all IBM PC family graphics modes on a single chip. These include CGA, MDA, Hercules, EGA, and VGA. The IGA chip has two program-selectable modes of operation: VGA and 8514/A. On power-up, the VGA mode is present with all its functions available for full program compatibility. The Advanced Graphics mode provides hardware assistance for complex drawing operations such as line drawing, area fill, bit-block transfer, scissoring, patterns, etc. The IGA supports a number of binary drawing modes that control the combination of color with existing pixel data, as well as simple Boolean operations such as REPLACE, AND, OR, and XOR. Arithmetic operations such as addition, subtraction, averaging, minimum, and maximum are also available. These functions provide the means for sophisticated image blending and control; operations that are performed much faster in hardware than in software, or with VGA alone.

FEATURE NOTES

- Single-chip, high-performance, video graphic solution for IBM PC/XT/AT and Personal System/2-compatible systems
- Fully supports IBM-compatible interfaces
- Fully compatible with VGA, EGA, CGA, MDA, and Hercules
- Fully comaptible with 8514/A
- 144 pin plastic QFP, 28 x 28 mm
- 1.2 Micron, custom-designed, CMOS VLSI technology
- Supports up to 65 MHz maximum video clock rate
- Supports interlaced or non-interlaced 640x480, 800x600, and 1024x768 pixels in 256 colors from a palette of 256K colors
- Supports 8- or 16-bit bus for IBM PC/XT/AT
- 16 KB RAM for scientific or foreign language applications
- Higher CPU-bus bandwidth (close to zero wait state)
- Hardware supports for drawing operations such as line draw, area fill, bit block transfer, scissoring, and patterns

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The IGA Chip

A Single-Chip Solution for 8514/A and VGA Graphics

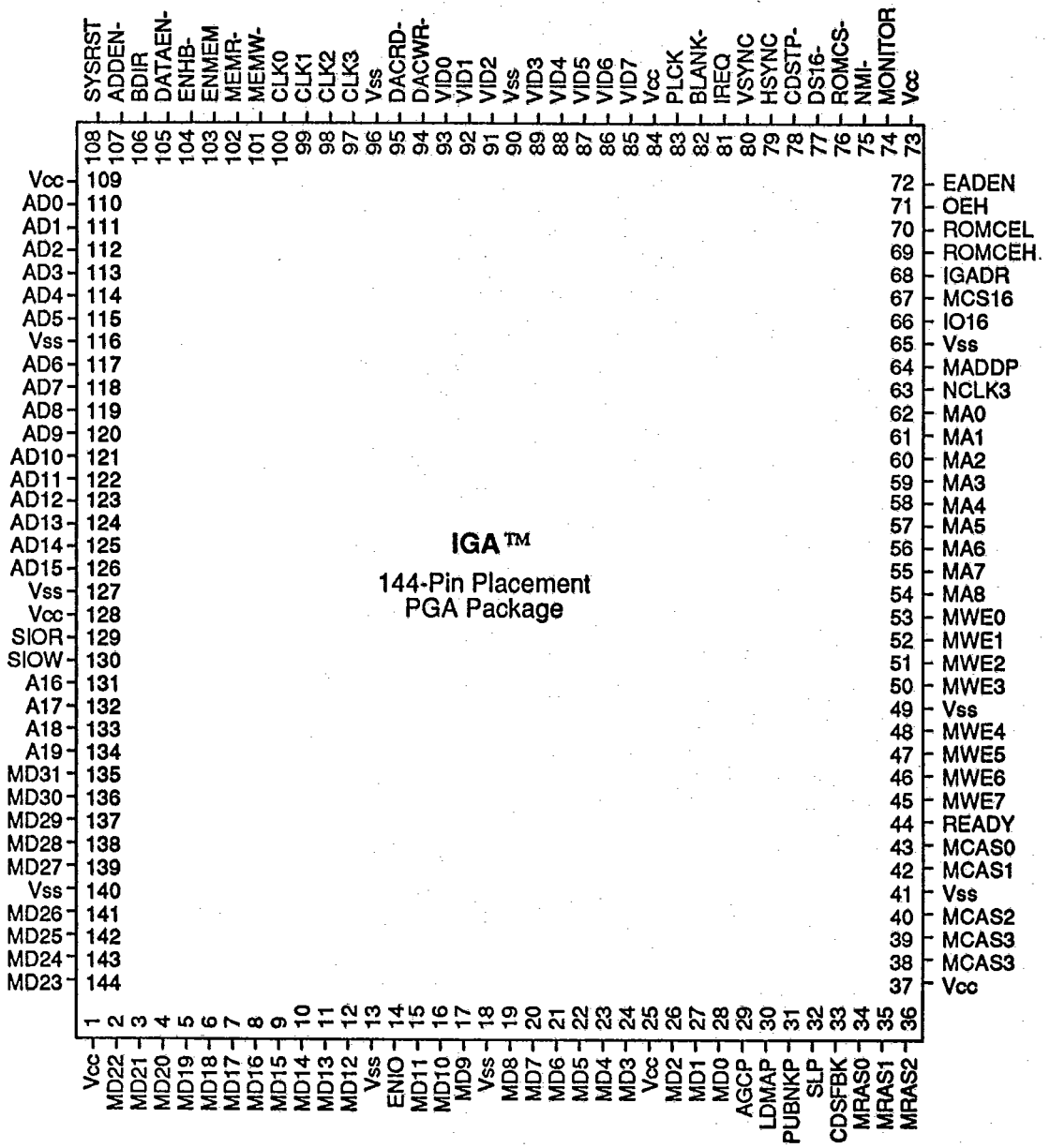

Figure 1. IGA Pin Diagram

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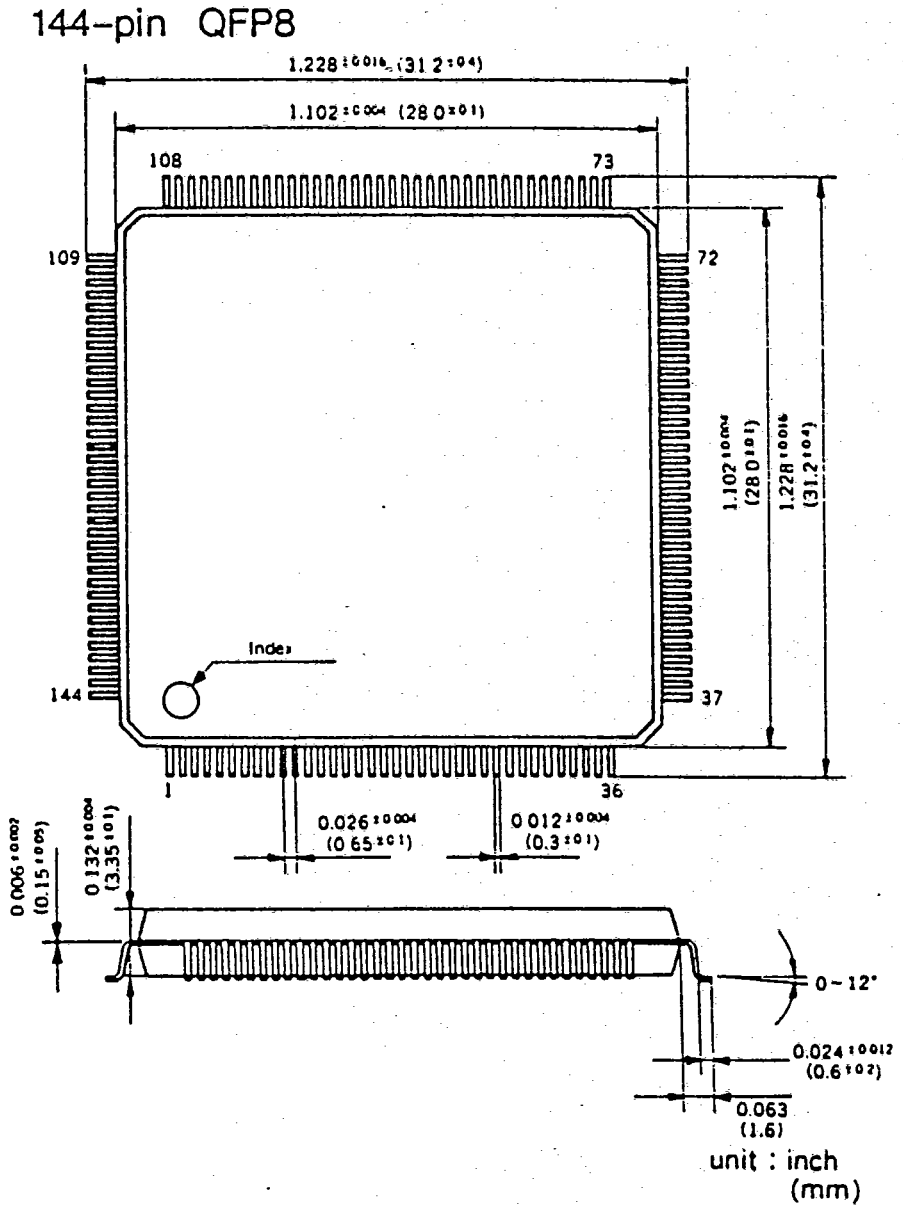
THE IGA QFP

This is the package that will be provided in the production version of the chip. The pin out is identical to that of Figure 1, Page 3.



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ABOUT THE DATA BOOK

This data book contains general information for the electrical and register specifications of the IGA as well as a summary of pin-out information and timing diagrams. This information is suffiecient for the IGA chip to be implemented on a board that can accommodate different IBM-compatible computer systems. The description of pin interfaces acts as a guide for choosing other components that are required to complete the board design.

The following IBM publication may be useful for the board designer: *IBM Personal System/2 Display Adapter 8514/A Technical Reference*, Publication No. 68x2248/S568X-2248-0, April 1987.

IGA ADVANTAGES

While fully emulating the IBM 8514/A chips that provide intelligent graphics functions (e.g., polygon drawing, polygon filling, and scissoring), the IGA also provides full VGA support in the same package, thus reducing the cost of development, cost of production, and cost to the end user.

Boards designed using the IGA are fully compatible with all the software applications that have been written for the IBM PC XT/AT and PS/2 compatibles.

Because the IGA is a single-chip solution, it requires only a single frame buffer and video DAC, rather than the two sets required by competitive solutions. Figure 2 illustrates how the IGA saves board space by reducing the number of components.

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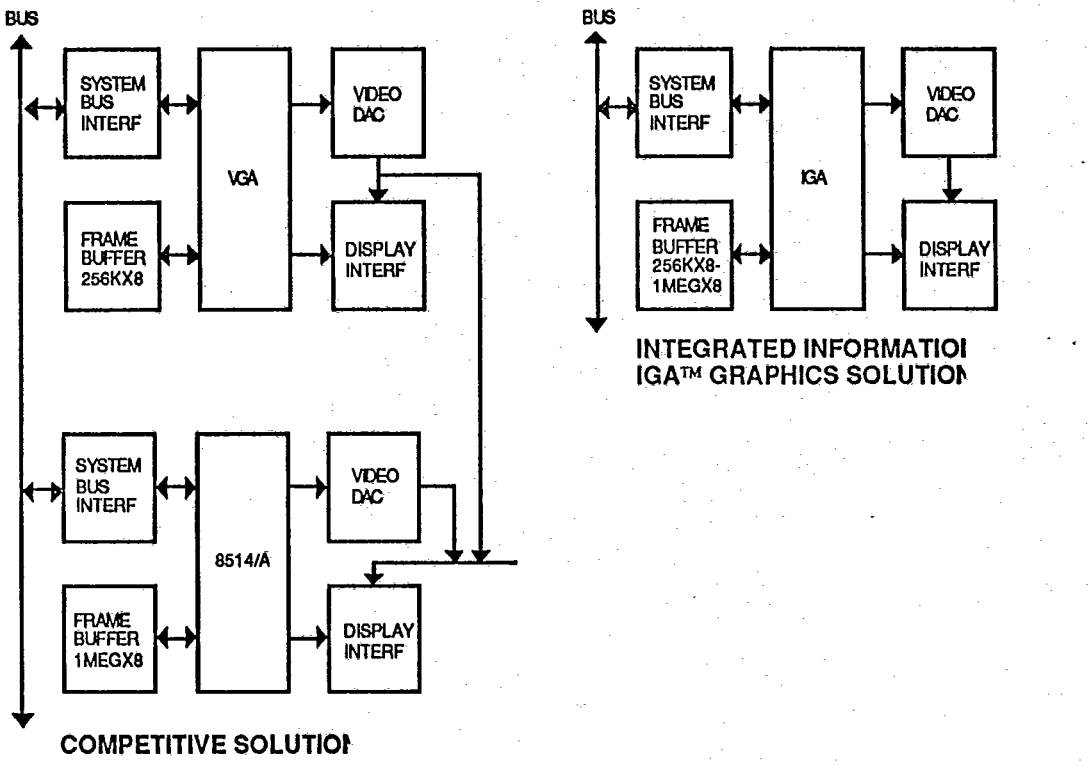

Figure 2. IGA vs. Competitive Solution

A board design using the IGA can be built on a single, half-size add-on board.

The IGA allows the chip designer to use inexpensive DRAM for the system frame buffer rather than the VRAM required by other designs.

Faster, non-interlaced flicker-free performance is made possible by the IGA's 65 MHz clock. In addition, the IGA supports all the standard IBM graphics modes: 640x480, 800x600, and 1024x768 with 256 colors out of a palette 256K colors.

For designers building graphics into a mother board, the IGA solution provides a complete and fully-compatible IBM PC graphics system.

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ARCHITECTURE

EXTERNAL BOARD FUNCTIONS

Figure 2 shows a typical IGA-based board compared to a solution in which the 8514/A and VGA capability are provided on separate chips. Each major element of an IGA-based board is discussed below.

The Frame Buffer (DRAM) block is the video memory subsystem. This is used to store screen images generated in the IGA (as a result of CPU drawing instructions) or image information sent to it by the CPU. Typically, information from the CPU restores previously drawn images that have been stored elsewhere is the system. The IGA reads image data to refresh the display screen. Drawing operations take place in a pixel coordinate space of 2K by 2K, which is identical to the 8514/A. The remaining DRAM storage is used by the IGA and CPU for "off-screen" use. This includes storage for fill patterns and scratchpad data.

In a typical board configuration, the IGA serializes, multiplexes, and forwards data to the DAC. The DAC, in turn, drives the RGB signals that perform the actual drawing on the monitor by generating analog intensity signals for the monitor's red, blue, and green (RGB) guns. The value of these signals is synchronized with pixel coordinates as the guns sweep horizontally across the screen. The value of the signals is determined by the pixel data that the IGA has read out of DRAM during screen refresh. External back-end support requires intelligence in the DAC to assist data formatting initiated in the serializing and multiplexing logic within the DRAM block.

The DAC also contains a color palette. This is a small memory that maps pixel data into values that are a combination of RGB intensities. Each cell in the palette memory represents a different color. For example, in a system having 256-colors, an eight-bit pixel selects one of 256 palette memory cells. Each of the cells has been previously loaded with an 18-bit word that is, in turn, divided into three 6-bit fields. These three fields represent red, blue and green signal intensities. In this manner, an 8-bit pixel is converted into a 24-bit color value. Palette values are loaded into the palette memory by the CPU.

The block representing the System Bus Interface contains bus transceivers and the TTL glue logic that interfaces the IGA chip to the system bus (either the IBM PS/2 Micro Channel, the IBM PC-AT bus, or other compatible buses). In addition, the block provides a data path through the IGA to the DAC. This permits the CPU to load 24-bit color values into the DAC as described above. The IGA also provides a path from the system bus to the Frame Buffer.

The remaining board elements (not shown) are the EPROM (containing BIOS extension firmware), clock generators, and other components such as pull-up/down resistors, logic, and DIP switches. DIP switches are used by the IGA to sense its environmental configuration: whether Micro Channel or AT bus, VRAM organization, etc.

Finally, the IGA contains a set of user-accessable internal registers that are compatible with those on an IBM 8514/A board. In the VGA mode, the chip configures itself for VGA operation. The registers and logic internal to the IGA are used to convert software commands from the CPU, and their parameters, into the signals required to drive the monitor.

IGA Internal Functional Description

As shown in Figure 3, the functional modules within the IGA are as follows: Host Interface/Interrupt, Graphics Controller, RISC Core, Decode, Attribute Controller, Instruction Fetch, Instruction Decoder, Microcode ROM, Display Memory Controller, and Video Timing Controller.

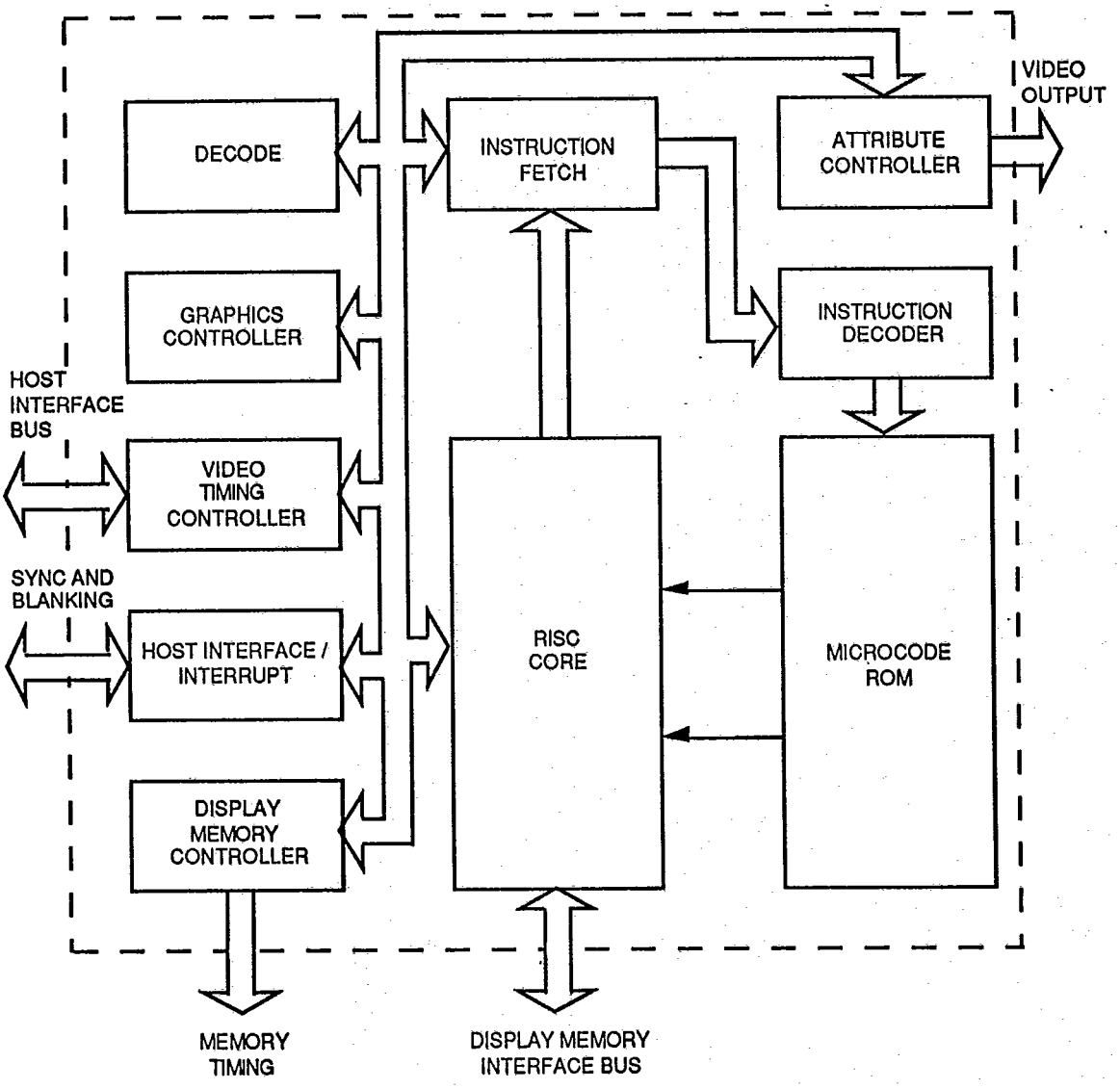

Figure 3. IGA Block Diagram

The Host Interface/Interrupt controls communication with the host interface bus and passes data to and from all the other units on the board.

The Graphics Controller performs drawing computations. It supports all 8514/A graphics mode and VGA mode operations. These include line drawing, fill area outline drawing, rectangle drawing, image transfer from the CPU, bit block copying, and scissoring. The Graphics Controller receives drawing instructions from the CPU via the Host Bus Interface and sends the pixel coordinates to the Display Memory Interface Bus.

The RISC Core is the computer internal to the IGA that controls all the operations required to emulate both the IBM 8514/A and VGA boards.

Decode interprets instructions sent by the system microprocessor.

The Attribute Controller takes in data from display memory by means of the Graphics Controller and the RISC core, then formats it for display.

Instruction Fetch is responsible for maintaining the flow of instructions from the CPU to the IGA.

The Instruction Decoder provides primary level decoding of the instructions fetched from the CPU. These instructions, in turn, drive the Microcode ROM.

The Microcode ROM provides a second level of instruction decoding that produces the microinstructions needed to drive the RISC Core computer.

The Display Memory Controller generates basic memory timings of the display memory RAMs.

The Video Timing Controller generates horizontal and vertical synchronous timings and refresh addressing for the display memory RAMs.

TEST CONSIDERATIONS

To make board testing easier, each output pin of the IGA may be disabled during Reset through the test strap pin (Bit 6 of the IAD bus).

When the test strap pin is held low, all output signals, with the exception of SLD, are tri-stated. SLD is tri-stated only if TSEL2 - TSEL0 are held high. Therefore, an in-circuit test of an IGA-based board requires that the test strap be held low at the same time as TSEL2 - TSEL0 is held high. Input pins that are normally bi-directional become output pins only. The pads for input and bi-directional pins have internal pull-up resistors. They are high if they are not driven low.

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IGA INTERFACE TO THE CPU

A path between the IGA interface pins and the IBM PS/2 Micro Channel or AT bus is provided by logic external to the IGA. The CPU is configured to either of the two bus types through the choice of the pin-strapping configuration.

Because either a PS/2 or AT bus configuration is possible, some of the CPU interface pins need to accommodate both configurations. Tables 1 and 2 provide descriptions of these pins as they correspond to IBM specifications for the Micro Channel or AT bus.

Name	IGA Pin #	I/O	Description
A16-A19 AD0-AD15	131-134 110-126	I	CPU address Bits 16 through 19, CPU address/data bits 0 - 15, Decoding of upper CPU address Bits 23-20, plus MADE24; all these should be 0 if the lower 20 bits of address are to be considered valid for the IGA based board
ENHB-	104	I	System Byte High Enable
SYSRST	108	I	Channel Reset
CDSTP	78	I	Card Setup
READY	44	O	Channel Reset
IREQ	81	O	Channel Ready
CDSFBK	33	O	Interrupt Request; tied to Micro Channel - IRQ 9
DS16	77	O	Card Selected Feedback
DATAEN	105	O	Data Bus Enable
BDIR	106	O	Data Bus Direction (high for CPU read, low for CPU write)

TABLE 1. MICRO CHANNEL – CPU INTERFACE PIN DESCRIPTIONS

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Name	PAM Pin #	I/O	Description
A16-A19	131-134	I	CPU address Bits 15 through 19
AD0-AD15	110-126	I	CPU Data bits 0 - 15
ENHB	104	I	System Bus High Enable
MEMR	102	I	Memory Read
MEMW	101	I	Memory Write
SIOR	129	I	I/O Read
SIOW	130	I	I/O Write
ADDEN	107	I	Address Buffer Enable
SYSRST	108	I	System Reset
READY	44	O	I/O Channel Ready
IREQ	81	O	Interrupt Request; tied to any AT bus interrupt line
IO16	66	O	I/O 16-bit Chip Select
DATAEN	105	O	Data Buffer Enable
BDIR	106	O	Data Bus Direction (high for CPU read, low for CPU write)

Table 2. AT Bus–CPU Interface Pin Descriptions

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DRAM Design and Interface

An IGA-based board can be configured with one of four DRAM designs. Each configuration can use two or three levels of chip population. Ten different configurations are possible. The design chosen depends upon the combination of criteria that is shown below. Only certain combinations are possible.

- Monitor resolution in pixels: 640x480, 1024x768, or 1280x1024
- Number of bits per pixel: 4 or 8 bits per pixel
- Number of screen pages: one or two
- Capacity of DRAM chips: 64Kx4 or 256Kx4
- Number of DRAM chips
- Requirement for future upgradeability
- Design Type:

  With back-end support (serializing and multiplexing of pixel data for screen refresh) integrated within the IGA;

  With external back-end support; support includes use of a more sophisticated DAC to achieve 1280x1024 resolution

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VIDEO DAC AND INTERFACE SUBSYSTEM

This section includes the following information for the board designer:

- Routing of DRAM pixel data to the video DAC
- Routing of control information from the IGA to the DAC and the monitor
- Palette access, with the board design option of implementing "flicker-free" mode

Note that a related topic, IGA recognition of monitor type, is grouped with other configuration strapping issues, and is discussed later in this chapter.

The IGA pins associated with the video interface subsystem and address decoding for 8514/A compatibility are shown in Table 3. The left-hand column, labeled bits, represents the hexadecimal value for bits 15-12 of the address. The top row represents the value in hexadecimal for the remaining twelve bits of the address. For example, read address A2E8 is decoded by looking at column 2E8, the last three characters, and going down the column to row A, where E2E8 is found. It should be noted that an I/O read from address A2E8 is the same as if read from address E2E8, the Pixel Data Transfer Register.

BITS 15-12/11-0	2E8	6E8	AE8	EE8H
0	2E8	2E8	2E8	2E8
1	2E8	2E8	2E8	2E8
2	2E8	2E8	2E8	2E8
3	2E8	2E8	2E8	2E8
4	42E8	42E8	42E8	42E8
5	42E8	42E8	42E8	42E8
6	42E8	42E8	42E8	42E8
7	42E8	42E8	42E8	42E8
8	83E8	86E8	0 *	0 *
9	92E8	0 *	9AE8	0 *
A	E2E8	E2E8	0 *	0 *
B	0 *	0 *	0 *	0 *
C	82E8	86E8	0 *	0 *
D	92E8	0 *	9AE8	0 *
E	E2E8	E2E8	0 *	0 *
F	0 *	0 *	0 *	0 *

* A value of zero will be read

Table 3. 8514/A Address Decoding for Read Operations

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Address decoding for a read is different from that of a write, as can be seen in Table 4.

BITS 15-12/11-0	2E8	6E8	AE8	EE8H
0	2E8	6E8	AE8	EE8
1	12E8	16E8	1AE8	1EE8
2	22E8	X	X	X
3	X	X	X	X
4	42E8	46E8	4AE8	X
5	42E8	46E8	4AE8	X
6	42E8	46E8	4AE8	X
7	42E8	46E8	4AE8	X
8	82E8	86E8	8AE8	8EE8
9	92E8	96E8	9AE8	9EE8
A	A2E8	A6E8	AAE8	AEE8
B	B2E8	B6E8	BAE8	BEE8
C	82E8	86E8	8AE8	8EE8
D	92E8	96E8	9AE8	9EE8
E	A2E8	A6E8	AAE8	AEE8
F	B2E8	B6E8	BAE8	BEE8

Table 4. 8514/A Address Decoding for Write Operations

When in wait-CPU-data-mode and the graphic engine is busy, registers A2E8, A6E8, E2E8, and E6E8 are the same as E2E8.

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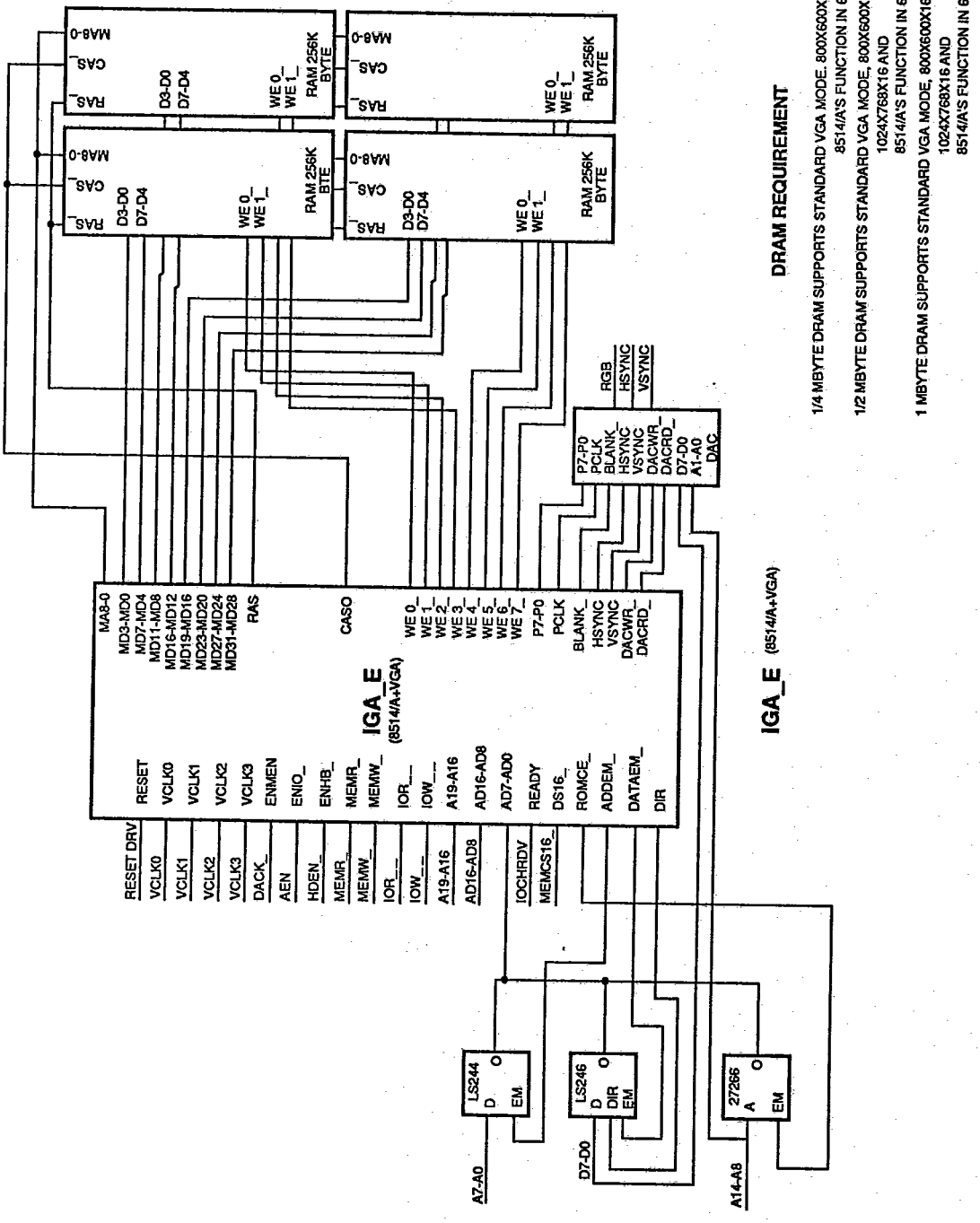

Figure 4. AT Bus Application

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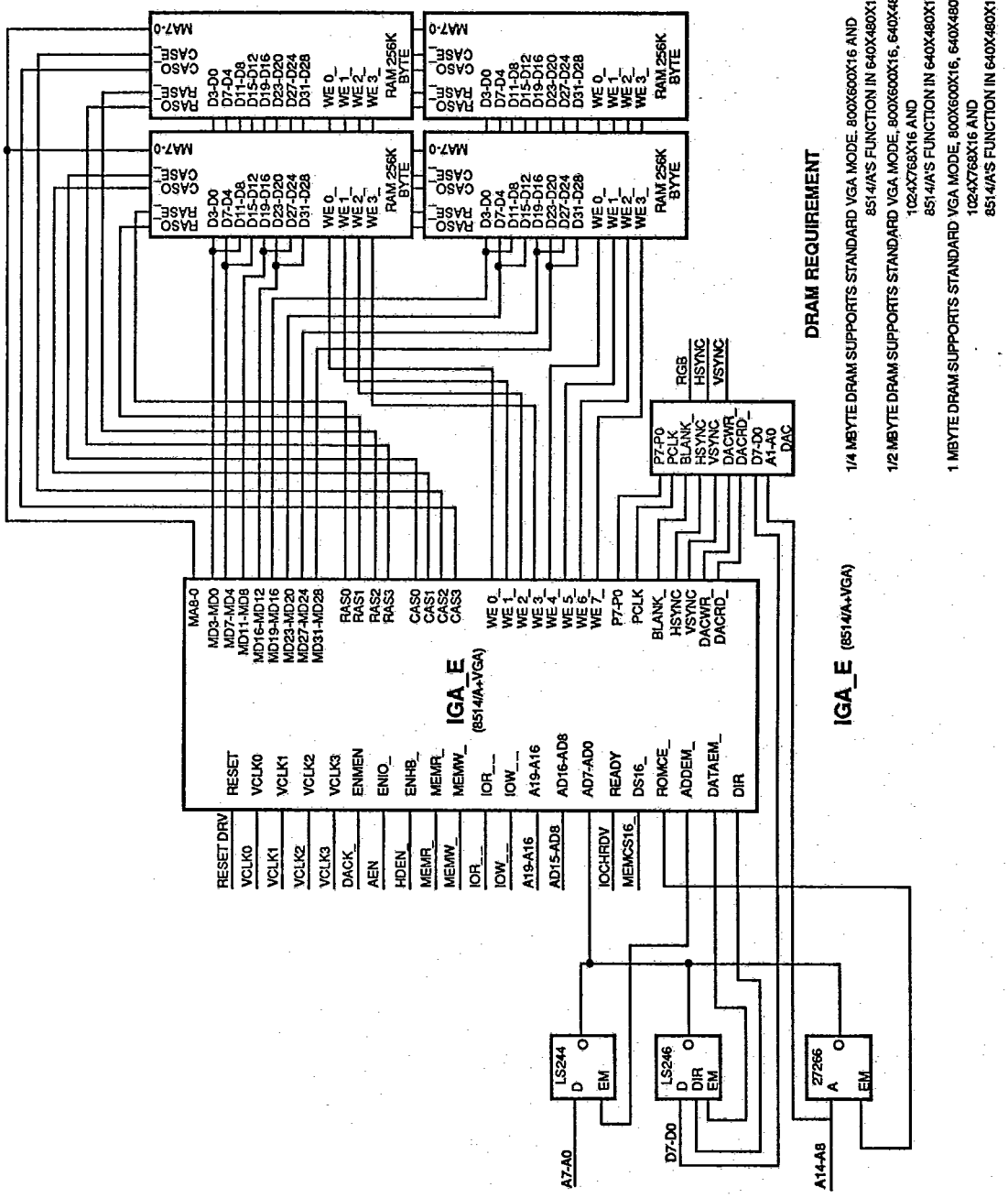

Figure 5. AT Bus Application

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Pad	Name	Type	Description	
1	VCC	-	+6.0 Volts	
2	MD22	Input/Output	Multiplexed display memory data bus,	bit-22
3	MD21	Input/Output	Multiplexed display memory data bus,	bit-21
4	MD20	Input/Output	Multiplexed display memory data bus,	bit-20
5	MD19	Input/Output	Multiplexed display memory data bus,	bit-19
6	MD18	Input/Output	Multiplexed display memory data bus,	bit-18
7	MD17	Input/Output	Multiplexed display memory data bus,	bit-17
8	MD16	Input/Output	Multiplexed display memory data bus,	bit-16
9	MD15	Input/Output	Multiplexed display memory data bus,	bit-15
10	MD14	Input/Output	Multiplexed display memory data bus,	bit-14
11	MD13	Input/Output	Multiplexed display memory data bus,	bit-13
12	VSS	-	Ground	
13	MD12	Input/Output	Multiplexed display memory data bus,	bit-12
14	ENIO-	Input	Enable Input/Output	
15	MD11	Input/Output	Multiplexed display memory data bus,	bit-11
16	MD10	Input/Output	Multiplexed display memory data bus,	bit-10
17	MD9	Input/Output	Multiplexed display memory data bus,	bit-9
18	VSS	-	Ground	
19	MD8	Input/Output	Multiplexed display memory data bus,	bit-8
20	MD7	Input/Output	Multiplexed display memory data bus,	bit-7
21	MD6	Input/Output	Multiplexed display memory data bus,	bit-6
22	MD5	Input/Output	Multiplexed display memory data bus,	bit-5
23	MD4	Input/Output	Multiplexed display memory data bus,	bit-4
24	MD3	Input/Output	Multiplexed display memory data bus,	bit-3
25	VCC	-	+6.0 Volts	
26	MD2	Input/Output	Multiplexed display memory data bus,	bit-2
27	MD1	Input/Output	Multiplexed display memory data bus,	bit-1
28	MD0	Input/Output	Multiplexed display memory data bus,	bit-0
29	AGCP	Input	8514/A Mode selection	
30	LDMAP-	-	N/C - Reserved	
31	PUBNKP	-	N/C - Reserved	
32	SLP	-	N/C - Reserved	
33	CDSFBK-	Input	Graphic Card Selection Feedback	
34	MRAS0-	Input	Row Address Strobe - Map 0	
35	MRAS1-	Input	Row Address Strobe - Map 1	
36	MRAS2-	Input	Row Address Strobe - Map 2	

Table 5. Connector Pad List for IGA

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Pad	Name	Type	Description	
37	VCC		+6.0 Volts	
38	MRAS3-	Input	Row Address Strobe - Map 3	
39	MCAS3-	Input	Column Address Strobe - Map 3	
40	MCAS2-	Input	Column Address Strobe - Map 2	
41	VSS		Ground	
42	MCAS1-	Input	Column Address Strobe - Map 1	
43	MCAS0-	Input	Column Address Strobe - Map 0	
44	READY	Output	Input/Output Channel Read	
45	MWE7-	Input	WE Enable - Map 7	
46	MWE6-	Input	WE Enable - Map 6	
47	MWE5-	Input	WE Enable - Map 5	
48	MWE4-	Input	WE Enable - Map 4	
49	VSS		Ground	
50	MWE3-	Input	WE Enable - Map 3	
51	MWE2-	Input	WE Enable - Map 2	
52	MWE1-	Input	WE Enable - Map 1	
53	MWE0-	Input	WE Enable - Map 0	
54	MA8	Output	Display Memory Muxed Address Bus	bit - 8
55	MA7	Output	Display Memory Muxed Address Bus	bit - 7
56	MA6	Output	Display Memory Muxed Address Bus	bit - 6
57	MA5	Output	Display Memory Muxed Address Bus	bit - 5
58	MA4	Output	Display Memory Muxed Address Bus	bit - 4
59	MA3	Output	Display Memory Muxed Address Bus	bit - 3
60	MA2	Output	Display Memory Muxed Address Bus	bit - 2
61	MA1	Output	Display Memory Muxed Address Bus	bit - 1
62	MA0	Output	Display Memory Muxed Address Bus	bit - 0
63	NCLK3	Input	Clock Input	
64	MADDP			
65	VSS		Ground	
66	IO16	Input	16 Bit Memory Transfer, Low Active	
67	MCS16	Input	16 Bit memory Transfer, Low Active	
68	IGADR	Input	IGA Data Direction	
69	ROMCEH	Input	BIOS ROM Select High	
70	ROMCEL	Input	BIOS ROM Select Low	
71	OEH	Input	Output Enable High, Low Active	
72	EADEN	Input	Address Enable, Low Active	

Table 5. Connector Pad List for IGA (Continued)

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Pad	Name	Type	Description
73	VCC	-	+6.0 Volts
74	MONITOR	Input	Monitor Type Detector
75	NMI-	Output	Non Maskable Interrupt
76	ROMCS	Output	BIOS EPROM Chip Select
77	DS16-	Output	Enable 16 Bit Master
78	CDSTP-		Graphic Card Set Up
79	VSYNC	Output	Vertical Synchronization Pulse
80	HSYNC	Output	Horizontal Synchronization Pulse
81	IREQ	Output	Interrupt Request
82	BLANK-	Output	Blank Output
83	PCLK	Output	Pixel Clock Output
84	VCC	-	+6.0 Volts
85	VID7	Output	Video DAC Pixel Address bit-7
86	VID6	Output	Video DAC Pixel Address bit-6
87	VID5	Output	Video DAC Pixel Address bit-5
88	VID4	Output	Video DAC Pixel Address bit-4
89	VID3	Output	Video DAC Pixel Address bit-3
90	VCC	-	+6.0 Volts
91	VID2	Output	Video DAC Pixel Address bit-2
92	VID1	Output	Video DAC Pixel Address bit-1
93	VID0	Output	Video DAC Pixel Address bit-0
94	DACWR-	Output	DAC Write Strobe
95	DACRD-	Output	DAC Read Strobe
96	VSS	-	Ground
97	CLK3	Input	CLOCK
98	CLK2	Input	CLOCK
99	CLK1	Input	CLOCK
100	CLK0	Input	CLOCK
101	MEMW-	Input	Memory Write Strobe
102	MEMR-	Input	Memory Read Strobe
103	ENMEM	Input	Enable Display Memory
104	ENHB-	Input	Enable Bus High Byte
105	DATAEN-	Output	Data Buffer Enable
106	BDIR	Output	Read Cycle Data Buffer Direction Control
107	ADDEN-	Output	Address Buffer Enable
108	SYSRST	Input	System Reset

Table 5. Connector Pad List for IGA (Continued)

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Pad	Name	Type	Description
109	VCC	-	+6.0 Volts
110	AD0	Input/Output	Multiplexed Address and Data bit-0
111	AD1	Input/Output	Multiplexed Address and Data bit-1
112	AD2	Input/Output	Multiplexed Address and Data bit-2
113	AD3	Input/Output	Multiplexed Address and Data bit-3
114	AD4	Input/Output	Multiplexed Address and Data bit-4
115	AD5	Input/Output	Multiplexed Address and Data bit-5
116	VSS	-	Ground
117	AD6	Input/Output	Multiplexed Address and Data bit-6
118	AD7	Input/Output	Multiplexed Address and Data bit-7
119	AD8	Input/Output	Multiplexed Address and Data bit-8
120	AD9	Input/Output	Multiplexed Address and Data bit-9
121	AD10	Input/Output	Multiplexed Address and Data bit-10
122	AD11	Input/Output	Multiplexed Address and Data bit-11
123	AD12	Input/Output	Multiplexed Address and Data bit-12
124	AD13	Input/Output	Multiplexed Address and Data bit-13
125	AD14	Input/Output	Multiplexed Address and Data bit-14
126	AD15	Input/Output	Multiplexed Address and Data bit-15
127	VSS	-	Ground
128	VCC	-	+6.0 Volts
129	SIOR-	Input	Input/Output Read Strobe
130	SIOW-	Input	Input/Output Write Strobe
131	A16	Input	Address Bus bit-16
132	A17	Input	Address Bus bit-17
133	A18	Input	Address Bus bit-18
134	A19	Input	Address Bus bit-19
135	MD31	Input/Output	Display Memory Muxed Address Bus bit-31
136	MD30	Input/Output	Display Memory Muxed Address Bus bit-30
137	MD29	Input/Output	Display Memory Muxed Address Bus bit-29
138	MD28	Input/Output	Display Memory Muxed Address Bus bit-28
139	MD27	Input/Output	Display Memory Muxed Address Bus bit-27
140	VSS	-	Ground
141	MD26	Input/Output	Display Memory Muxed Address Bus bit-26
142	MD25	Input/Output	Display Memory Muxed Address Bus bit-25
143	MD24	Input/Output	Display Memory Muxed Address Bus bit-24
144	MD23	Input/Output	Display Memory Muxed Address Bus bit-23

Table 5. Connector Pad List for IGA (Continued)

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VGA OPERATION

VGA Text Mode

Mode	Resolution	Char Box	Col x Row	Board	Colors
0,1	320x200	8x8	40x25	CGA	16
	320x350	8x14	40x25	EGA	16/64
	320x400	8x16	40x25	MCGA	16/256K
	360x400	9x16	40x25	VGA	16/256K
2,3	640x200	8x8	80x25	CGA	16
	640x350	8x14	80x25	EGA	16/64
	640x400	8x16	80x25	MCGA	16/256K
	720x400	9x16	80x25	VGA	16/256K
7	720x350	9x14	80x25	MDA	MON
	720x350	9x14	80x25	EGA	MON
	720x400	9x16	80x25	VGA	MON
	1056x344	8x8	132x43	IGA	MON
	1180x350	9x14	132x25	IGA	MON

Table 6. IIT-IGA VGA-Compatible Graphic and Text Mode

VGA Graphic Mode

Mode	Resolution	Board	Colors
4,5	320x200	CGA	4
		EGA	4/64
		MCGA	4/256K
		VGA	4/256K
6	640x200	CGA	2
		EGA	2/64
		MCGA	2/256K
		VGA	2/256K
D	320X200	EGA	16/64
		VGA	16/256

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E	640x200	EGA	16/64
		VGA	16/256K
F	640x350	EGA	MON
		VGA	MON
10	640x350	EGA	16/64
		VGA	16/256K
11	640x480	MCGA	2/256K
		VGA	2/256K
12	640x480	VGA	16/256K
13	320x200	MCGA	256/256K
		VGA	256/256K
IGA	640x480	IGA	256/256K
IGA	800x600	IGA	256/256K
IGA	1024x768	IGA	16/256K
IGA	1024x768	IGA	256/256K
HER	720x348	HERCULES	MON

Table 7. IIT-IGA Operation Modes

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8514/A OPERATION

Command	Action
HLINE	Draws absolute polygon starting at absolute position
HCLINE	Draws absolute polygon starting at current position
HRLINE	Draws relative polygon starting at absolute position
HRCLINE	Draws relative polygon starting at current position
HBAR	Begins filled area
HEAR	Ends filled area
HRECT	Draws filled rectangle
HMRK	Draws a marker symbol at absolute position
HCMRK	Draws a marker symbol at current position
HBBW	Defines Bit-BLT destination at absolute position
HCBBW	Defines Bit-BLT destination at current position
HBBR	Defines Bit-BLT source at absolute position
HOPEN	Opens the display adapter interface
HCLOSE	Closes the display adapter interface
HSCP	Moves to absolute location
HQCP	Inquires about current position
HQDFPAL	Inquires about default palette
HINIT	Initializes task-dependent state buffer
HSYNC	Sets adapter to a task-dependent state
HINT	Waits for a vertical retrace
HSMODE	Set display adapter mode
HQMODE	Inquires about display adapter mode
HQMODES	Inquires if display adapter modes are available
HEGS	Clears screen to zero
HSGQ	Sets graphics quality/drawing styles
HSHS	Sets scissor
HIDPAL	Loads palette
HSPAL	Saves palette

Table 8. Advanced Graphic Mode Commands

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Command	Action
HIRPAL	Restores palette
HSLPC	Saves line pattern position
HRLPC	Restores line pattern position
HSBP	Sets bit plane controls
HQCOORD	Inquires about coordinate types
HSCOORD	Sets coordinate types
HESC	Escapes
HQDPS	Inquires about drawing process state buffer size
HSMARK	Sets current marker shape
HSPATT	Sets current pattern shape
HSPATTO	Sets current pattern origin point
HSLT	Sets current line type
HSLW	Sets current line width
HSCOL	Sets current foreground color
HSBCOL	Sets current background color
HSMX	Sets mix
HSCMP	Sets color comparison register
HSCS	Sets character set
HCHST	Draws text string at absolute position
HXLATE	Assigns color index table for text
ABLOCKMFI	Writes alphanumeric character block
ABLOCKCGA	Writes CGA-format alphanumeric character block
AERASE	Erases character cell rectangle
ASCROLL	Scrolls character cell rectangle
ACURSOR	Sets alphanumeric cursor position
ASCUR	Sets alphanumeric cursor shape
ASFONT	Sets alphanumeric character set
AXLATE	Sets alphanumeric attribute color index table

Table 8. Advanced Graphic Mode Commands (Continued)

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ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (V_{SS} = OV)

Symbol	Parameter	Value MIN	MAX	Units
I_{IN}	Input current	-10	10	µA
I_{OUT}	Output current	-10	10	mA
PD	Power dissipation		1.5	W
T_A	Ambient temperature under bias	0°	70°	C
T_{STG}	Storage temperature	-65°	150°	C
V_{CC}	Power Supply Voltage	V_{SS} -0.5	6.0	V
V_{IN}	Input Voltage	V_{SS} -0.5	V_{OO} +0.5	V

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

IIT-IGA Characteristics (V_{CC} = 5V + /- 5%, T_A = 0 to 70° C)

Recommended Operating Conditions (V_{SS} = 0 V)

Symbol	Parameter	Value MIN	MAX	Units
V_{IN}	Input voltage	V_{SS}	V_{OO}	V
T_{OPR}	Operating temperature	0°	70°	C
V_{OO}	Power supply voltage	4.75	5.25	V

Electrical Characteristics (V_{SS} = 0 V)

Symbol	Parameter	Condition	Value MIN	MAX	Units	Notes
V_{CC}	Power supply current	f Max = 50 MHZ		200	mA	no DC Loads
I_{DDS}	Standby current	V_{DC} = MAX		10	µA	
I_L	Input leakage		-1	+1	µA	
I_H	Input high current	V_{IN} = V_{CC}		10	µA	
I_{L1}	Input low current	V_{IN} = OV	-100		µA	pull-up.
I_{L2}	Special input low current	V_{IN} = OV		-10	µA	no pull-up
V_{IN}	Input voltage high	V_{IDO} = 5.25	2.0		V	
V_{IL}	Input voltage low			.08	V	
V_{OH}	Output voltage high	I_{CH} = 2,4,8 mA	2.4		V	
V_{OL}	Output voltage low	I_{OL} = 4,6,8 mA V_{DC} = 4.75	2.4	V_{SS} +0.4	V	
V_{SK}	Input voltage skew			2	V/ns	

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TIMING SPECIFICATIONS

IIT-IGA AC Characteristics (V_{CC} = 5V + 5%, T_A = 0 to 70°C)

		Value				
Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t_1	Address Set-up time to -CMD	15	-	-	ns	7
t_2	CMD pulse width	-	180	-	ns	7
t_3	Read data valid from -CMD	-	-	135	ns	7
t_4	Write data set-up time from READY	-	120	-	ns	7
t_5	Read data hold time	-	0	-	ns	7
t_6	Write data hold time	5	-	-	ns	7
t_7	ADDEN hold time to -CMD active	9	15	20	ns	
t_8	DATAEN hold time to -CMD active	9	15	20	ns	
t_9	DS16 active from address valid	10	17	24	ns	8
t_{10}	BDIR valid from read CMD active	8	13	19	ns	
t_{11}	READY active from -CMD active	12	18	30	ns	
t_{12}	ADDEN active from -CMD inactive	10	16	20	ns	
t_{13}	DATAEN hold time from -CMD	10	16	22	ns	
t_{14}	DS16 hold time from address invalid	8	17	24	ns	
t_{15}	BDIR hold time to -CMD inactive	10	24	20	ns	
t_{16}	Address AD0"15 setup to -CMD active	5	-	-	ns	1
t_{17}	Address AD0'15 hold to -CMD active	5	-	-	ns	
t_{18}	ENHB.A16"19 setup to -CMD active	5	-	-	ns	
t_{19}	Address AD0"15 hold from -ADDEN	5	-	-	ns	
t_{20}	read Data (AD0"15) delay from -CMD	35	-	-	ns	2b
t_{21}	Read Data (AD0"15) hold from -CMD	-	-	0	ns	2b
t_{22}	Write Data (AD0"15) setup from -CMD	15	-	-	ns	2a
t_{23}	Write Data (AD0"15) hold from -CMD	2	-	-	ns	2a
t_{24}	DACWR delay from -IOW/write cmd active	10	14	40	ns	
t_{25}	ACWR delay from -IOW/write cmd active	10	16	22	ns	
t_{26}	-DACRD delay from -IOr/read cmd active	11	14	20	ns	
t_{27}	DACRD delay from -IOr/read cmd active	10	16	22	ns	
t_{28}	P0"P7 pixel word setup to PCLK	3	-	-	ns	6
t_{29}	P0"P7 pixel word hold from PCLK	t6-t62-4	-	ns	6	
t_{30}	Blank setup to PCLK	1	-	-	ns	
t_{31}	Blank hold from PCLK	3	-	-	ns	
t_{32}	Sync setup to PCLK	6	-	-	ns	
t_{33}	Sync hold from PCLK	10	-	-	ns	
t_{34}	Reset pulse width	128 tc	-	-	ns	
t_{35}	MEMEM setup to -MEMR	10	-	-	ns	
t_{36}	MEMEM hold from -MEMR inactive	10	-	-	ns	
t_{37}	ENIO setup to -IOCMD	15	-	-	ns	
t_{38}	ENIO hold from -IOCMD inactive	10	-	-	ns	
t_{39}	MONITOR setup to -IOR/read command	50	-	-	ns	
t_{40}	MONITOR hold to -IOR/read cmd active	1-	-	-	ns	

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TIMING SPECIFICATIONS (CONTINUED)

Symbol	Parameter	MIN	TYP	MAX	Units	Notes
t41	Video vertical blank period					4
t42	Active vertical video period					4
t43	Video display end to VSYNC					4
t44	VSYNC interval					4
t45	Video Sync pulse width					4
t46	IREQ active from VSYNC	10	-	25	ns	
t47	IREQ inactive from -IOW/write command	30	-	40	ns	
t48	NMI active from -IOW/write command	-	14	20	ns	
t49	NMI inactive from -IOW/write command	-	16	22	ns	
t50	ROMCS active from -MEMR	10	-	19	ns	
t51	Video horizontal blank period					5
t52	Active horizontal video period					5
t53	Horizontal display end to HSYNC					5
t54	HSYNC end to active video period					5
t55	HSYNC interval					5
t56	HSYNC period					5
t57	HSYNC interval					5
t58	PCLK slew from VCLK	4	-	20	ns	
t59	DS16 from IOW	6	17	22	ns	9
t60	ROMCS from valid address	12	22	30	ns	
t61	PCLK high time	tch-4	-	-	ns	
t62	PCLK low time	tcl-1	-	-	ns	
t63	CMD active period	3tc	-	-	ns	3
t64	READY pulse width	4tc	-	128tc	ns	
t65	Read data setup to READY	25	-	-	ns	
t66	Read data delay time	-	-	3tc+30	ns	
fc	VCLK 0-3 input clock frequency			50	MHz	
tc	VCLK 0-3 input clock period	20			ns	
tch	VCLK 0-3 high time	tc/2+/-5%		ns		
tcl	VCLK 0-3 low time	tc/2+/-5%		ns		

Notes:

1. Address A0"A15 must be valid 10 ns before -CMD goes inactive.
2a. WRCMD can be either -IOW or valid S0, S1, MIO lines indicating -IOW.
2b. RDCMD can be either -IOW or valid S0, S1, MIO lines indicating -IOR.
3. The -CMD pulse width indicated is a recommended minimum, the VGA control may work with a lesser pulse period.
4. See VSYNC timing table below.

VSYNC	350 Lines	400 Lines	480 Lines	600 Lines
t41	2.768 mS	1.112 mS	0.922 mS	0.72 mS
t42	11.504 mS	13.156 mS	15.762 mS	17.07 mS
t43	0.985 mS	0.159 mS	0.064 mS	0.030 mS
t44	14.258 mS	14.258 mS	15.583 mS	17.75 mS
t45	0.064 mS	0.064 mS	0.064 mS	0.06 mS

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TIMING SPECIFICATIONS (CONTINUED)

5. See HSYNC timings table below.

HSYNC	40/80 no border	80 with border	800-pixel graphics
t51	6.356 µS	5.720 µS	6.23 µS
t52	24.422 µS	25.068 µS	22.22 µS
t53	0.636 µS	0.318 µS	0.67 µS
t54	1.907 µS	1.589 µS	3.56 µS
t55	3.813 µS	3.813 µS	2.00 µS
t56	31.778 µS	31.778 µS	28.44 µS
t57	3.813 µS	3.813 µS	1.00 µS

6. PCLK can be inverted externally to improve t26 and t29 timings.
   $T26(improved) = t26 + t61 \cdot t_{delay}(inverted) \cdot t28(improved) - t_{gc} - t_{delay}(inverted) - t29.$
7. These timing numbers are meant only as a general reference: timing numbers t1 to t6 may vary depending upon system implementations. Do not use these numbers as a basis for designing systems.
8. DS16 is active only during CPU memory cycles and is inactive during CPU I/O cycles.
9. DS16 active time when I/O register is written to enable -DS16.

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IIT-IGA DRAM TIMING

Symbol	Parameter	8-dot Mode Min		9-dot Mode Min	
			Max		Max
t_{rc}	Read/Write cycle time	6tc	-	7tc	-
t_{ras}	RAs pulse width	3.5tc	-	4tc+2tt	-
t_{ar}	Column address hold from RAS	2tc	-	2tc	-
t_{rp}	RAS precharge	2.5tc	-	3.5tc	-
t_{crp}	CAS to RAS precharge	2.5tc	-	3.5tc	-
t_{csh}	CAS hold from RAS	3.5tc	-	3.5tc	-
t_{rsh}	RAS hold from CAS	2tc-2tt	-	2tc-2tt	-
t_{cpn}	CAS precharge	4tc-tt	-	6tc-tt	-
t_{cas}	CAS pulse width	2tc-2tt	-	2tc-2tt	-
t_{asr}	Row address setup to RAS	0.5tc	-	0.5tc	-
t_{asc}	Column address hold from CAS	0.5tc	-	0.5tc	-
t_{rs}	Row address hold from RAS	0.5tc	-	0.5tc	-
t_{cs}	Column address hold from RAS	0.5tc	-	0.5tc	-
t_{dsc}	Read data setup to CAS inactive	7ns	-	7ns	-
t_{off}	Read data hold to CAS inactive	0ns	-	0ns	-
t_{wp}	WE pulse width	2.5tc	-	2.5tc	-
t_{ds}	Write data setup to CAS	tc-10	-	tc-10	-
t_{dh}	Write data hold from CAS	1.5tc	-	1.5tc	-
t_{dhr}	Write data hold from RAS	3tc	-	3tc	-
t_{wct}	WE hold from RAS	3.5tc	-	1tc	-
t_{wcs}	Write command setup time	0.5tc-tt	-	0.5tc-tt	-
t_{wch}	Write command setup time	2tc	-	2tc	-
t_{rcd}	RAS to CAS delay	1.5 tc	-	1.5tc	

Notes:
tc = 1 input clock frequency.
All DRAM timings are listed at a maximum clock rate of 20 MHz during production.
Timing numbers guaranteed by design, not tested.

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IIT-VGA DRAM TIMING (High Bandwidth Mode)

Symbol	Parameter	Value MIN	MAX	Units	Notes
t_{ic}	Read/Write cycle time	6tc	19tc	ns	1
t_{cas}	RAS pulse width	17tc-2tt	-	ns	
t_{ca}	Column address hold from RAS	2tc	-	ns	2,6
t_{cp}	RAS precharge	2..5tc	-	ns	2
t_{crh}	CAS hold from RAS	2.5tc	-	ns	2
t_{rch}	RAS to CAS delay	3.5tc	-	ns	
t_{crh}	RAS hold from CAS	2tc-2tt	-	ns	2
t_{cpn}	CAS precharge	2tc-2tt	-	ns	2
t_{cpw}	CAS pulse width	2tc-2tt	-	ns	
t_{rra}	Row address setup to TAS	0.5tc-tt	-	ns	2
t_{aac}	Column Address setup to CAS	tc-tt	-	ns	
t_{ra}	Row address hold from RAS	0.5tc-tt	-	ns	2
t_{cad}	Column address hold from CAS	0.5tc-tt	-	ns	6
t_{rds}	Read data setup to CAS inactive	7	-	ns	3
t_{rdh}	Read data hold to CAS inactive	0	-	ns	3
t_{wp}	WE pulse width	2.5tc	-	ns	4
t_{ds}	Write data setup	tc-10	-	ns	4
t_{dh}	Write data hold from CAS	1.5tc	-	ns	4
t_{dhr}	Write data hold from RAS	3tc	-	ns	4
t_{wcs}	Write command setup time to CAS	0.5tc-tt	-	ns	4
t_{wch}	Write Command hold time from CAS	2tc	-	ns	4
t_{wce}	WE hold from RAS	3.tc	-	ns	4

IIT-VGA DRAM TIMING (RAS-ONLY REFRESH)

t_{hde}	Horizontal display enable inactive to RAS only refresh delay	16/18tc	-	ns[8-dot/9-dot]
t_{rpw}	RAS pulse width	3.5tc	-	ns
t_{rp}	RAS precharge	2.5tc	-	ns
t_{ast}	Row address setup time	0.5tc	-	ns
t_{ht}	Row address setup time	tc	-	ns

tt = minimum (3 ns) transition time

tc = clock period

Notes:

1. Minimum time indicated is for non-page mode, 8-dot cycle.
   Maximum time indicated is for page mode cycle (CRT read cycle).
2. These timings are more relaxed in page mode operation and minimum times are controlled by 8-dot cycle timings.
3. Read cycle timings are similar to 8-dot cycle timings.
4. Write cycle is not a page mode cycle, hence timings indicated are 8-dot cycle timings.
5. All DRAM timings are listed at a maximum clock rate of 20 MHz during production.
6. Timing numbers are guaranteed by design, and are not tested.

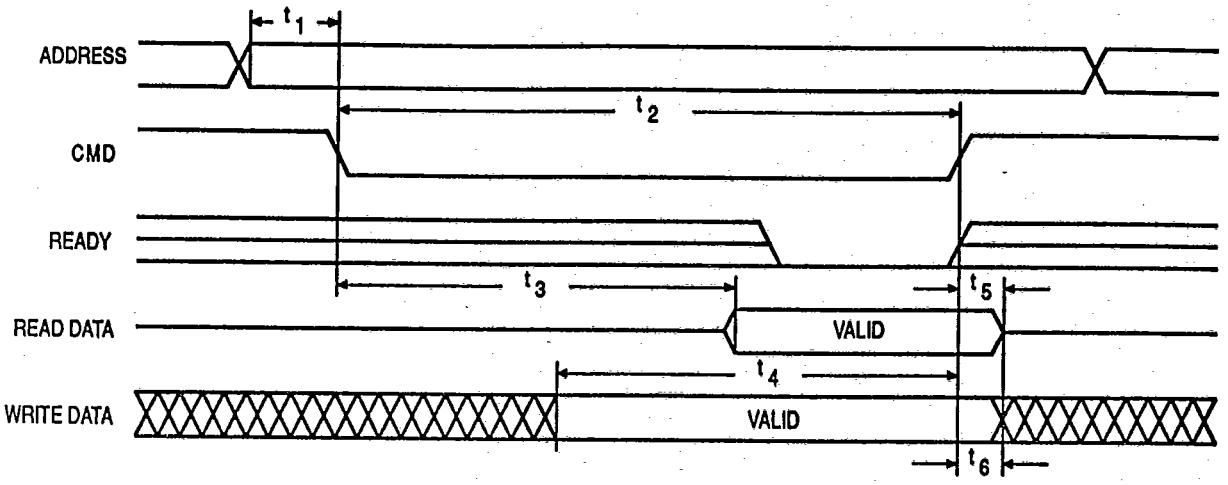

Figure 6. PC XT/AT Bus Cycle Timing

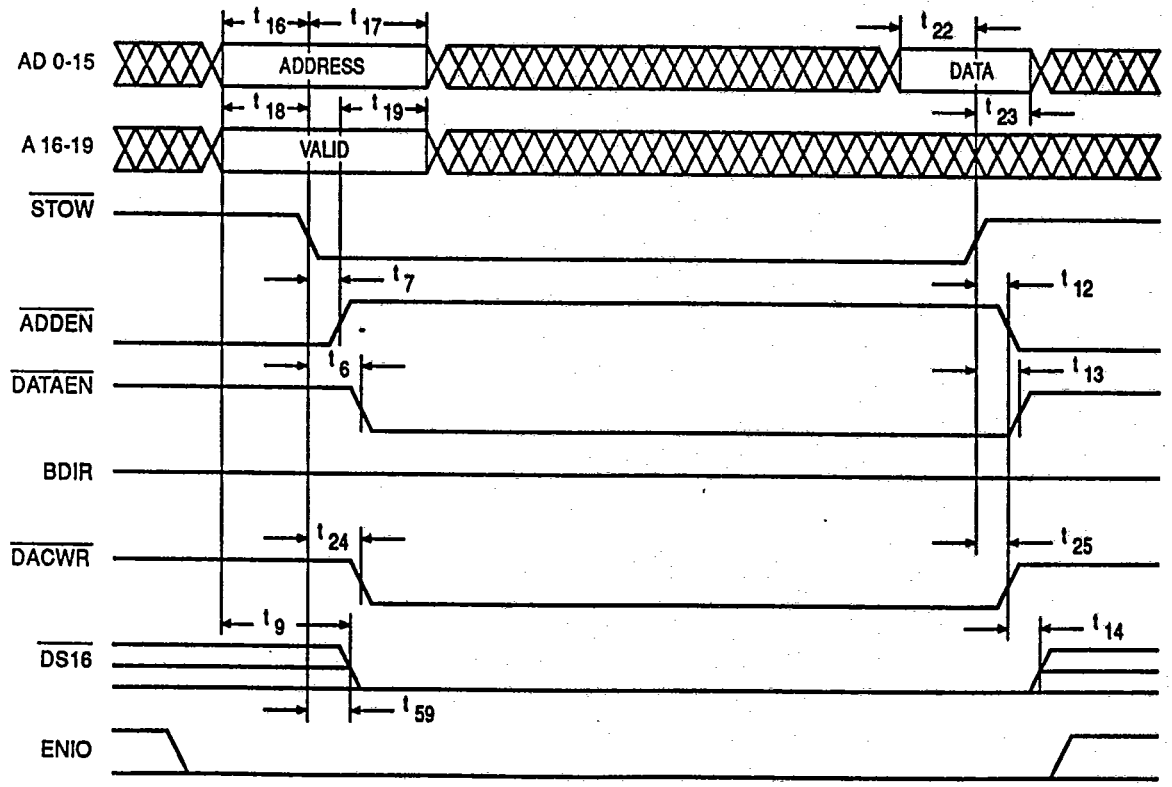

Figure 7. AT Mode I/O Write Timing

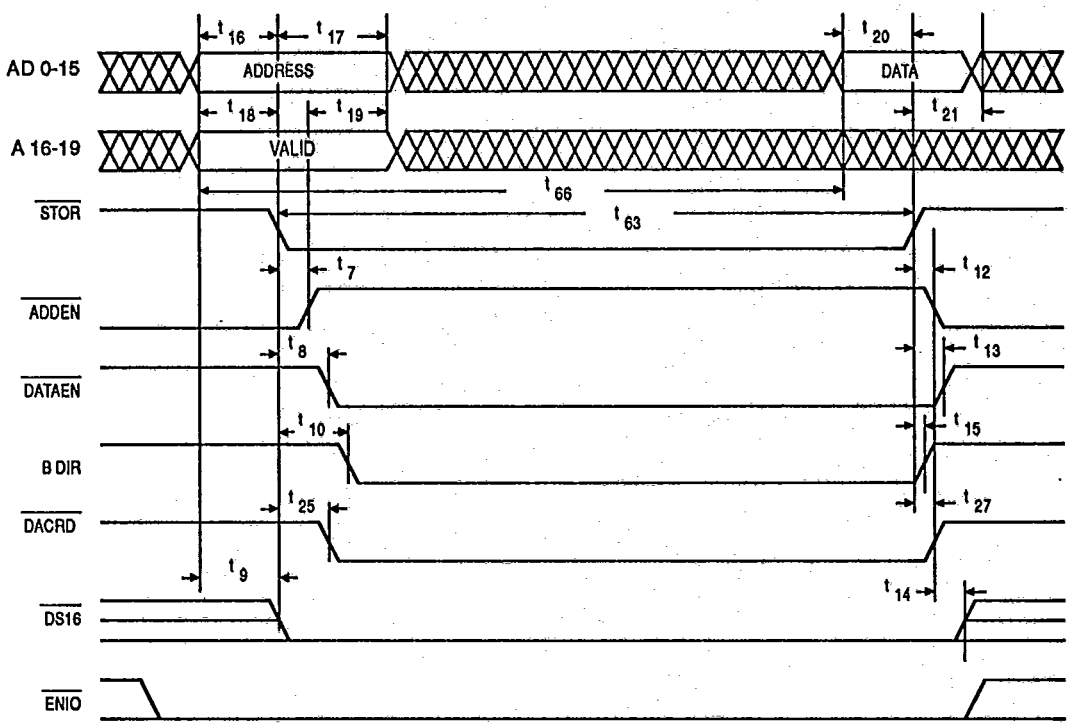

Figure 8. AT Mode I/O Read Timing

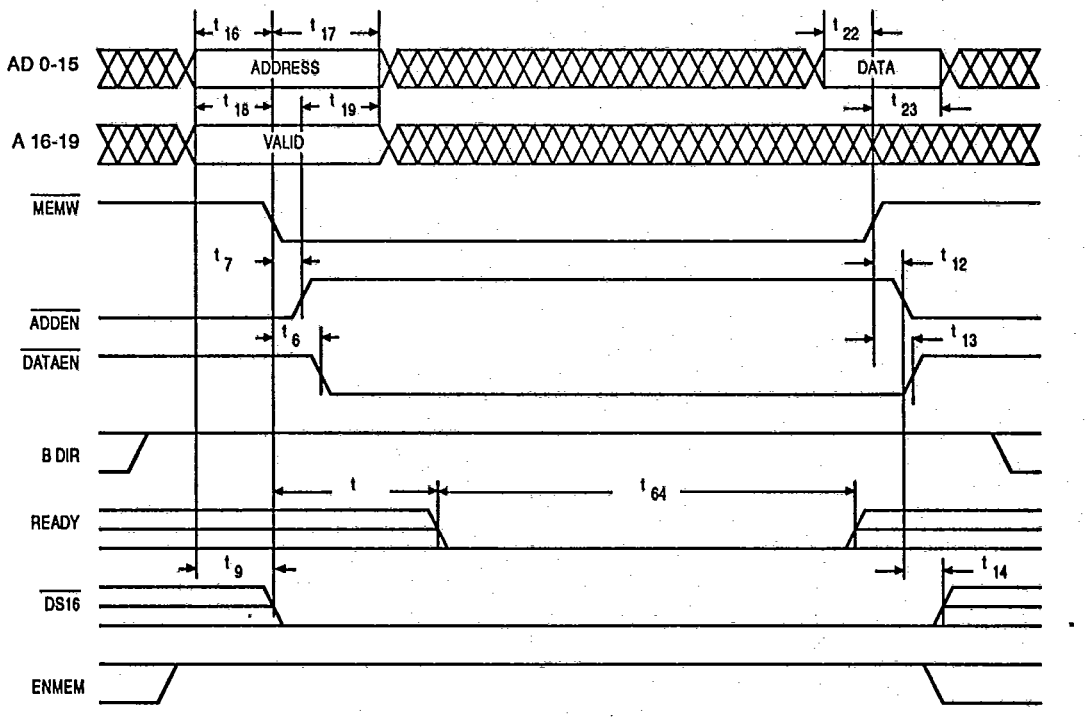

Figure 9. AT Mode Memory Write Timing

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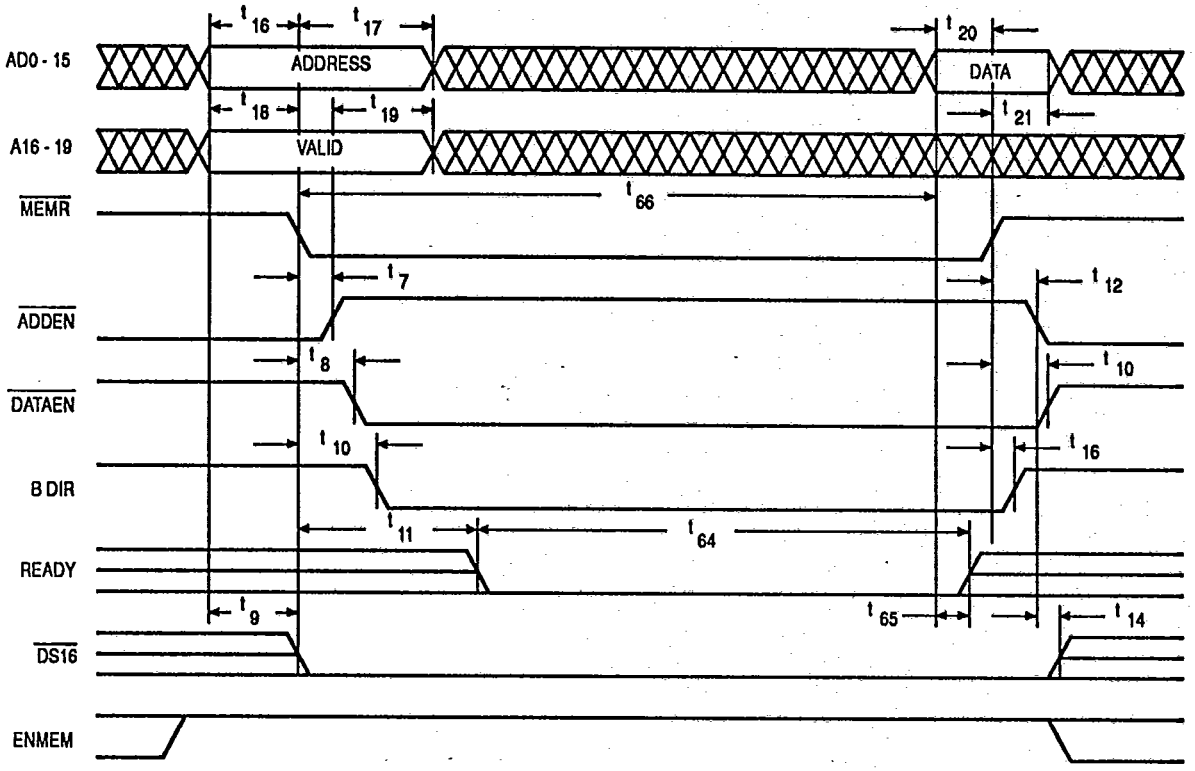

Figure 10. AT Mode Memory Read Timing

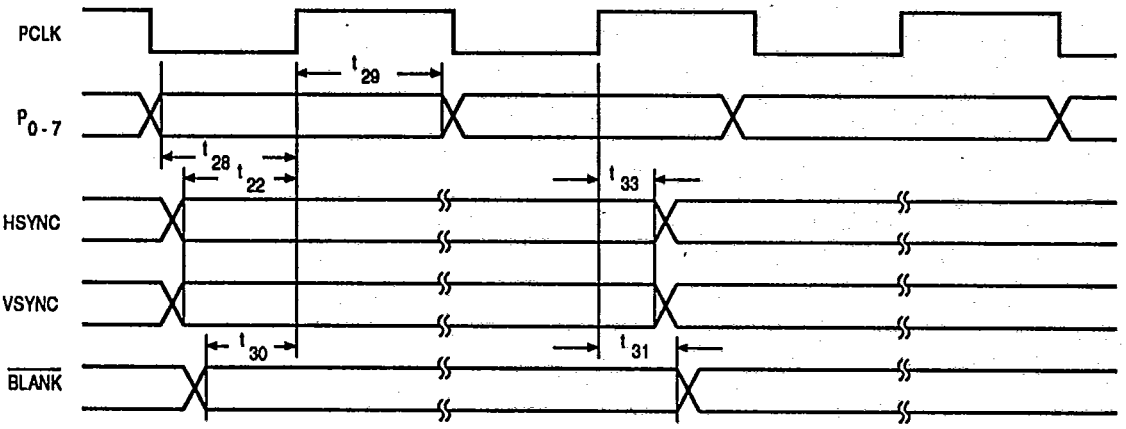

Figure 11. DAC Interface Timings

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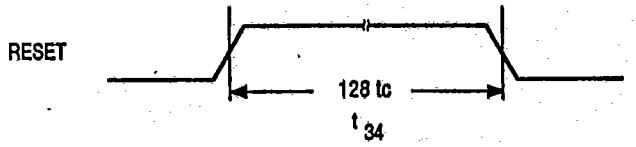

Figure 12. Reset Timing

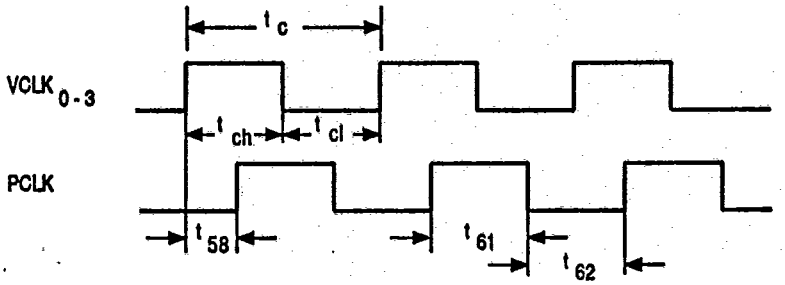

Figure 13. Clock/PCLK Timing

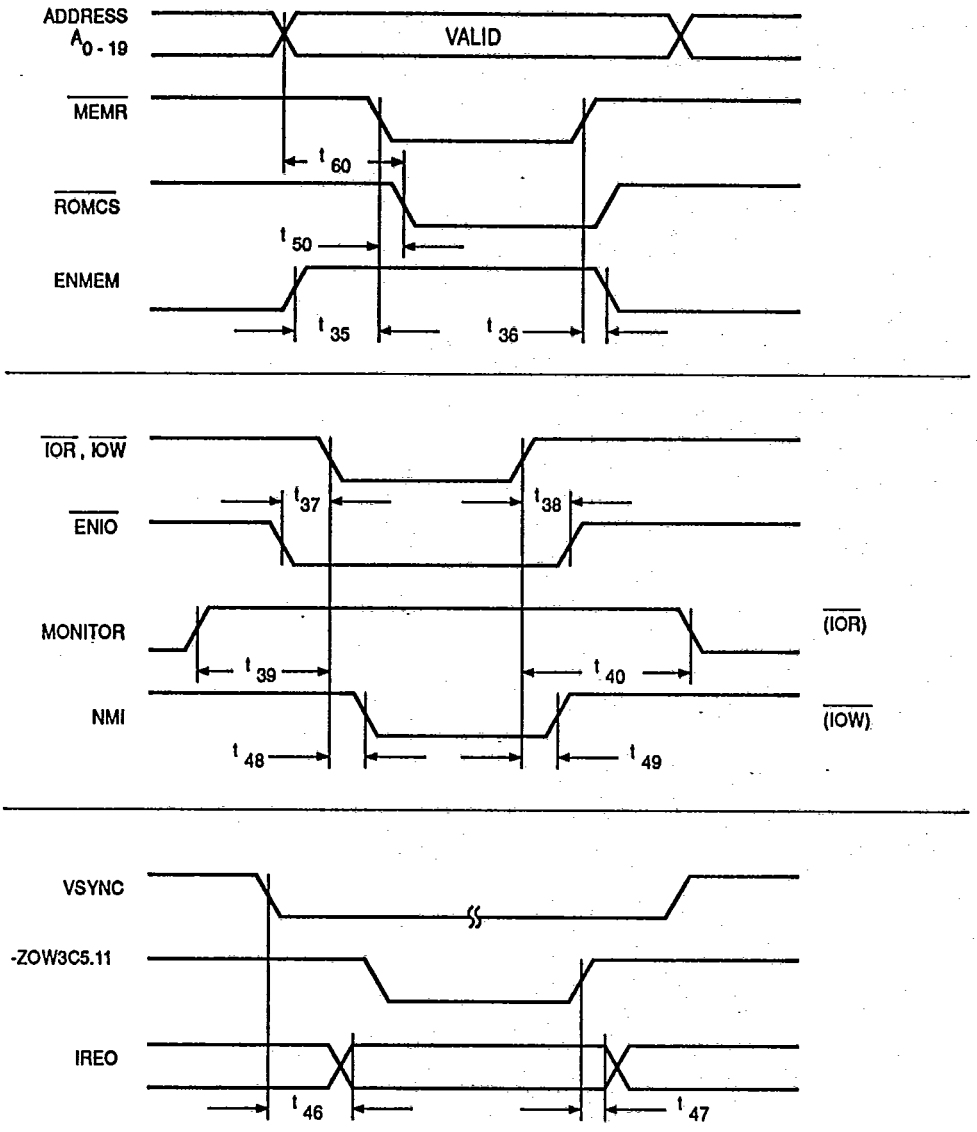

Figure 14. Miscellaneous Interface Timings

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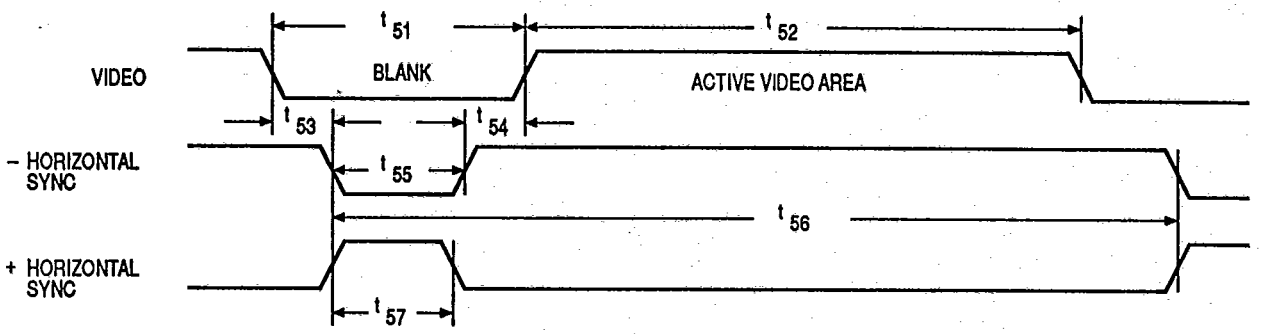
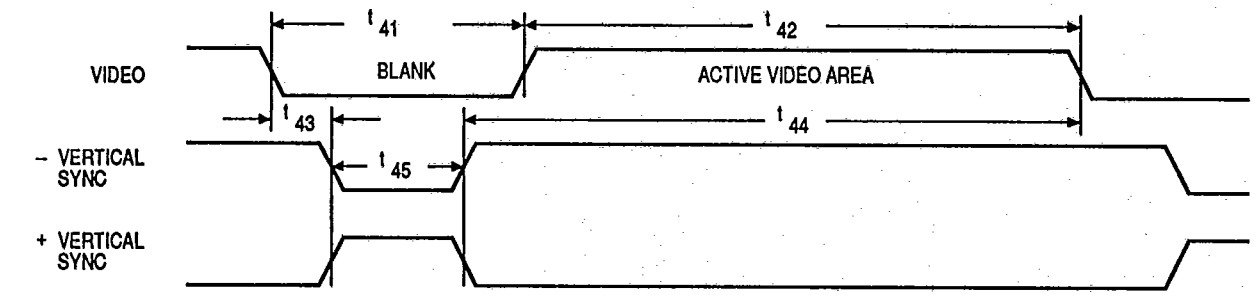


Horizontal Timing



Vertical Timing

Figure 15. Horizontal and Vertical Timing

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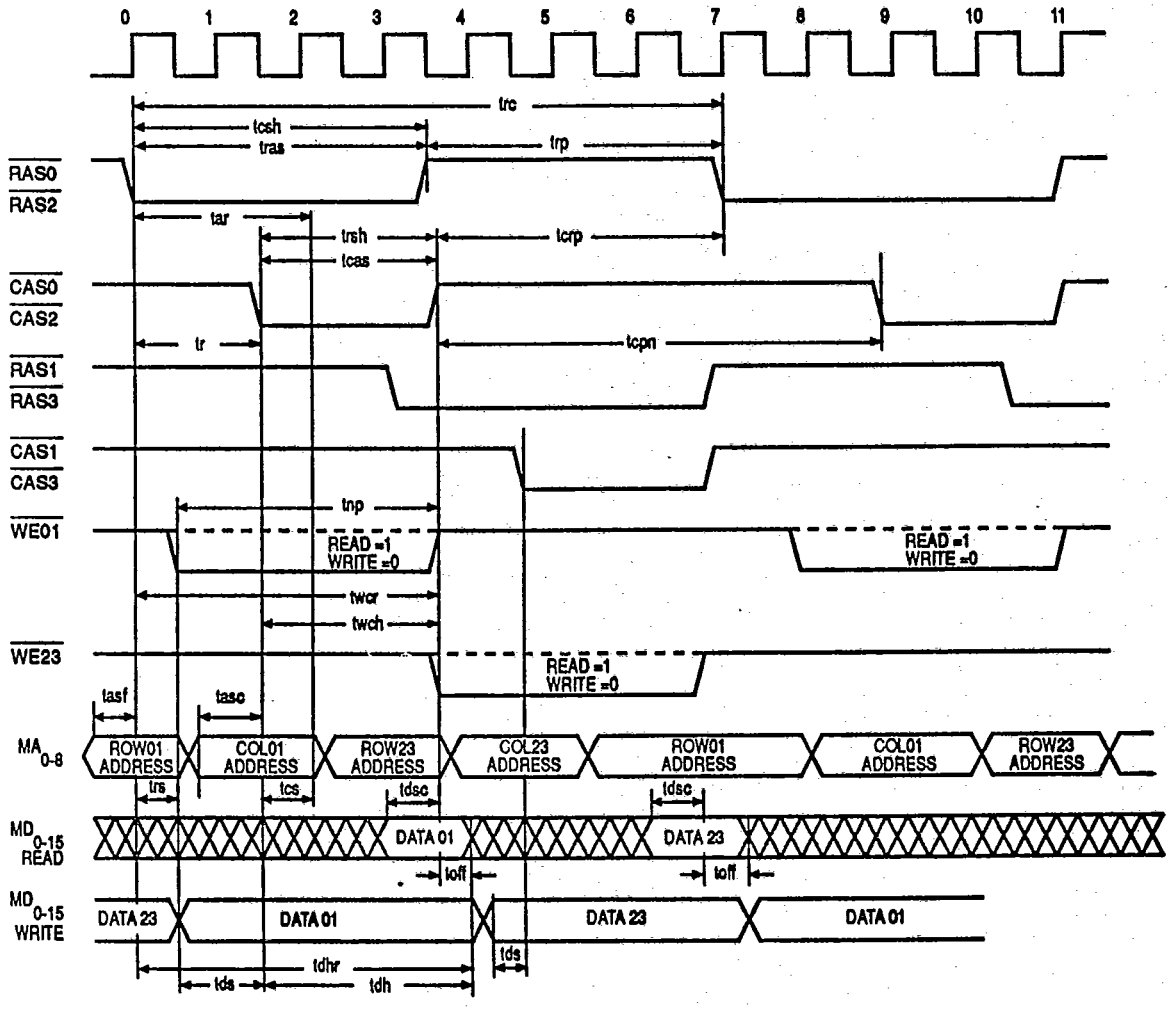

Figure 16. IGA Dram Timing Waveforms

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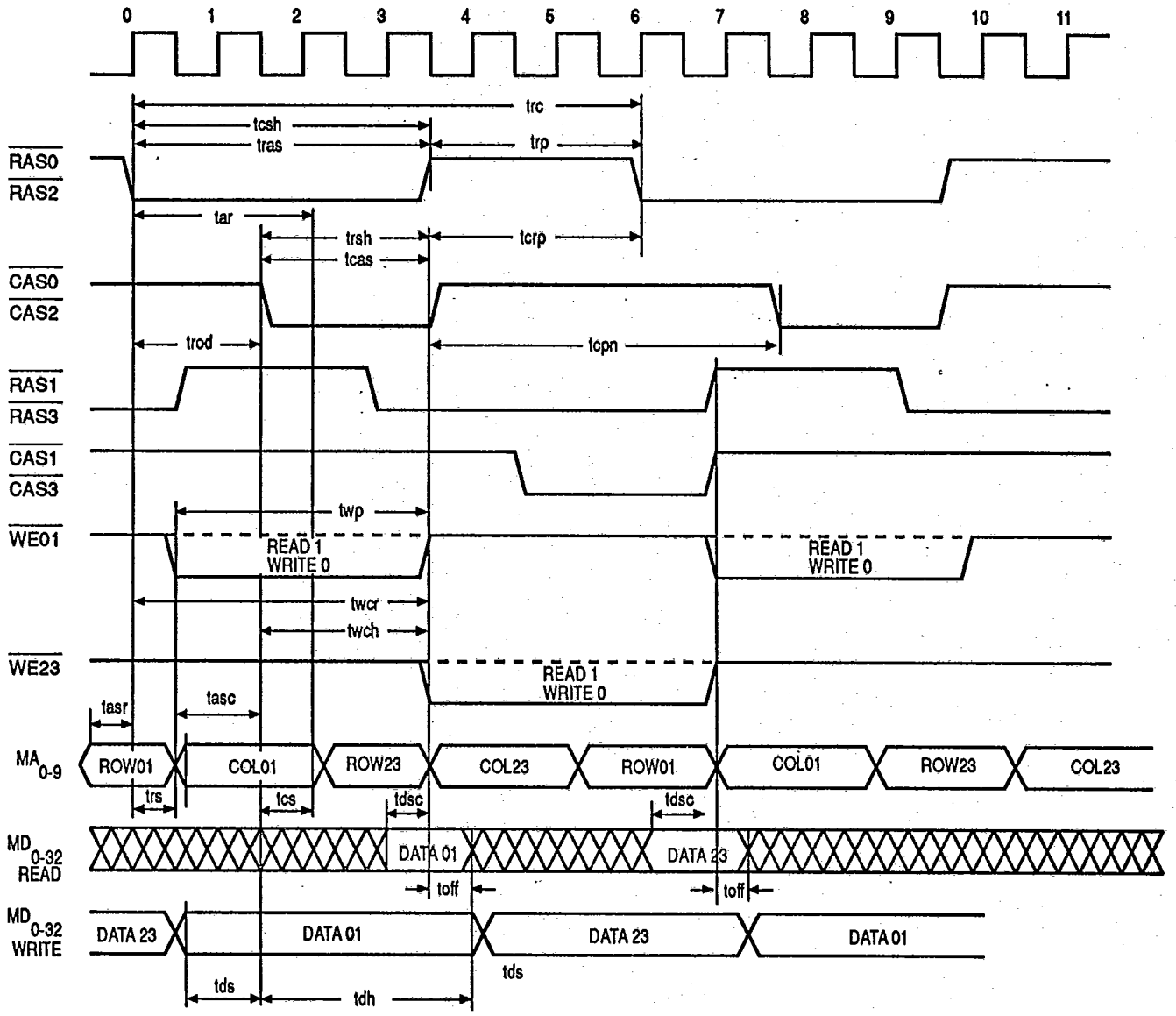

Figure 17. Eight-Dot DRAM Cycle Timing

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IGA DRAM TIMING WAVEFORMS (HIGH BANDWIDTH MODE AND RAS-ONLY REFRESH)

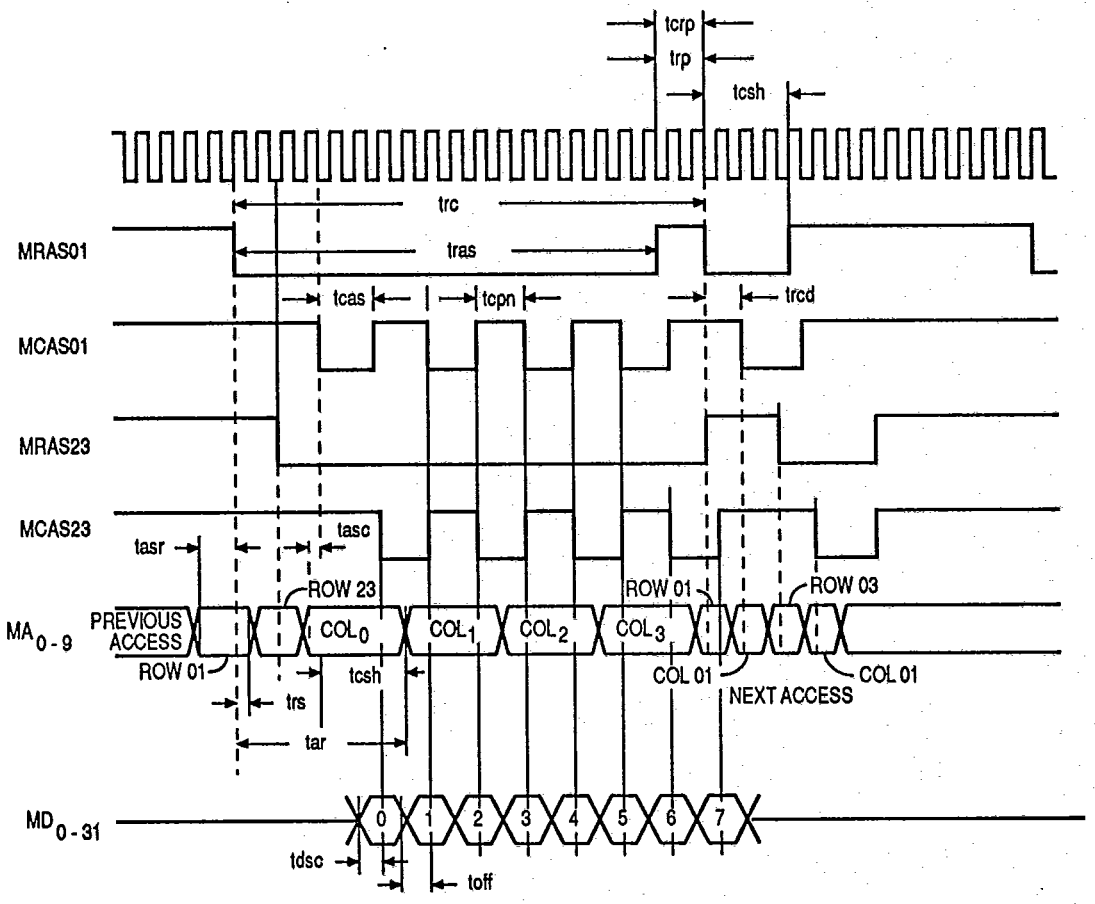

Figure 18. Page Mode Timing

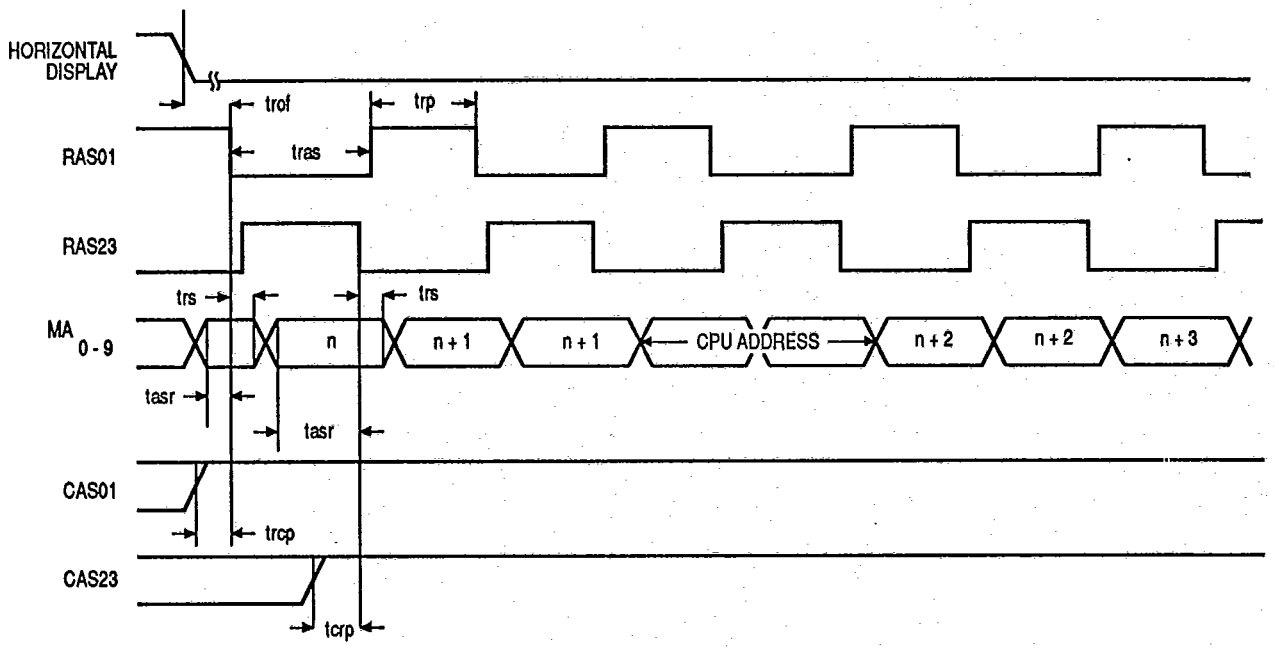

Figure 19. RAS-Only Refresh Timing

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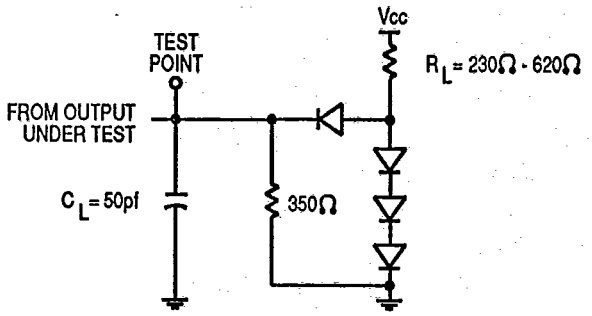
TEST LOAD NETWORK

Standard Outputs



Open Collector Outputs

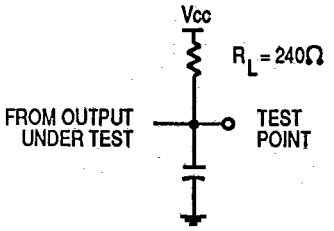


Figure 20. Standard and Open Collector Outputs

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IGA REGISTERS

Register Name	Page	Size	Address	Function
DAC Interface Registers				
DAC Mask	43	8 bit	02EA	Read/Write
DAC Read Index	43	8 bit	02EB	Read/Write
DAC Write Index	44	8 bit	02EC	Read/Write
DAC Data	44	8 bit	02ED	Read/Write
Advanced Function Control	45	16 bit	4AE8	Write Only
Interrupt Control Register				
Subsystem Control	46	16 bit	42E8	Write Only
Drawing Control Registers				
Current Y Position	48	16 bit	82E8	Read/Write
Current X Position	48	16 bit	86E8	Read/Write
Destination Y Position/Axial Step Constant	49	16 bit	8AE8	Write Only
Destination X Position/Diagonal Step Constant	49	16 bit	8EE8	Write Only
Error Term	50	16 bit	92E8	Read/Write
Major Axis Pixel Count	50	16 bit	96E8	Write Only
Command	51	16 bit	9AE8	Write Only
Short Stroke Vector	53	16 bit	9EE8	Write Only
Background Color	55	16 bit	A2E8	Write Only
Foreground Color	55	16 bit	A6E8	Write Only
Write Mask	55	8 bit	AAE8	Write Only
Read Mask	56	16 bit	AEE8	Write Only
Color Compare	57	16 bit	B2E8	Write Only
Background Mix	57	16 bit	BAE8	Write Only
Foreground Mix	58	16 bit	B6E8	Write Only
Multifunction Control	59	16 bit	BEE8 I	Write Only
Fixed Pattern Low	61	16 bit	BEE8-8	Write Only
Fixed Pattern High	62	16 bit	BEE8-9	Write Only
Pixel Control	63	16 bit	8BEE8-A	Write Only
Pixel Data Transfer	64	16 bit	E2E8	Read/Write
Status Registers				
Subsystem Status	65	16 bit	42E8	Read Only
Graphics Processor Status	66	16 bit	9AE8	Read Only

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IBM 8514/A-COMPATIBLE REGISTERS

With the exception of DAC interface registers, all IGA registers are 16 bits in length. All unused bits are reserved.

DAC INTERFACE REGISTERS

The four 8-bit DAC Interface Registers are used to program the external video DAC. All four registers are read/write registers. After the index for read/write is written, multiple read/write operations can be performed without the need of setting a new index for each entry.

To write to the DAC:

1. Set Start DAC Write Index at 02EC.
2. Write three bytes (R, G, B values) at 02ED. The index will automatically increment to the next write entry.
3. Repeat the previous step for the desired number of entries.

To read from the DAC:

1. Set Start DAC Read Index at 02EB.
2. Read three bytes (R, G, B values) at 02ED. The index will automatically increment to the next read entry.
3. Repeat the previous step for the desired number of entries.

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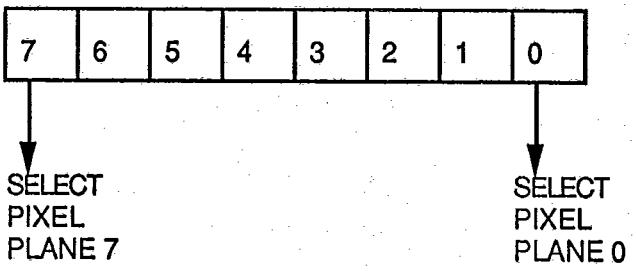
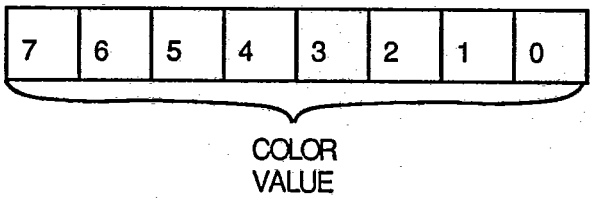
DAC Mask Register	Read/Write
8-bit	Address 02EA

The DAC Mask Register selects the pixel planes to be displayed. Each bit in the register will select the corresponding pixel plane; thus bit 0 selects pixel plane 0 and bit 7 selects pixel plane 7.



DAC Read Index Register	Read/Write
8-bit	Address 02EB

The DAC Read Index Register selects one of the 256 Color Lookup registers to be read through the DAC Data Register at address 02ED.



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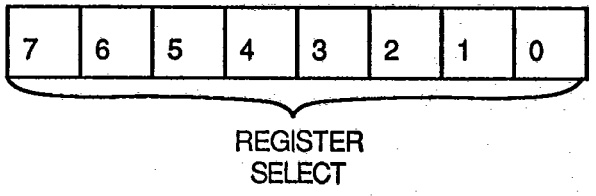
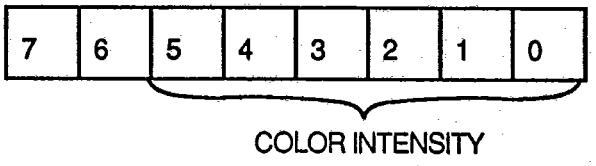
DAC Write Index Register	Read/Write
8-bit	Address 02EC

The DAC Write Index Register selects one of 256 Color Lookup registers to be written through the DAC Data Register at address 02ED.



DAC Data Register	Read/Write
8-bit	Address 02ED

The DAC Data Register (bits 5 to 0) specifies one of the three R, G, or B color intensities. Three consecutive accesses are needed to load every Color Lookup Register.



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Advanced Function Control Register	Write Only
16-bit	Address 4AE8

The Advanced Function Control Register is employed by all functions of the IGA to select the graphics mode. Bits 0 and 2 are used to select mode and resolution.

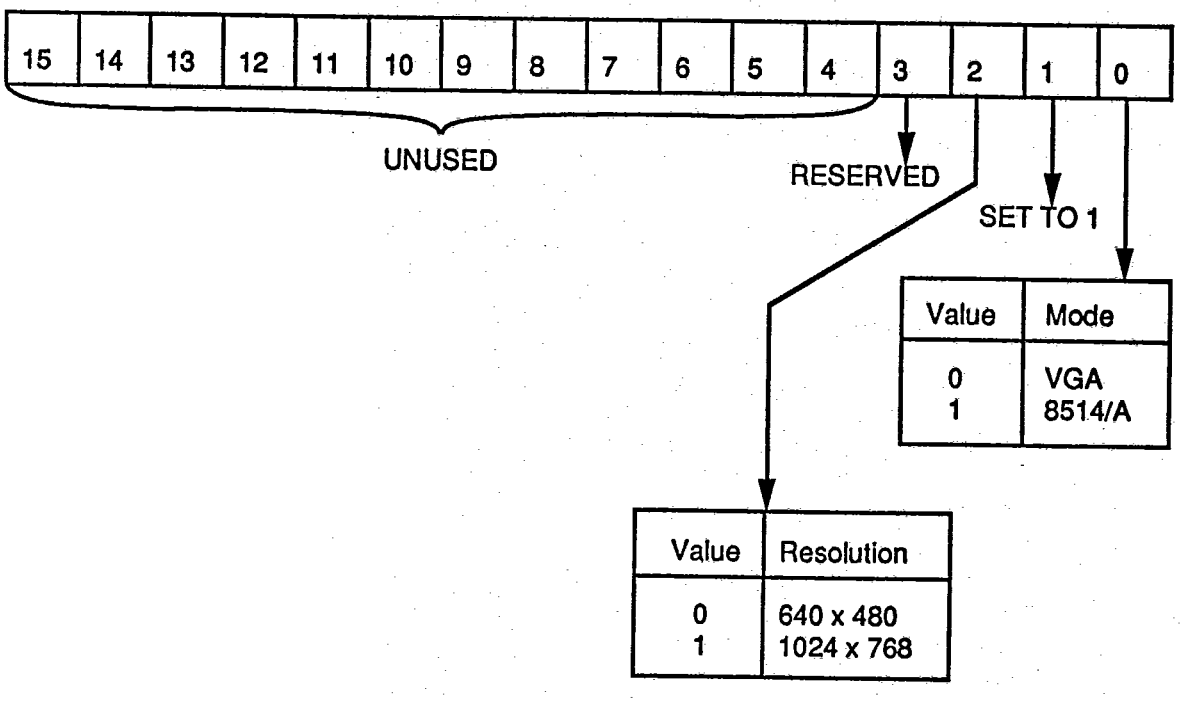
Bit 0, Mode, is used to select 8514/A graphics mode or VGA mode.

Bit 1 is set to 1.

Bit 2, Resolution, is used to select the screen resolution.

Bit 3 is reserved.

Bits 15 to 4 are unused.



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INTERRUPT CONTROL REGISTER

Subsystem Control Register	Write Only
16-bit	Address 42E8

The Subsystem Control Register controls interrupts, CPU resets, and CPU interface functions. The register effects bits 0 to 3 of the Subsystem Status Register.

Bit 0, VSYNC, puts a zero in the vertical sync status bit of the Subsystem Status Register that can be read at address 42E8.

Bit 1, Graphic Engine Busy, puts a zero in the data transfer ready flag bit of the Subsystem Status Register that can be read at address 42E8.

Bit 2, FIFO Overflow, puts a zero in the queue full bit of the Subsystem Status Register that can be read. This bit is cleared at the end of every line during a read across the plane.

Bit 3, FIFO Empty, puts a zero in the graphic processor empty bit of the Subsystem Status Register that can be read.

Bits 7 to 4 are zero.

Bit 8, Interrupt on Vertical Field, enables/disables the vertical field interrupt.

Bit 9, Interrupt on Data Transfer Ready, enables/disables the data transfer ready interrupt.

Bit 10, Interrupt on Queue Full Flag, enables/disables the queue full interrupt.

Bit 11, Interrupt on Graphics Processor Idle, enables/disables the graphics processor idle interrupt.

Bits 13 to 12 are a code for Enable/Disable Pixel Synchronizer.

Bits 15 to 14 are a code for Enable/Disable Graphics Sequencer.

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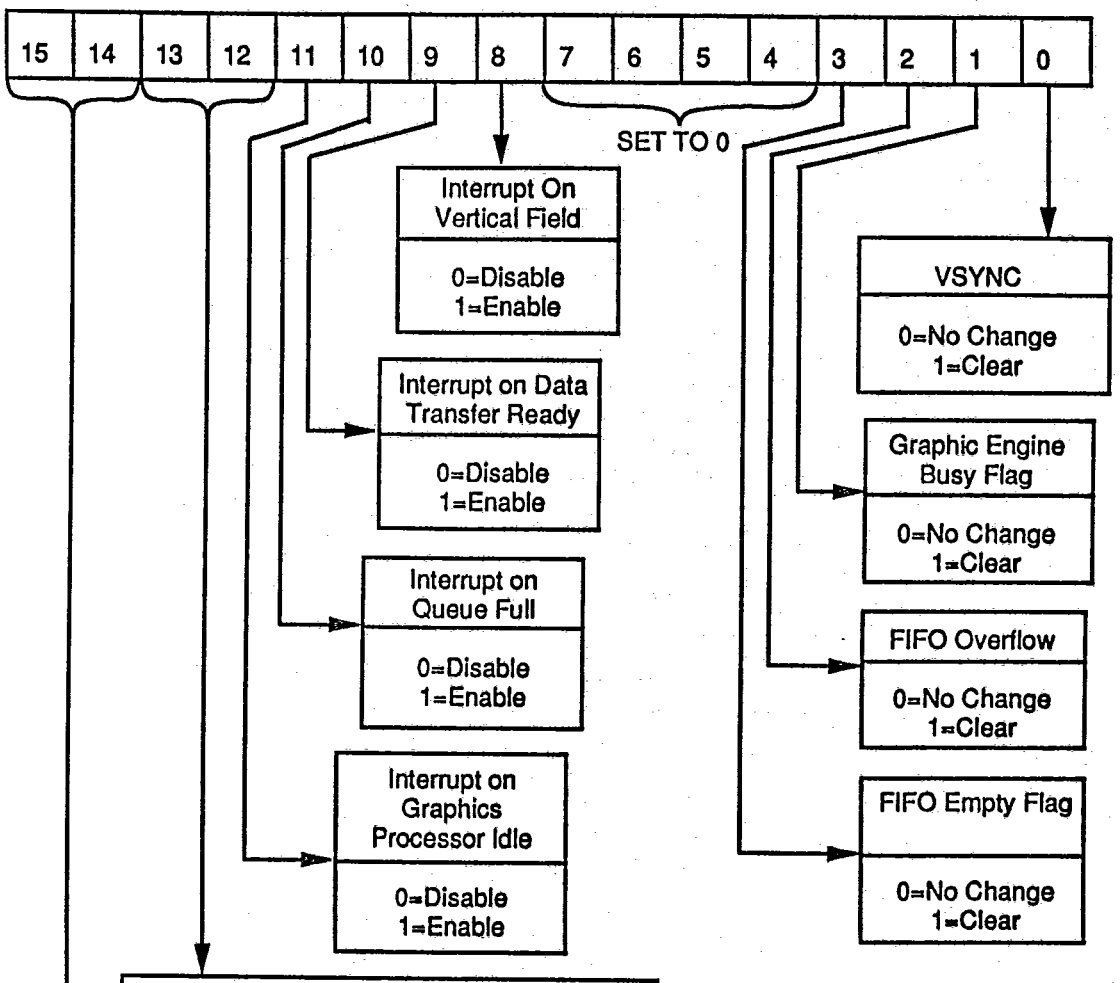
SUBSYSTEM CONTROL REGISTER



Enable/Disable Pixel Syncronizer	
Value	Description
00	No Change from Previous Setting
01	Enable Pixel Syncronizer
10	Disable Pixel Syncronizer
11	Disable Pixel Syncronizer

Enable/Disable Graphics Sequencer	
Value	Description
00	No Change from Previous Setting
01	Enable Graphics Sequencer
10	Disable Graphics Sequencer
11	Disable Graphics Sequencer

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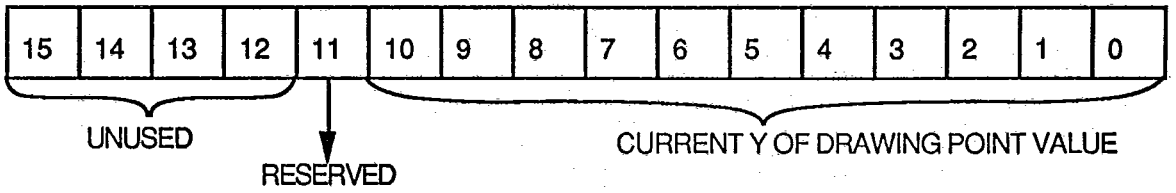
DRAWING CONTROL REGISTERS

There are sixteen registers associated with drawing control.

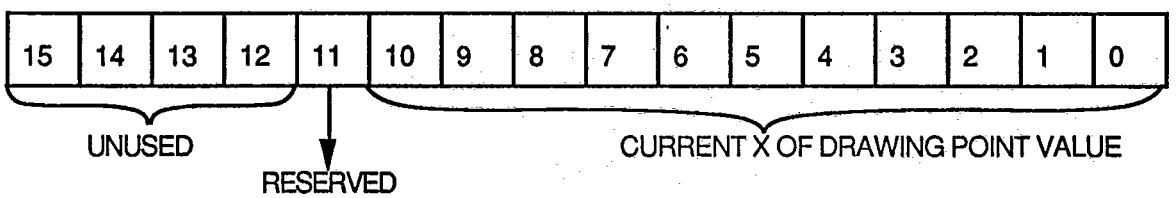
Current Y Position Register	Read/Write
16-bit	Address 82E8

The Current Y Position Register (bits 10 to 0) defines the Y position of the pixel currently being drawn. The status of this register can be read. The value is 11 unsigned bits. Bit 11 is reserved for higher resolution. Bits 15 to 12 are unused.



Current X Position Register	Read/Write
16-bit	Address 86E8

The Current X Position Register (bits 10 to 0) defines the X position of the pixel currently being drawn. The status of this register may be read. The value is 11 unsigned bits. Bit 11 is reserved for higher resolution. Bits 15 to12 are unused.



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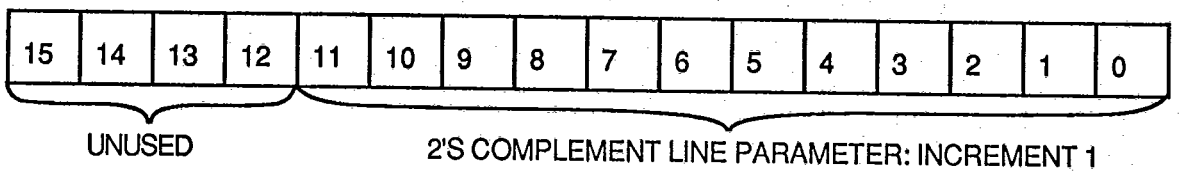
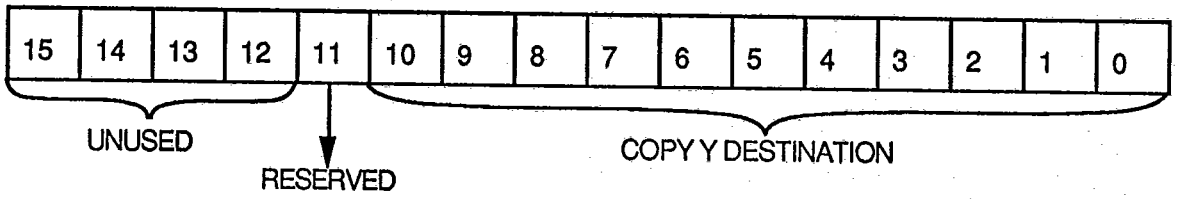
Destination Y Position/Axial Step Constant Register	Write Only
16-bit	Address 8AE8

The Destination Y Position/Axial Step Constant Register defines the Y destination in two ways as specified by the Command register. During bit block (BITBLT) copying, bits 10 to 0 are used to define the Y destination. During line drawing, bits 11 to 0 define the increment value. The command to be performed is specified by the Command Register. Bits 15 to 12 are unused. The minterm for line drawing is:

Increment 1 = 2 * (min (|dx|, |dy|))





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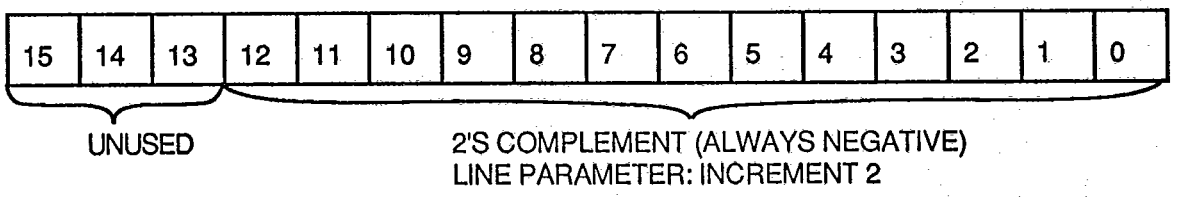
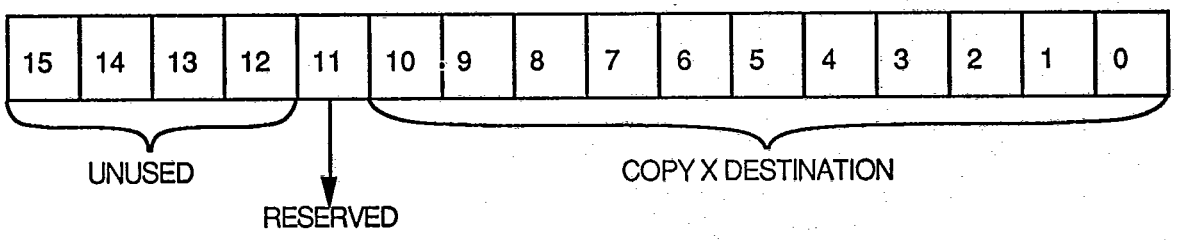
Destination X Position/Diagonal Step Constant Register	Write Only
16-bit	Address 8EE8

The Destination X Position/ Axial Step Constant Register defines the X destination in two ways as specified by the Command register. During bit block (BITBLT) copying, bits 10 to 0 are used to define the Y destination. The value is 13 signed bits during line drawing. Bits 15 to 12 are unused. The minterm for line drawing is:

Increment 2 = 2*(min|dx|, |dy|) - max (|dx|, |dy|)





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Error Term Register	Read/Write
16-bit	Address 92E8

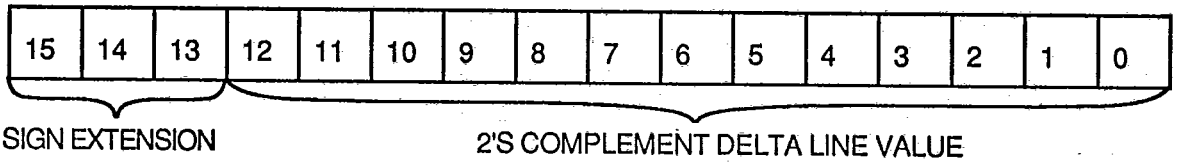
The Error Term Register defines the delta for the current line drawing (bits 12 to 0) as 2's complement with the sign bit extended (bits 15 to 13). The value is signed, 2's complement, 13 bits. The minterm for line drawing is:

if starting x < ending x,

2* [min (|dx|, |dy|)] - max (|dx|, |dy|) - 1)

and if starting x ≥ ending x, then

2* [min (|dx|, |dy|)] - max (|dx|, |dy|)



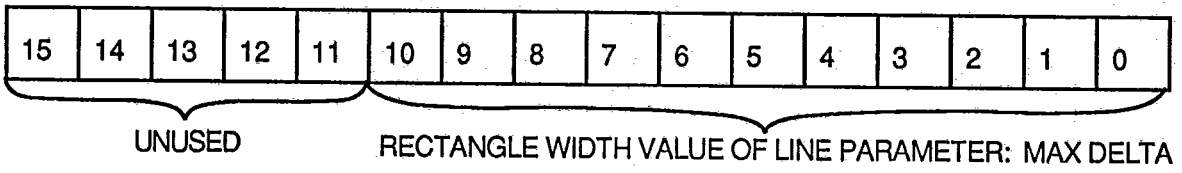
Major Axis Pixel Count Register	Write Only
16-bit	Address 96E8

The Major Axis Pixel Count Register (bits 10 to 0) defines the width the rectangle in bit block (BITBLT) or rectangle mode, or line length in line drawing mode.

The drawing mode is determined by the Command Register. The value is 11 unsigned bits. Bits 15 to 11 are unused. In line drawing mode, the minterm is:

Line Parameter = max(|dx|, |dy|)

Rectangle Width Value = Rectangle Width -1



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Command Register	Write Only
16-bit	Address 9AE8

The Command Register selects drawing commands as shown below in the register diagram. All parameters must be set before the command is sent to activate drawing.

Bit 0, Read/Write, specifies read (0) or write (1).

Bit 1, Pixel Mode Flag, specifies single pixel mode (0) or multi-pixel mode (1).

Bit 2, Last Pixel Off Flag, specifies the last pixel drawn (0) or pixel turned off (1).

Bit 3, Drawing Type Flag, specifies drawing direction as coordinate-based (0) or radial (1). The direction is specified by bits 5 to 7 as shown in the table below.

Bit 4, Draw/Move Flag, specifies move (0) or draw (1).

Bits 7 to 5 specify the drawing direction as shown in the drawing direction table on the next page.

Bit 8, Wait State, is set to 1 to allow waiting for CPU data for functions such as image transfer or texture line drawing.

Bit 9, Bus select, specifies 8-bit bus (0) or 16-bit bus (1).

Bit 10 is reserved for a future feature.

Bit 11 is unused.

Bit 12, Swap Data Bytes Flag, specifies that either the most significant byte is drawn first (0), or the least significant byte is drawn first (1) when the 16-bit data bus is selected.

Bits 15 to 13 specify the drawing function as shown in the table below.

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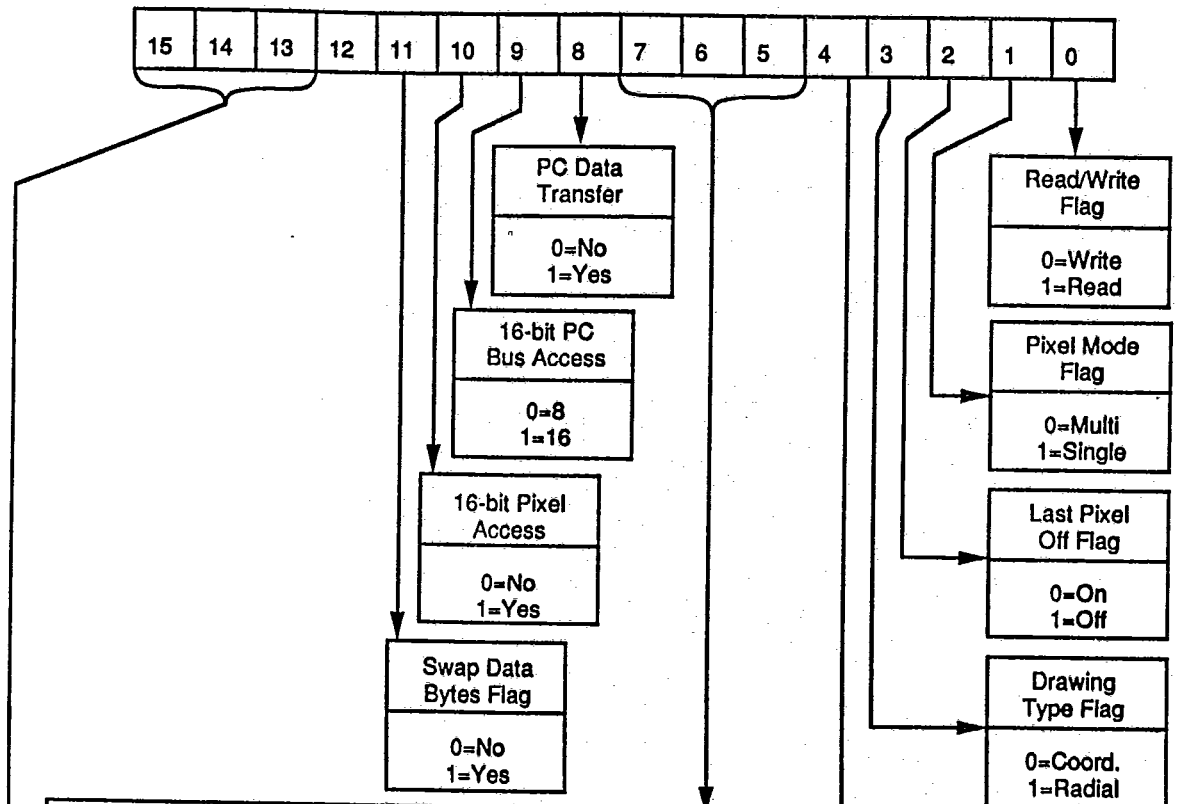
COMMAND REGISTER



Drawing Direction		
Value	Line Algorithm Flag bit-3 Command Reg.=0	Line Algorithm Flag bit 3 Command Reg.=1
000	0 degrees	y neg, x major, x neg
001	45 degrees	y neg, x major, x pos
010	90 degrees	y neg, y major, x neg
011	135 degrees	y neg, y major, x pos
100	180 degrees	y pos, x major, x neg
101	225 degrees	y pos, x major, x pos
110	270 degrees	y pos, y major, x neg
111	315 degrees	y pos, y major, x pos

Value	Drawing Function
000	No Operation
001	Line Drawing
010	Rectangle Fill (Horizontal first) polygon fill
011	Rectangle Fill (Vertical 1st by 2 Vert. pixel)
100	Rectangle Fill (Vertical 1st by 4 Hor. pixel)
101	Polygon Boundry Line Draw
110	BITBLT
111	Not defined

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Short Stroke Vector Register	Write Only
16-bit	Address 9EE8

The Short Stroke Vector Register holds two data bytes. Each byte specifies pixel length, drawing direction, and move/draw control for a short stroke vector.

Bits 3 to 0 define the pixel line length.

Bit 4, Move/Draw, selects a move function (0) or draw function (1).

Bits 7 to 5 define the direction of the line to be drawn. Whether the line is coordinate- or radial-based is determined by bit 3 of the Command Register.

Bits 11 to 8 define the pixel line length.

Bit 12, Move/Draw, selects a move function (0) or draw function (1).

Bits 15 to 13, define the direction of the line to be drawn. Whether the line is coordinate- or radial-based is determined by bit 3 of the Command Register.

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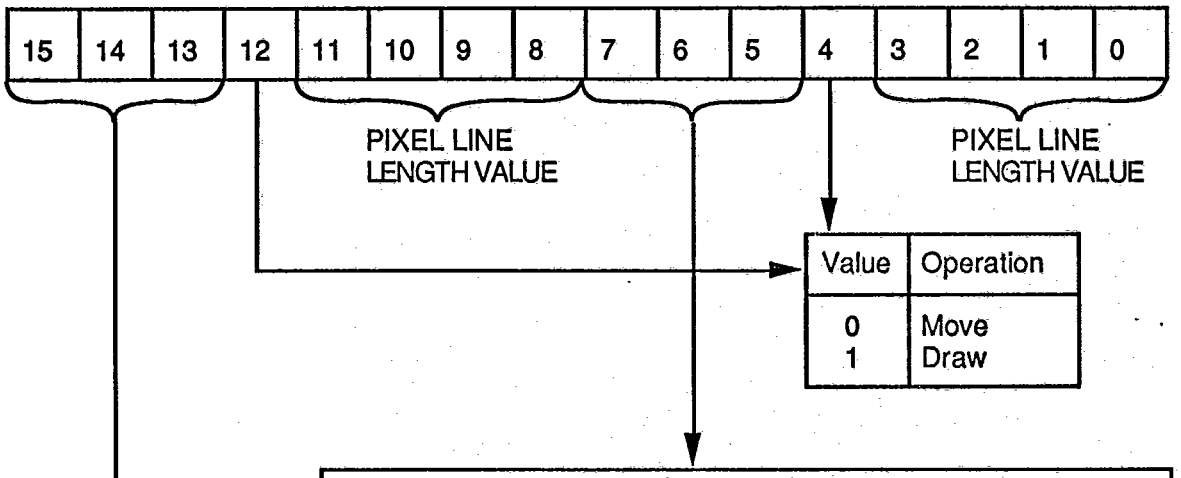
SHORT STROKE VECTOR REGISTER



Value	Operation
0	Move
1	Draw

Drawing Direction		
Value	Line Algorithm Flag bit-3 Command Reg.=0	Line Algorithm Flag bit 3 Command Reg.=1
000	0 degrees	x major, x neg. (left)
001	45 degrees	x major, x pos. (right)
010	90 degrees	y major, y neg. (up)
011	135 degrees	y major, y neg (up)
100	180 degrees	x major, x neg. (left)
101	225 degrees	x major, x pos. (right)
110	270 degrees	y major, y pos. (down)
111	315 degrees	y major, y pos. (down)

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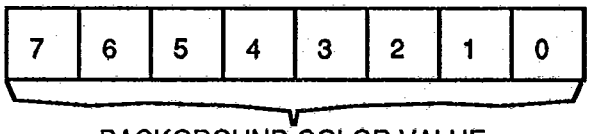
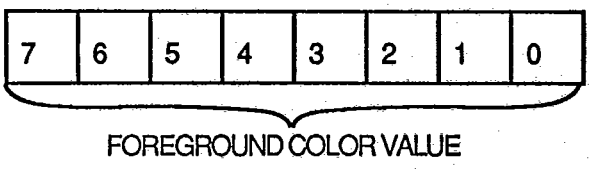
Background Color Register	Write Only
8-bit	Address A2E8

The Background Color Register (bits 7 to 0) specifies the background color selected by the Source Data Field of the Foreground/Background Mix registers.



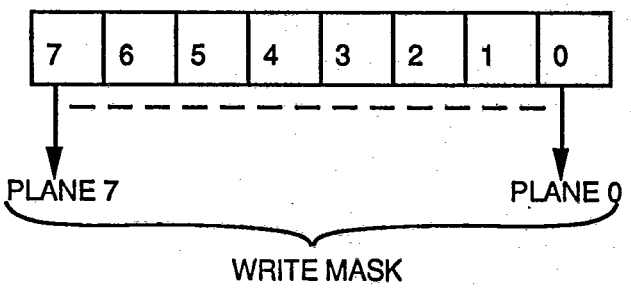
Foreground Color Register	Write Only
8-bit	Address A6E8

The Foreground Color Register (bits 7 to 0) contains the value of the foreground color.



Write Mask Register	Write Only
8-bit	Address AAE8

The Write Mask Register selects the bit-planes for graphics and text update. Each bit selects the associated plane.



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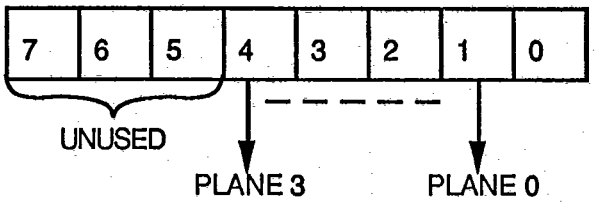
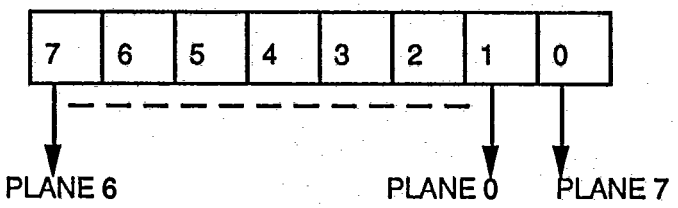
Read Mask Register	Write Only
16-bit	Address AEE8

The Read Mask register selects the read source for graphics or text updates. The mask bits are rotated to the left by one bit, except for polygon fills as shown in the diagrams below. The value is the true mask rotated one bit to the left for 4-bit plane and 8-bit plane operations as shown below. However, for polygon fill the relationship of bit position to plane is in direct correspondence as shown below.

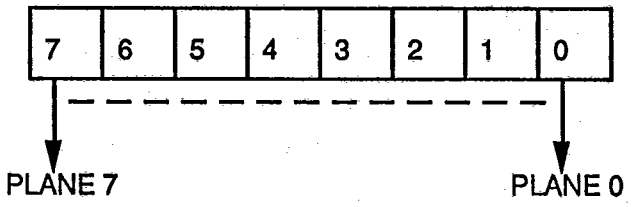
4-bit Bit-plane



8-bit Bit-plane

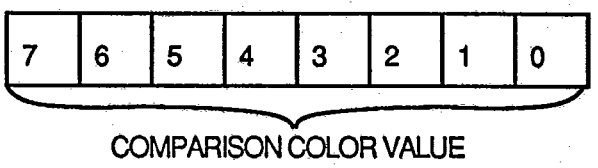


Polygon Fill



Color Compare Register	Write Only
16-bit	Address B2E8

The Color Compare Register (bits 7 to 0) defines the color compare value that is used in conjunction with the Pixel Control Register to determine which pixel positions require updating.



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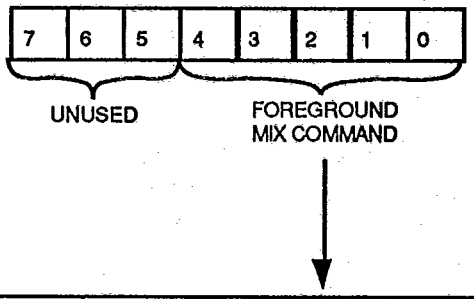
Background Mix Register	Write Only
8-bit	Address B6E8

The Background Mix Register selects background color source and mix modes as shown below.



Value (h)	Description
00	NOT Screen
01	Zero
02	One
03	Leave Alone
04	NOT New
05	XOR
06	NOT Screen XOR New
07	Overpaint
08	NOT Screen OR NOT New
09	Screen OR NOT New
0A	NOT Screen OR New
0B	Screen OR New
0C	Screen OR New]
0D	NOT Screen AND New
0E	Screen AND NOT New
0F	NOT Screen AND NOT New
10	Minimum
11	(Screen-New) without saturate
12	(New-Screen) without saturate
13	(New+Screen) without saturate
14	Maximum
15	(Screen-New)/2 without saturate
16	(New-Screen)/2 without saturate
17	Average = (New+Screen)/2 without saturate
18	(Screen-New) with saturate
19	(Screen-New) with saturate
1A	(New-Screen) with saturate
1B	(New+Screen) with saturate
1C	(Screen-New)/2 with saturate
1D	(Screen-New)/2 with saturate
1E	(New-Screen)/2 with saturate
1F	(New+Screen)/2 with saturate

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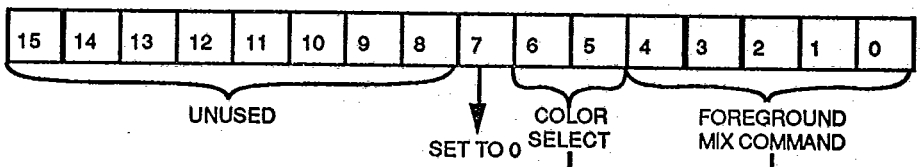
Foreground Mix Register	Write Only
16-bit	Address BAE8

The Foreground Mix Register selects foreground color source and mix commands as shown below.



Value	Description
00	Background Color Mode
01	Foreground Color Mode
10	CPU Data Transfer Mode
11	Frame Buffer Mode

Value (h)	Description
00	NOT Screen
01	Zero
02	One
03	Leave Alone
04	NOT New
05	XOR
06	NOT Screen XOR New
07	Overpaint
08	NOT Screen OR NOT New
09	Screen OR NOT New
0A	NOT Screen OR New
0B	Screen OR New
0C	Screen OR New]
0D	NOT Screen AND New
0E	Screen AND NOT New
0F	NOT Screen AND NOT New
10	Minimum
11	(Screen-New) without saturate
12	(New-Screen) without saturate
13	(New+Screen) without saturate
14	Maximum
15	(Screen-New)/2 without saturate
16	(New-Screen)/2 without saturate
17	Average = (New+Screen)/2 without saturate
18	(Screen-New) with saturate
19	(Screen-New) with saturate
1A	(New-Screen) with saturate
1B	(New+Screen) with saturate
1C	(Screen-New)/2 with saturate
1D	(Screen-New)/2 with saturate
1E	(New-Screen)/2 with saturate
1F	(New+Screen)/2 with saturate

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Multifunction Control Register	Write Only
16-bit	Address BEE8

The Multifunction Control Register selects drawing control parameters as shown below. As the drawing select bits of the register change, the function of the register changes as described below.

Bits 15 to 12 = 0, Minor Axis Pixel Count Register, bits 10 to 0 specify the height of the rectangle, where

Value = Rectangle Height - 1.

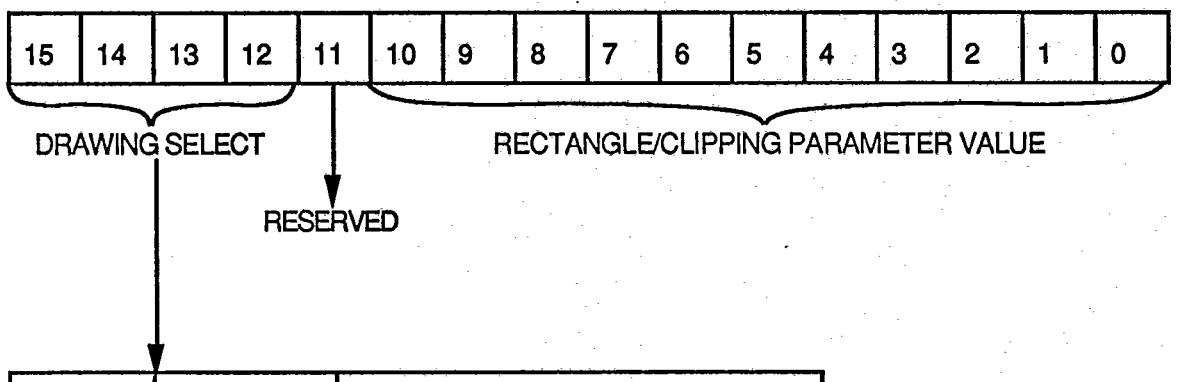
Bits 15 to 12 = 1, Top Scissors Register, bits 10 to 0 specify the top limit of the clipping window.

Bits 15 to 12 set to 2, Left Scissors Register, bits 10 to 0 specify the left limit of the clipping window.

Bits 15 to 12 set to 3, Bottom Scissors Register, bits 10 to 0 specify bottom limit of clipping window.

Bits 15 to 12 set to 4, Right Scissors Register, bits 10 to 0 specify the right limit of the clipping window.

Bit 11 is reserved.



Value	Address	Parameter
0000	BEE8-0	Rectangle Height-1
0001	BEE8-1	Clipping Window Top Limit
0010	BEE8-2	Clipping Window Left Limit
0011	BEE8-3	Clipping Window Bottom Limit
0100	BEE8-4	Clipping Window Right Limit

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Memory Control Register	Write Only
16-bit	Address BEE8-5

The Memory Control Register function is selected when the index (bits 12 to 15) is set to 5.

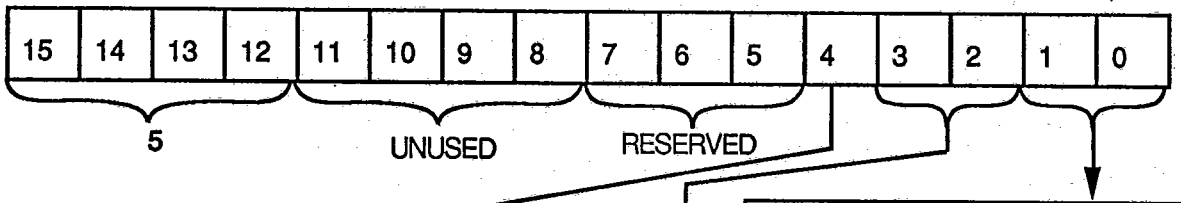
Bits 1 to 0, CAS Configuration, are as shown below.

Bits 3 to 2, Write Enable, are as shown below.

Bit 4, Planes for Drawing, selects lower 4 planes (0) or upper 4 planes (1).

Bits 7 to 5 are reserved.

Bits 11 to 8 are unused.



Planes for Drawing
0=Lower 4 Planes 1=Upper 4 Planes

Value	Description
00	2 CAS Configuration
01	4 CAS Configuration
10	6 CAS Configuration
11	8 CAS Configuration

Value	Description
00	4 Write Enable
01	5 Write Enable
10	8 Write Enable
11	10 Write Enable

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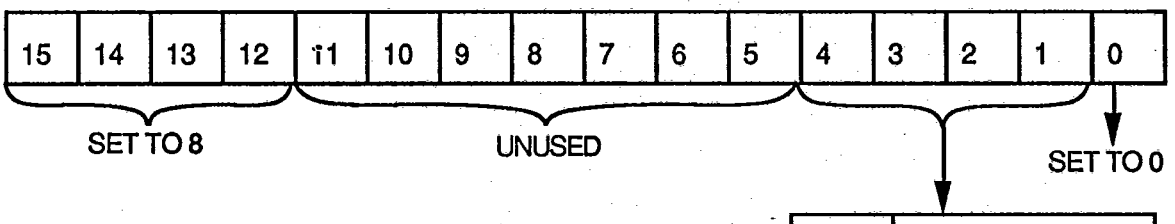
Fixed Pattern Low Register	Write Only
16-bit	Address BEE8-8

The Fixed Pattern Low Register function is selected when the index (bits 12 t0 15) is set to 8.

Bit 0 is set to 0.

Bits 4 to 1 select the pixel mix as shown in the table below.

Bits 11 to 5 are unused.



Bit	Description
0	Pixel 4 Mix Select
1	Pixel 3 Mix Select
2	Pixel 2 Mix Select
3	Pixel 1 Mix Select
4	Pixel 0 Mix Select

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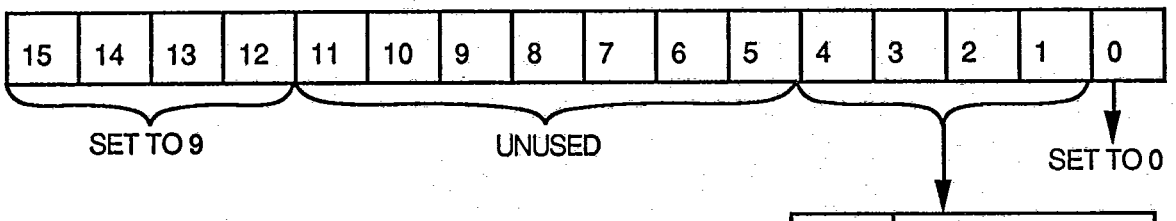
Fixed Pattern High Register	Write Only
16-bit	Address BEE8-9

The fixed Pattern High Register function is selected when the index (bits 12 to 15) is set to 9.

Bit 0 is set to 0.

Bits 4 to 1 select the pixel mix as shown in the table below.

Bits 11 to 5 are unused.



Bit	Description
0	Pixel 9 Mix Select
1	Pixel 8 Mix Select
2	Pixel 7 Mix Select
3	Pixel 6 Mix Select
4	Pixel 5 Mix Select

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Pixel Control Register	Write Only
16-bit	Address BEE8-A

The Pixel Control Register Function is selected when the index (bits 12 to 15) are set to A.

Bits 1 to 0 are set to 0.

Bit 2, Packed Enable:

For read operations, packed data is computed from the source. Packed data is screen data OR'ed with the complement of the bit plane read mask. If the result is all 1s, 1 is extracted. Otherwise,the result is 0.

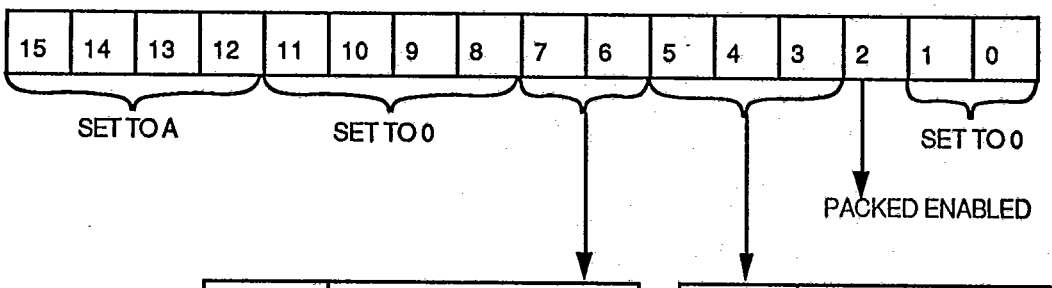
For write operations, IGA uses a special search and fill mode. Screen data is read. If extracted packed data is 0, the write operation is suspended. If a 1 is extracted, the write operation is enabled until the occurrence of the next 1.

The purpose of the mode is to detect polygon boundaries in fill operations.

Bits 5 to 3, Data Comparison, are as shown in the table below.

Bits 7 and 6, specify data extension, mix type, and extension sources as shown below.

Bits 11 to 8 are set to 0.



Value	Description
00	Forground Mix Active
01	Fixed Pattern Mode
10	Planar Write Mode
11	Single Plane Copy Mode

Value	Data Comparison
000	False
001	True
010	Plane Data ≥ Color Compare
011	Plane Data <Color Compare
100	Plane Data ≠ Color Compare
101	Plane Data = Color Compare
110	Plane Data ≤ Color Compare
111	Plane Data > Color Compare

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Pixel Data Transfer Register	Read/Write
16-bit	Address E2E8

The Pixel Data Transfer Register specifies the port for image transfer. For transfers across the plane image the data to be read or written is selected by the nibble boundary on the screen. The starting point falls on the first nibble group. In word mode, two data nibbles can be transfered for each read or write.

For Pixel Read operation across the plane:

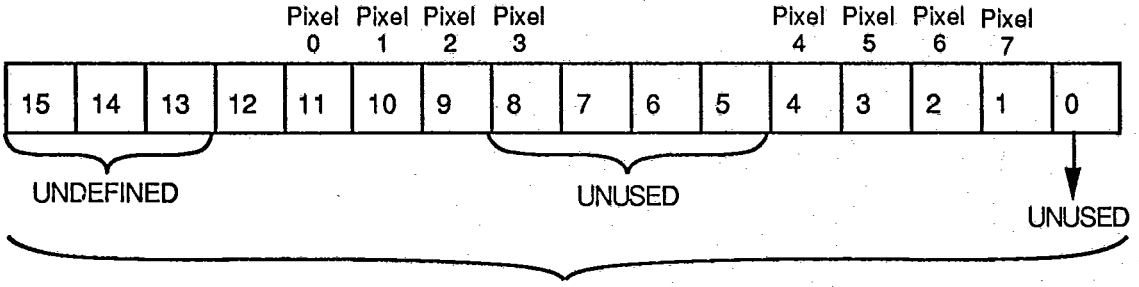
$$\text{Bit Value} = \prod_{i=1}^{n} (P_i + \overline{RM_i})$$

Where:

n = maximum bit-plane value
Pi = pixel value of the bit plane
RM_i = read mask for the i-th bit plane

For Pixel write operations across plane:

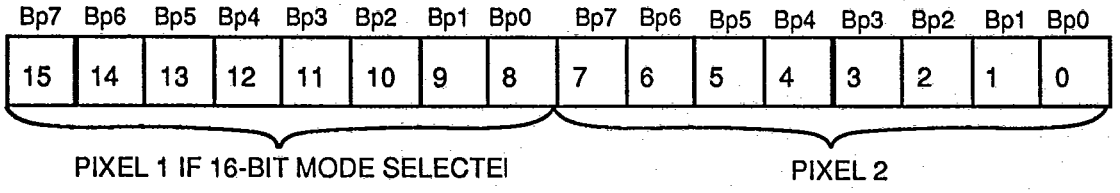
Bit =0, write background color
Bit=1, write foreground color



Value	Operation
0	Write Background Color
1	Write Foreground Color

FOR ALL PIXELS

For transfers through the plane image, two pixels can be transfered for each read or write.



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STATUS REGISTERS

There are two status registers: the Subsystem and Graphics Processor Status Registers.

Subsystem Status Register	Read Only
16-bit	Address 42E8

The Subsystem Status Register indicates interrupt status, monitor ID, and plane size.

Bit 0, VSYNC Interrupt Detection, is not detected (0) or detected (1).

Bit 1, Data Transfer Busy, is not busy (0) or busy (1).

Bit 2, FIFO Overflow, is no overflow (0) or overflow (1).

Bit 3, FIFO Empty, is not empty (0) or empty(1)

Bits 6 to 4, are the monitor ID.

Bit 7, Plane Size, is 4-bit (0) or 8-bit (1).

Bits 15 to 8, are reserved for hardware tests.

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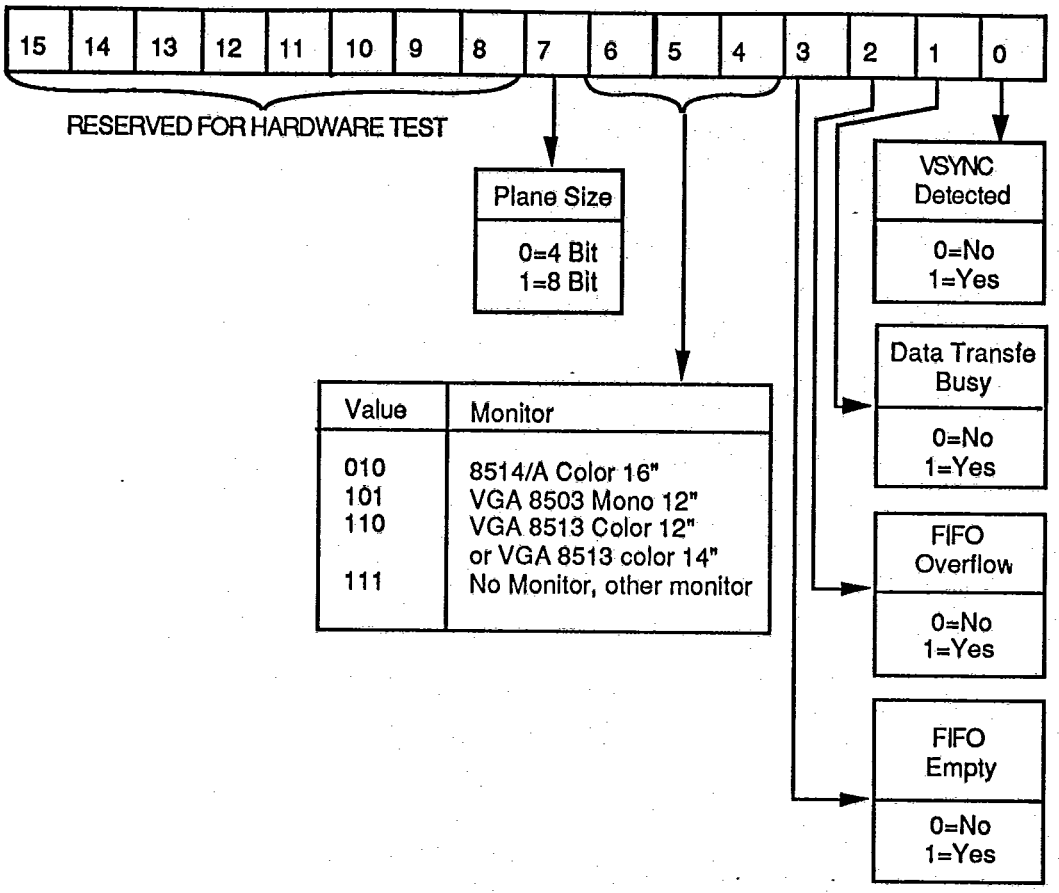

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Graphics Processor Status Register	Read Only
16-bit	Address 9AE8

The Graphics Processor Status Register provides status information concerning queue information, PC read data, and hardware busy.

Bits 7 to 0, FIFO Occupied, each bit indicates if the equivalent entity is not occupied (0) or occupied (1).

Bit 8, PC Read Data Available, is not available (0) or available (1).

Bit 9, IGA Busy, is no (0) or yes (1).

Bits 15 to 10 are unused.