

Typical Applications

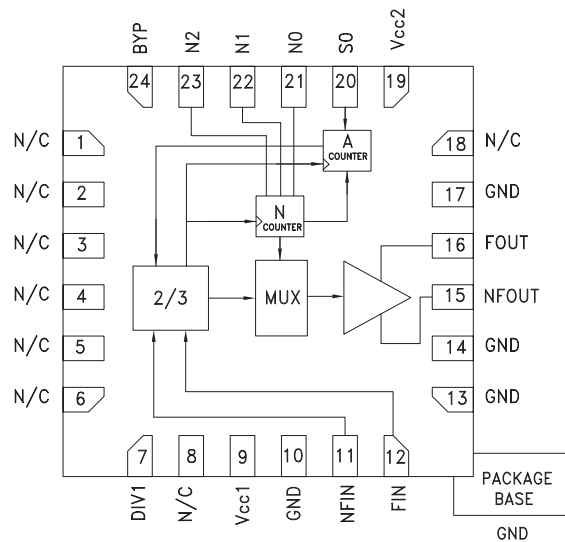
The HMC705LP4(E) is ideal for:

- Satellite Communication Systems
- Point-to-Point Radios
- Military Applications
- Sonet Clock Generation
- Test Equipment

Features

- Ultra Low SSB Phase Noise Floor: -153 dBc/Hz @ 100 kHz
- Programmable Divider (N= 1 - 17) Operating up to 6.5 GHz
- 24 Lead 4X4mm SMT Package: 16mm²

Functional Diagram



General Description

The HMC705LP4(E) is a low noise GaAs HBT programmable divider in a 4x4 mm leadless surface mount package. The divider can be programmed to divide by any number from N = 1 to N = 17 up to 6.5 GHz. The HMC705LP4E's high frequency operation along with low phase noise floor is very useful in high performance fast settling synthesizer architectures.

Electrical Specifications, $T_A = +25^\circ C$, $V_{cc} = V_{cc1} = V_{cc2} = +5V$

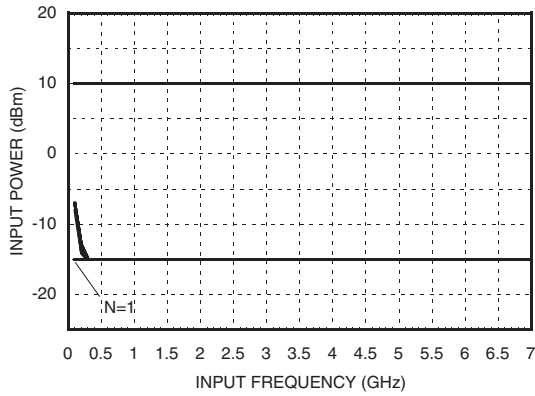
Parameter	Conditions	Min.	Typ.	Max.	Units
Maximum Input Frequency	Sine Wave or Square Wave Input	6.5			GHz
Minimum Input Frequency	Sine Wave or Square Wave Input			0.1	GHz
Input Power Range	Fin 0.1 to 6.5 GHz	-15	0	10	dBm
Output Power	Divide-by-2		0		dBm
SSB Phase Noise	Fin = 6 GHz, N = 17		-153		dBc/Hz
Total Supply Current			200		mA



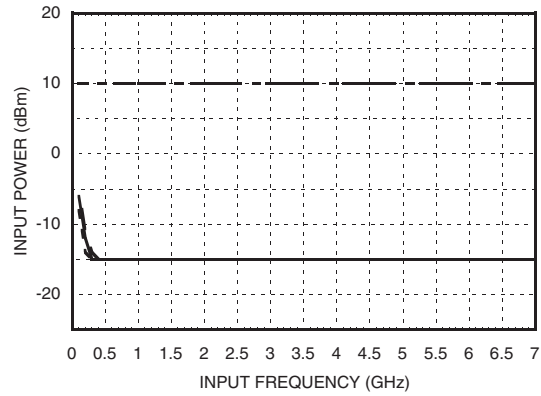
**6.5 GHz PROGRAMMABLE
DIVIDER (N = 1 - 17)**

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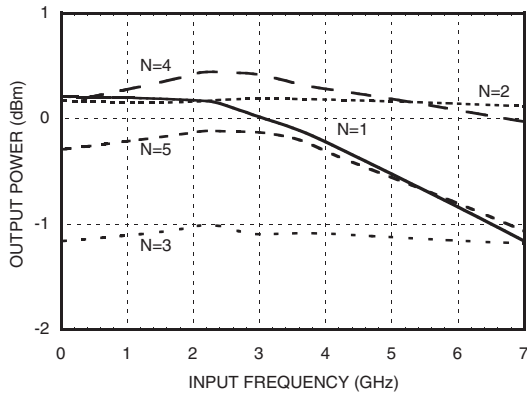
Input Sensitivity Window, All States



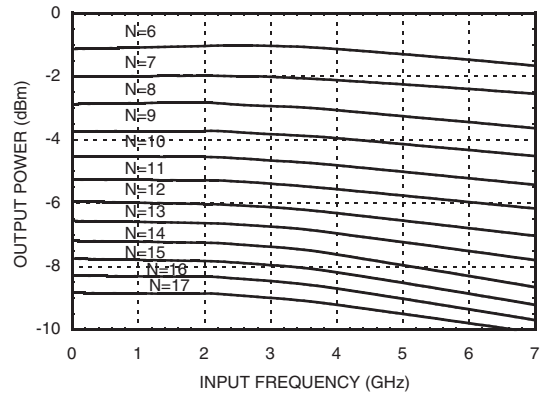
**Input Sensitivity Window vs. Temperature,
N = 17, T = -40°C to +85°C**



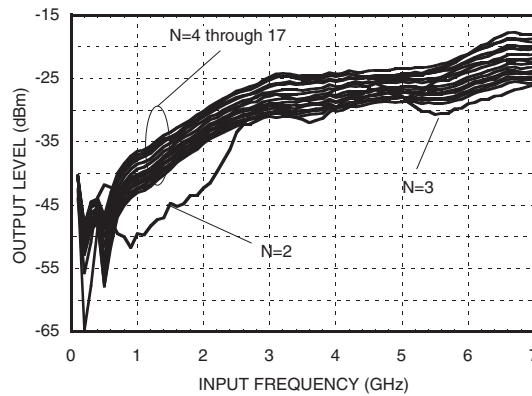
**Output Power, Divide Ratio
States 1 through 5**



**Output Power, Divide Ratio
States 6 through 17**

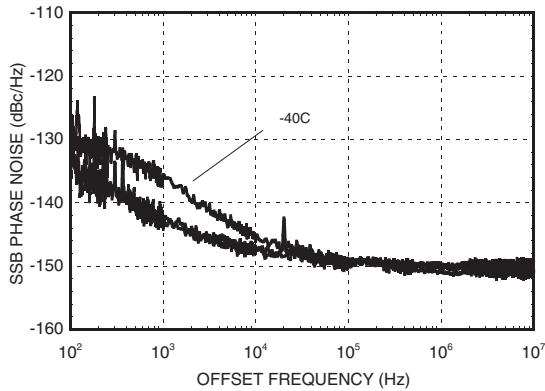


Fundamental Feedthru Power, Pin = 0 dBm



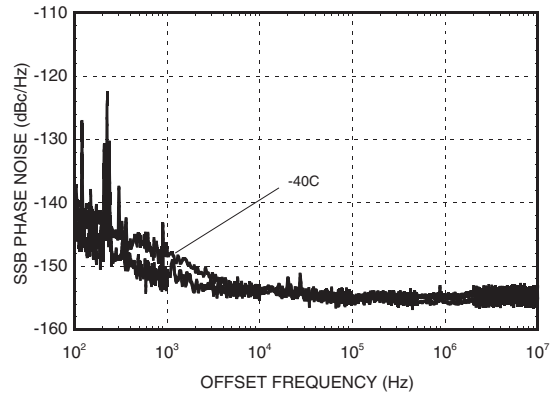
SSB Phase Noise Performance

$F_{in} = 6 \text{ GHz}$, $N = 2$; $T = -40^\circ\text{C}$, $+25^\circ\text{C}$, $+85^\circ\text{C}$



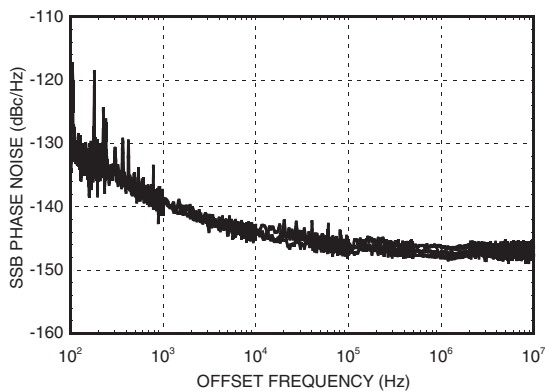
SSB Phase Noise Performance

$F_{in} = 6 \text{ GHz}$, $N = 17$; $T = -40^\circ\text{C}$, $+25^\circ\text{C}$, $+85^\circ\text{C}$



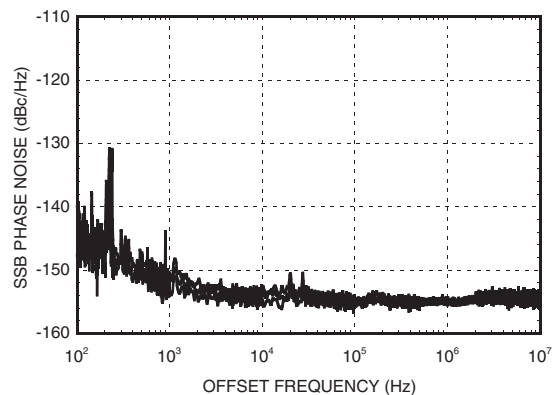
SSB Phase Noise Performance

$F_{in} = 6 \text{ GHz}$, $N = 2$; $V_{cc} = 4.75\text{V}$, 5V , 5.25V

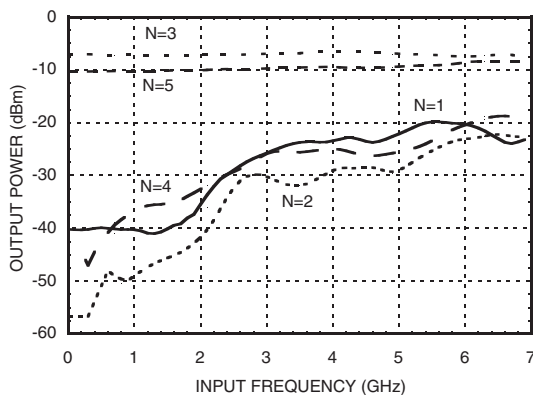


SSB Phase Noise Performance

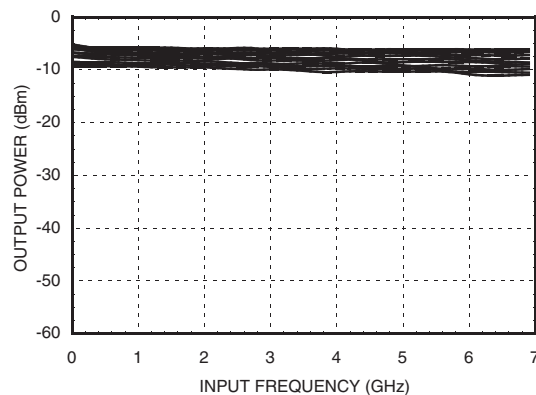
$F_{in} = 6 \text{ GHz}$, $N = 17$; $V_{cc} = 4.75\text{V}$, 5V , 5.25V



2nd Harmonic, N = 1 though 5

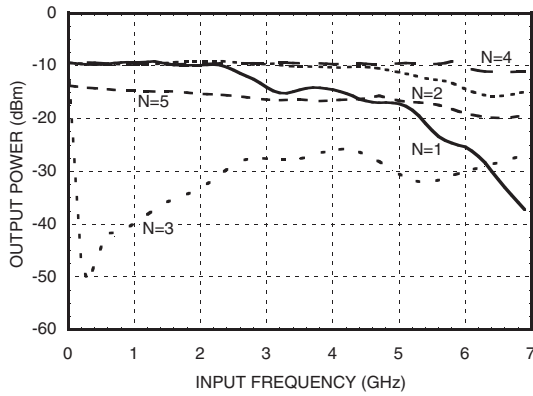


2nd Harmonic, N = 6 though 17

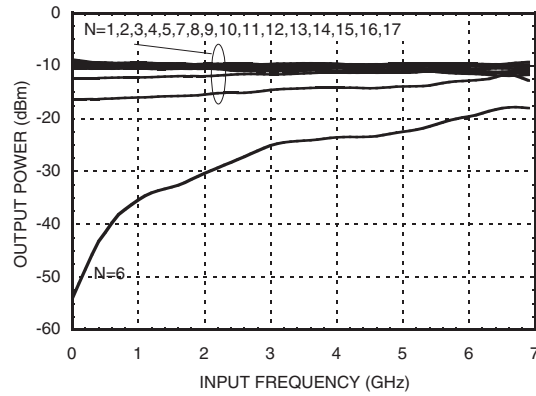


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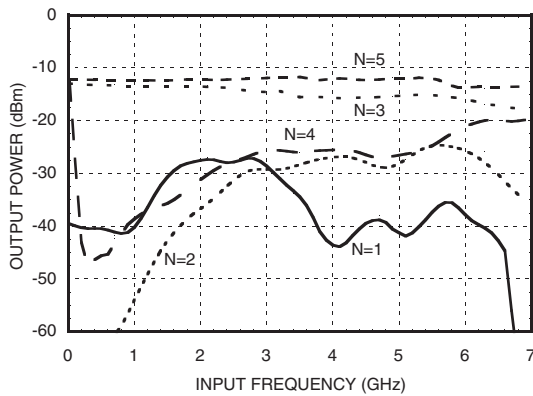
3rd Harmonic, N = 1 though 5



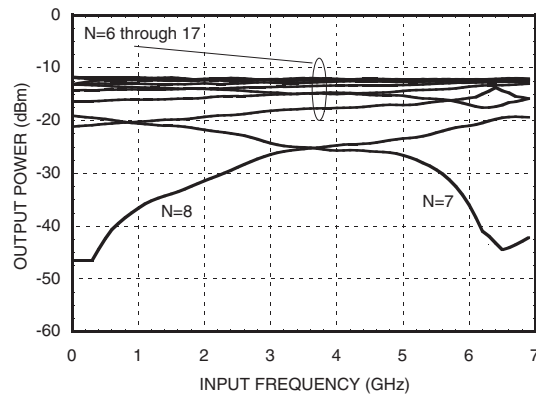
3rd Harmonic, N = 6 though 17



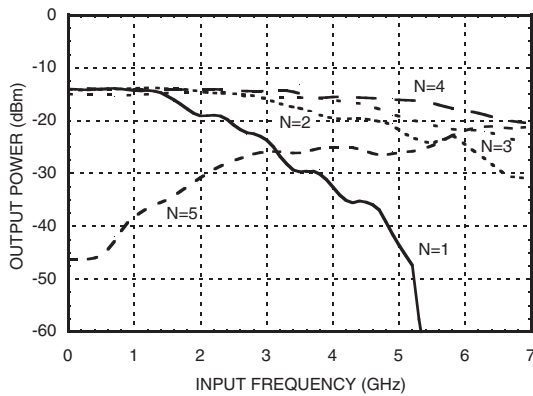
4th Harmonic, N = 1 though 5



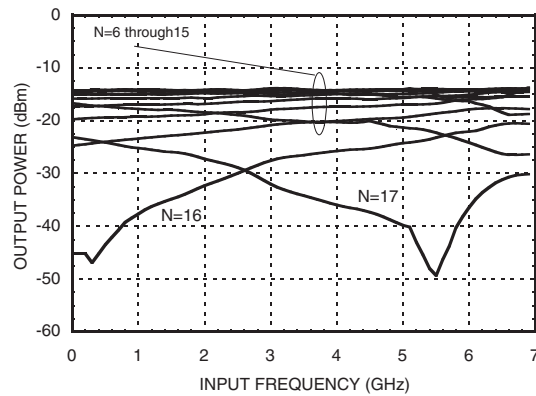
4th Harmonic, N = 6 though 17



5th Harmonic, N = 1 though 5



5th Harmonic, N = 6 though 17



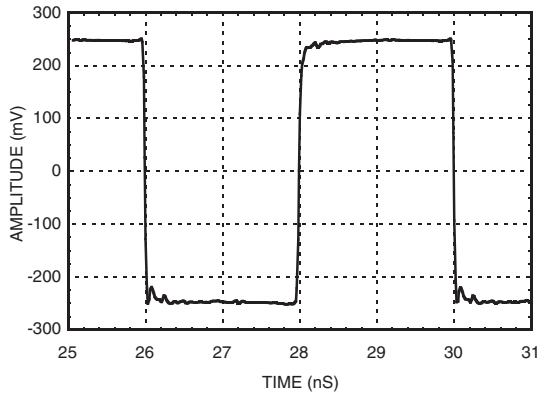


6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

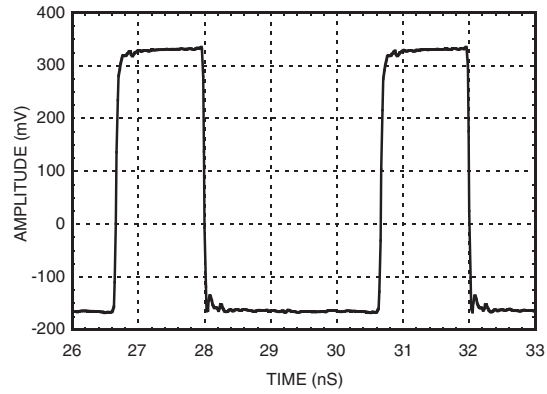
6

FREQUENCY DIVIDERS & DETECTORS - SMT

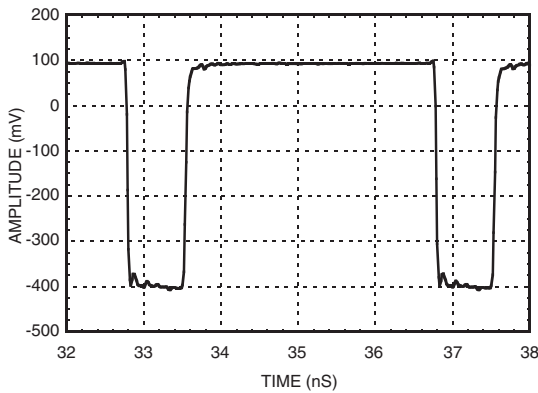
Output Voltage Waveform, $f_{in} = 500$ MHz, $N = 2$, $P_{in} = 0$ dBm, $T = 25$ °C



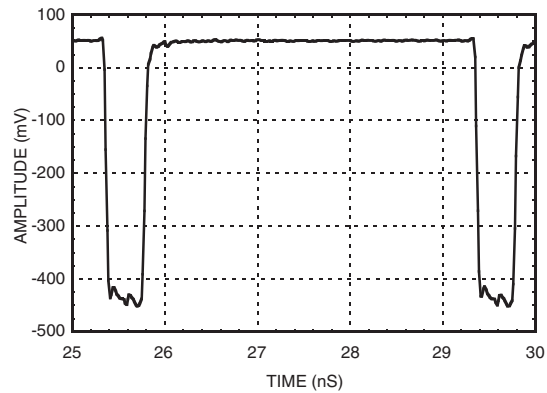
Output Voltage Waveform, $f_{in} = 750$ MHz, $N = 3$, $P_{in} = 0$ dBm, $T = 25$ °C



Output Voltage Waveform, $f_{in} = 2500$ MHz, $N = 10$, $P_{in} = 0$ dBm, $T = 25$ °C



Output Voltage Waveform, $f_{in} = 4250$ MHz, $N = 17$, $P_{in} = 0$ dBm, $T = 25$ °C



N	Duty Cycle %
1	Input
2	50
3 - 17	$[1 - (2/N)] \times 100$

Note:

- [1] Peak to peak amplitude does not change relative to N.
- [2] Pulse duty cycle changes relative to N.

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Absolute Maximum Ratings

RF Input (Vcc= +5V)	+13 dBm
Supply Voltage (Vcc)	+5.5V
Logic Inputs	-0.5V to (0.5V + Vcc)
Channel Temperature (Tc)	135 °C
Continuous P _{diss} (T = 85 °C) (derate 49 mW/° C above 85 °C)	2.4 W
Thermal Resistance (Junction to ground paddle)	20.5 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

Typical Supply Current vs. Vcc

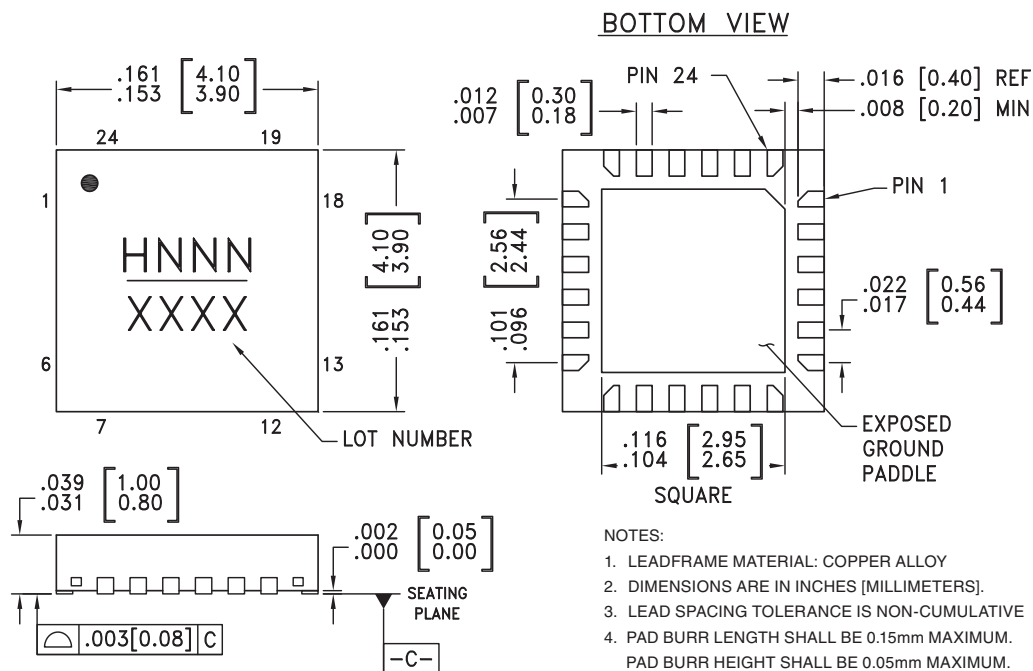
Vcc (V)	I _{cc} (mA)
4.75	180
5.00	200
5.25	210

Note: HMC705LP4E will work over full voltage range above.



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

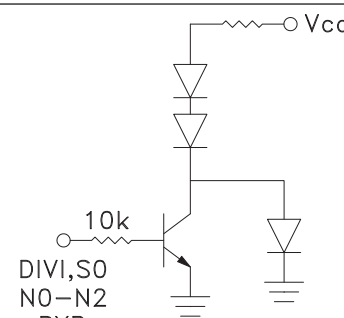
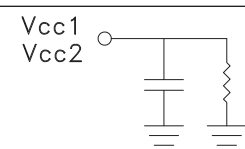


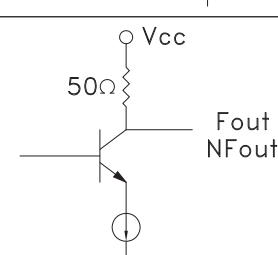


Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[3]
HMC705LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 ^[1]	H705 XXXX
HMC705LP4(E)	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H705 XXXX

[1] Max peak reflow temperature of 235 °C
 [2] Max peak reflow temperature of 260 °C
 [3] 4-Digit lot number XXXX

Pin Description

Pin Number	Function	Description	Interface Schematic
1 - 6, 8, 18	N/C	No Connection required. These pins may be connected to RF/DC ground without affecting performance.	
7, 20 - 24	DIV1, S0 N0 - N2 BYP	<p>PFD INVERT function</p> <p>CMOS compatible input control bit</p> <p>Logic "LOW" = NORMAL</p> <p>Logic "HIGH" = INVERT</p>	
9 - 19	Vcc1, Vcc2	Supply Voltage	
10, 13, 14, 17	GND	Package bottom must be connected to RF DC ground.	
11	NFIN	(These pins are AC coupled and must be DC Blocked externally.) Frequency Input	
12	FIN	Frequency Input Compliment	
15	NFout	Frequency, output compliment	
16	Fout	Frequency output	



MICROWAVE CORPORATION v00.0808



HMC705LP4 / 705LP4E

6.5 GHz PROGRAMMABLE DIVIDER (N = 1 - 17)

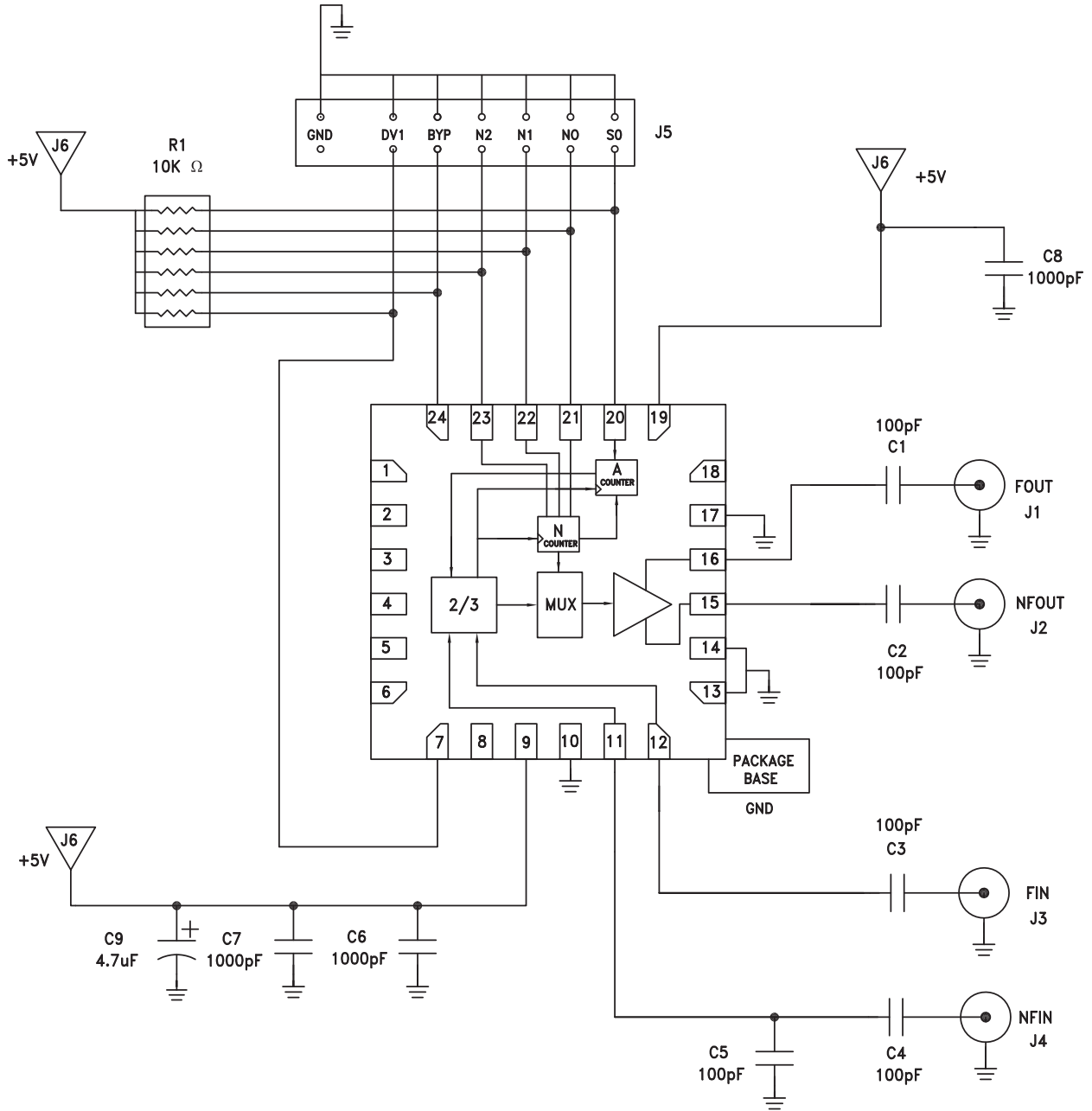
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HMC698LP5(E) Programming Truth Table

Division Ratio n	S0	N0	N1	N2	DIV 1	BYP
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	1	0	0	0	1	0
4	0	1	0	0	0	0
5	1	1	0	0	0	0
6	0	0	1	0	0	0
7	1	0	1	0	0	0
8	0	1	1	0	0	0
9	1	1	1	0	0	0
10	0	0	0	1	0	0
11	1	0	0	1	0	0
12	0	1	0	1	0	0
13	1	1	0	1	0	0
14	0	0	1	1	0	0
15	1	0	1	1	0	0
16	0	1	1	1	0	0
17	1	1	1	1	0	0

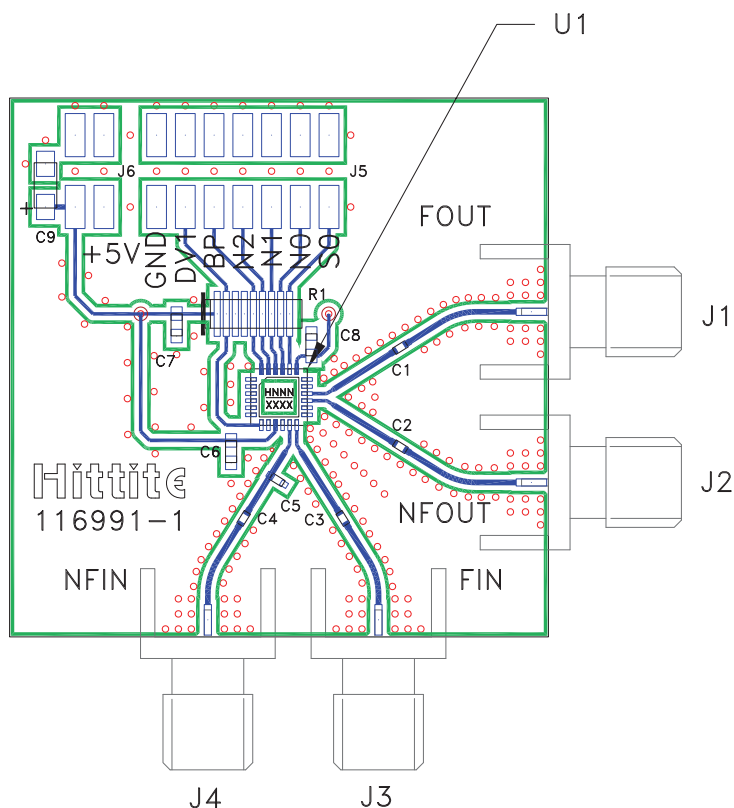
0 = Logic Low
1 = Logic High

Evaluation PCB Circuit



Evaluation PCB

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**List of Materials for
Evaluation PCB 116992 [1]**

Item	Description
J1 - J4	PCB Mount SMA Connector
J5	14 Position SMA Header Connector
J6	8 Position SMA Header Connector
R1	10K Ohm Resistor Network, Bissel SMD
C1 - C5	100 pF Capacitor, 0402 Pkg.
C6 - C8	1000 pF Capacitor, 0603 Pkg.
C9	4.7 μF Tantalum Capacitor, Case A
U1	HMC705LP4(E) Programmable Divider
PCB [2]	116991 Eval Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

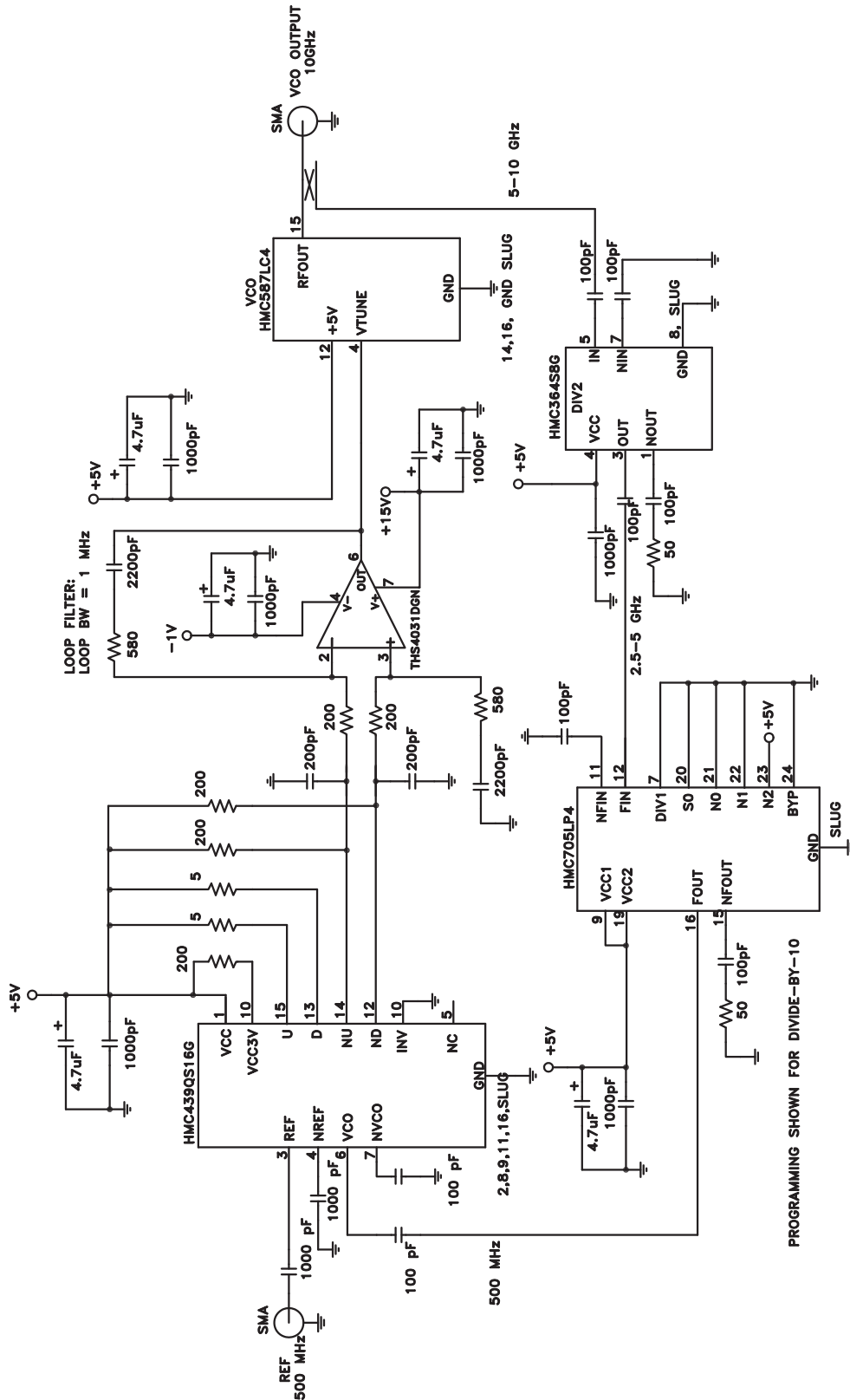
The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and backside ground slug should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.



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Typical PLL Application Circuit using HMC705LP4

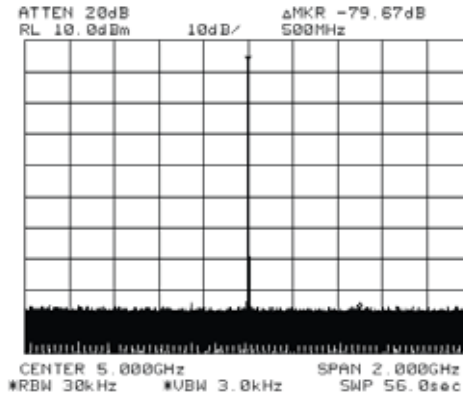
PLL application shown for Divide-by-10. Contact HMC to discuss your specific application.





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Typical Application Showing Spurious Performance



CMOS/TTL Input Characteristics

Maximum Input Logic "0" Voltage ($V_{IL\ MAXIMUM}$) = 1.1V @ 1 μ A.

Minimum Input Logic "1" Voltage ($V_{IH\ MINIMUM}$) = 1.8V @ 50 μ A.

Input IV characteristics for the logic inputs (S0, N0 - N2, DIV1, BYP) are shown below:

