HARRIS HC-5510/11

Monolithic CODECs

Features

- Industry Standard Pinout
- Low Power switched capacitor CMOS
- Low Operation Power ..... 45mW Typical
- Low Standby Power ..... 1mW Typical
- ±5V Operation
- TTL Compatible Digital Interface
- Time Slot Assignment or Alternate Fixed Time Slot Modes
- Internal Precision Reference
- Internal Sample and Hold Capacitors
- Internal Auto-Zero Circuit
- HC-5510-μ-Law Coding With Signaling Capabilities that meet Bell D3/D4 specifications
- HC-5511-A-Law Coding with Signaling Capabilities that meet CCITT specifications
- Synchronous or Asynchronous Operation

Applications

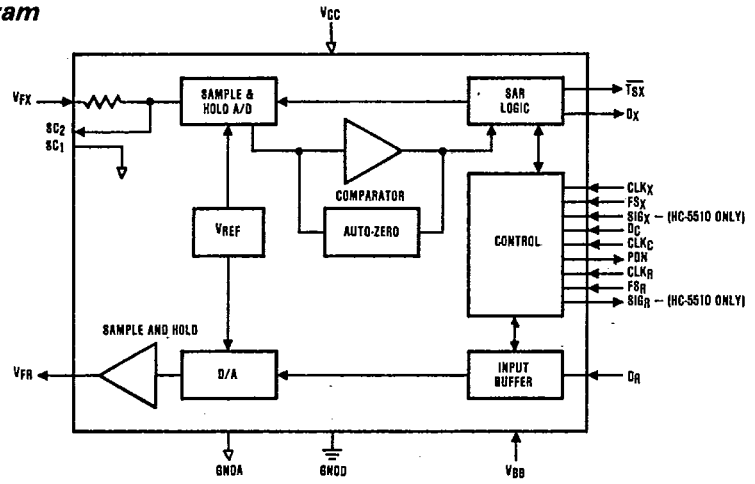
- Pulse Code Modulation Coding and Decoding for Digital PBX and Central Office Telecommunications Switching Systems
- Analog to Digital Conversion in MODEMs and Multiplexers
- Data Acquisition Systems

Description

The HC-5510 and HC-5511 are monolithic PCM CODECs implemented with double-poly CMOS technology. The HC-5510 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The HC-5511 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the HC-5510/HC-5511 may be operated in a fixed time slot mode. Both devices are ideal for use with the HC-5512/12A/12C/12D monolithic PCM filters, which provide the input anti-aliasing function for the encoder, smooth the output of the decoder, and correct for the sin x/x distortion introduced by the decoder sample and hold output. All devices may be used with the Harris Family of Subscriber Line Interface Circuits (SLICs), including the HC-5502A, HC-5504 and HC-5508. Application Notes are available.

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Operating Temperature	-25°C to +125°C
Storage Temperature	-65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	-7V
Voltage at Any Input or Output	V_{BB} -0.3V to V_{CC} +0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0V ± 5%, V_{BB} = -5.0V ± 5%. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = -5.0V and T_A = 25°C. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
DIGITAL INTERFACE						
I_I	Input Current	-10		10	µA	$0 < V_{IN} < V_{CC}$
V_{IL}	Input Low Voltage			0.6	V	
V_{IH}	Input High Voltage	2.2			V	
V_{OL}	Output Low Voltage			0.4	V	D_X, I_{OL} = 4.0mA
				0.4	V	SIG_R, I_{OL} = 0.5mA
				0.4	V	$\overline{TS}_X$, I_{OL} = 3.2mA, Open Drain
				0.4	V	PDN, I_{OL} =1.6mA
V_{OH}	Output High Voltage	2.4			V	D_X, I_{OH} = 6mA
		2.4			V	SIG_R, I_{OH} = 0.6mA
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	2.0			kΩ	Resistance in Series with Approximately 70pF
Z_O	Output Impedance at VF_R		10	20	Ω	-3.1V < VF_R < 3.1V
V_{OS}	Output Offset Voltage at VF_R	-25		25	mV	D_R = PCM Zero Code, HC-5510 or Alternating ±1 Code, HC-5511
I_{IN}	Analog Input Bias Current	-0.1		0.1	µA	V_{IN} = 0V
R1 x C1	DC Blocking Time Constant	4.0			ms	
C1	DC Blocking Capacitor	0.1			µF	
R1	Input Bias Resistor			160	kΩ	
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}		0.1	0.4	mA	
I_{BB0}	Standby Current, V_{BB}		0.03	0.1	mA	
I_{CC1}	Operating Current, V_{CC}		4.5	8.0	mA	
I_{BB1}	Operating Current, V_{BB}		4.5	8.0	mA	

A.C. Electrical Characteristics

Unless otherwise noted, the analog input is a 0dBm0, 1.02kHz sine wave. The digital input is a PCM bit stream generated by passing a 0dBm0, 1.02kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
	Absolute Level					The nominal 0dBm0 levels for the HC-5510 and HC-5511 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the HC-5510/ HC-5511 are based on these nominal levels after the necessary sin x/x corrections are made.
G_{RA}	Receive Gain, Absolute	-0.125		0.125	dB	T = 25°C, V_{CC} =+5V,V_{BB} = -5V
G_{RAT}	Absolute Receive Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 75°C
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} =-5V±5%
G_{XA}	Transmit Gain, Absolute	-0.325		-0.075	dB	T = 25°C, V_{CC} = 5V, V_{BB} = -5V
G_{XAT}	Absolute Transmit Gain Variation with Temperature	-0.05		0.05	dB	T = 0°C to 75°C
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	-0.07		0.07	dB	V_{CC} = 5V ±5%, V_{BB} = -5V ±5%
G_{RAL}	Absolute Receive Gain Variation with Level	 -0.3 -0.2 -0.4 -1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
G_{XAL}	Absolute Transmit Gain Variation with Level	 -0.3 -0.2 -0.4 -1.0		 0.3 0.2 0.4 1.0	 dB dB dB dB	CCITT Method 2 Relative to -10dBm0 0dBm0 to 3dBm0 -40dBm0 to 0dBm0 -50dBm0 to -40dBm0 -55dBm0 to -50dBm0
S/D_R	Receive Signal to Distortion Ratio	 35 29 25			 dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
S/D_X	Transmit Signal to Distortion Ratio	 35 29 25			 dBc dBc dBc	Sinusoidal Test Method Input Level -30dBm0 to 0dBm0 -40dBm0 -45dBm0
N_R	Receive Idle Channel Noise			 6 -84	 dBnrc0 dBm0p	D_R = Steady State PCM Code HC-5510 HC-5511
N_X	Transmit Idle Channel Noise			13 -67	dBrnc0 dBm0p	HC-5510, VF_X = 0V (no signaling) HC-5511, VF_X = 0V
HD_R	Receive Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
HD_X	Transmit Harmonic Distortion			-47	dB	2nd or 3rd Harmonic
$PPSR_R$	Positive Power Supply Rejection, Receive	40			dB	D_R = Steady PCM Code, V_{CC} = $5.0V_{DC}$ + 200mVrms, f = 1.02kHz
$PPSR_X$	Positive Power Supply Rejection, Transmit	50			dB	Input Level = 0V, V_{CC} = $5.0V_{DC}$ + 200mVrms, f = 1.02kHz
$NPSR_R$	Negative Power Supply Rejection, Receive	45			dB	D_R = Steady PCM Code, V_{BB} = $-5.0V_{DC}$ +200mVrms, f = 1.02kHz
$NPSR_X$	Negative Power Supply Rejection Transmit	50			dB	Input Level = 0V , V_{BB} = $-5.0V_{DC}$ + 200mVrms, f = 1.02kHz
CT_{XR}	Transmit to Receive Crosstalk			-75	dB	D_R = Steady PCM Code
CT_{RX}	Receive to Transmit Crosstalk			 -70 -65	 dB dB	Transmit Input Level = 0V HC-5510 HC-5511

Timing Specifications

Unless otherwise noted, T_A = 0°C to 75°C, V_{CC} = 5.0 ±5%, V_{BB} = -5.0 ±5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the timing waveforms.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
t_{PC}	Period of Clock	485			ns	CLK_C, CLK_R, CLK_X
t_{RC}, t_{FC}	Rise and Fall Time of Clock			30	ns	CLK_C, CLK_R, CLK_X
t_{WCH}	Width of Clock High	165			ns	CLK_C, CLK_R, CLK_X
t_{WCL}	Width of Clock Low	165			ns	CLK_C, CLK_R, CLK_X
$t_{A/D}$	A/D Conversion Time			16	Time Slots	From End of Encoder Time Slot to Completion of Conversion
$t_{D/A}$	D/A Conversion Time			2	Time Slots	From End of Decoder Time Slot to Transition of VF_R
t_{SDC}	Set-Up Time, D_C to CLK_C	100			ns	
t_{HDC}	Hold Time, CLK_C to D_C	100			ns	
t_{SFC}	Set-Up Time, FS_X or CLK_X	100			ns	
t_{HFX}	Hold Time, CLK_X to FS_X	100			ns	
t_{DZX}	Delay Time to Enable D_X on TS Entry	25		125	ns	C_L = 150pF
t_{DDX}	Delay Time, CLK_X to D_X			125	ns	C_L = 150pF
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	50		165	ns	C_L = 0pF
t_{DTSL}	Delay to $\overline{TS}_X$ Low	30		185	ns	$0 \leq C_L \leq 150pF$
t_{DTSH}	Delay to $\overline{TS}_X$ Off	30		185	ns	C_L = 0pF
t_{SSX}	Set-Up Time, SIG_X to CLK_X	100			ns	
t_{HSX}	Hold Time, CLK_X to SIG_X	100			ns	
t_{SFR}	Set-Up Time, FS_R to CLK_R	100			ns	
t_{HFR}	Hold Time, CLK_R to FS_R	100			ns	
t_{SDR}	Set-Up Time, D_R to CLK_R	40			ns	
t_{HDR}	Hold Time, CLK_R to D_R	30			ns	
t_{DSR}	Delay Time, CLK_R to SIG_R			300	ns	C_L = 100pF

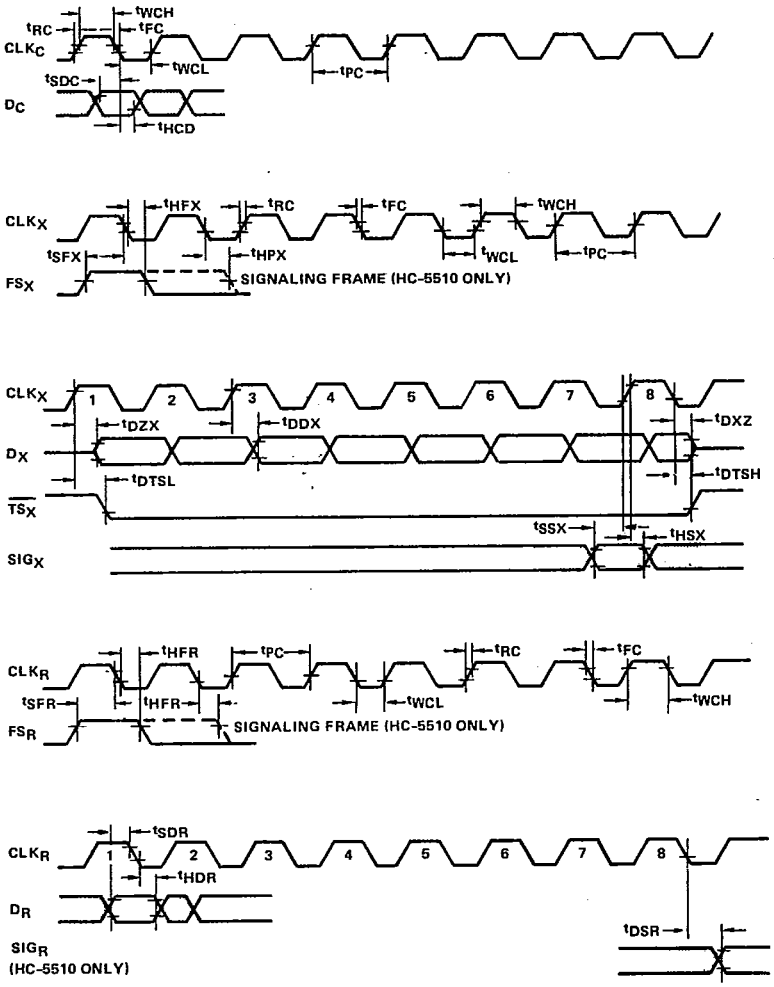
HC-5510 Pin Assignments

PIN NO.	SYMBOL	DESCRIPTION
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample / hold capacitor if fitted for use with pin compatible NMOS CODEC. Insures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin. Must be same potential as GNDD.
6	SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output-SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused
13	GNDD	Digital ground. All digital levels are referenced to this pin. Must be same potential as GNDA.
14	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V (±5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
22	V_{BB}	-5V (±5%) input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

HC-5511 Pin Assignments

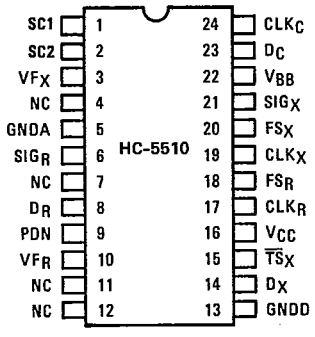
PIN NO.	SYMBOL	DESCRIPTION
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample / hold capacitor if fitted for use with pin compatible NMOS CODEC. Insures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin. Must be same potential as GNDD.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DR, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15μs after the end of the decode time slot.
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin. Must be same potential as GNDA.
13	D_X	Serial PCM "Three-State" output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most signficant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external "Three-State" bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	5V (±5%) input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536MHz, 1.544MHz or 2.048MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536MHz, 1.544MHz, or 2.048MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	-5V (±5%) input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the HC-5510/HC-5511 into the fixed time slot mode.

Timing Waveforms

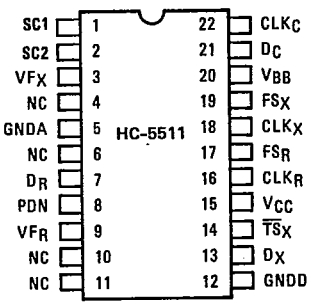


Pinouts

TOP VIEW



TOP VIEW



Functional Description

Power-Up

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or -5V is required. In the power-down mode, all non-essential circuits are deactivated, the "Three-State" PCM data output D_X is placed in the high impedance state and the receive signaling output of the HC-5510, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the HC-5510/5511 depends on the chosen mode of operation, time slot assignment or fixed time slot.

Time Slot Assignment Mode

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated, the PCM data will appear at the output pin during the previously assigned time slot which may now be assigned to another CODEC.

Fixed Time Slot Mode

There are several ways in which the HC-5510/5511 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

Serial Control Port

When the HC-5510/HC-5511 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	ACTION
0	0	Assign Time Slot to Encoder and Decoder
0	1	Assign Time Slot to Encoder
1	0	Assign Time Slot to Decoder
1	1	Power-Down CODEC

B3	B4	B5	B6	B7	B8	TIME SLOT
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

Signaling

The HC-5510 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "1/2" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

Encoding Delay

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048MHz clock, the FS_X rate could be increased to 15kHz, reducing the delay from 125μs to 67μs.

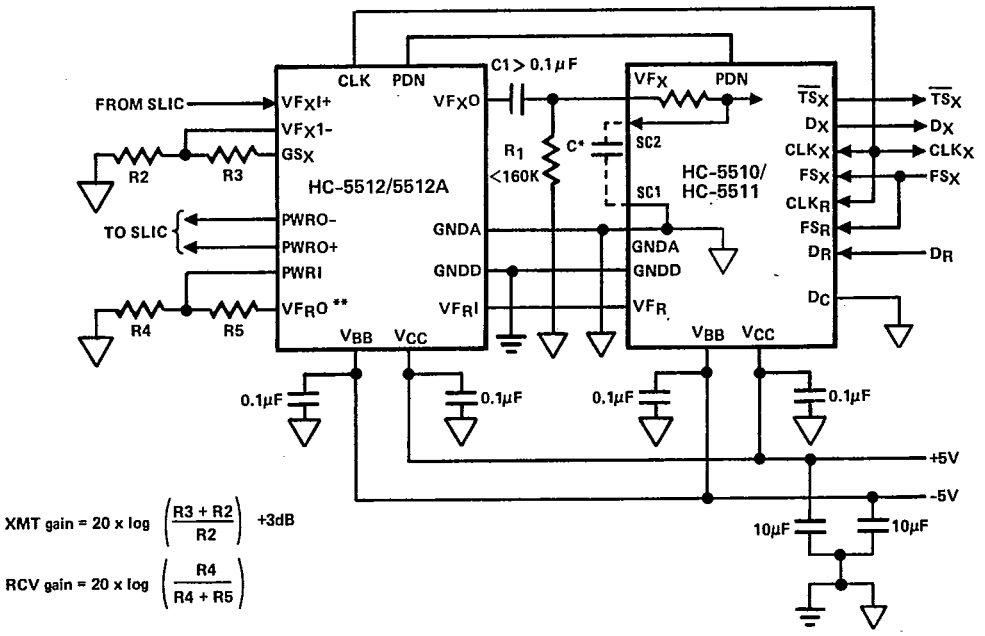
Decoding Delay

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81μs for a 1.544MHz system with an 8kHz frame rate or 76μs for a 2.048MHz system with an 8kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

Typical Application

A typical application of the HC-5510/11 used in conjunction with the HC-5512/12A PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are noncritical. The capacitor value should exceed 0.1μF, R1 should be less than 160kΩ, and the product R1 x C1 should exceed 4ms.

Typical Application



The power supply decoupling capacitors should be 0.1μF. In order to take advantage of the excellent noise performance of the HC-5510/HC5511/HC-5512, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. The above application is configured for a fixed time slot mode of operation.

* The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pins connect VF_X to this sample/hold capacitor (via a 300 Ω resistor) to ensure gain compatibility. The HC-5510/11 itself does not require an external sample/hold capacitor.

** For use with Monolithic Slics, such as HC-5502A, HC-5504 and HC-5508. The output may be taken directly at VF_RO.