

FEATURES

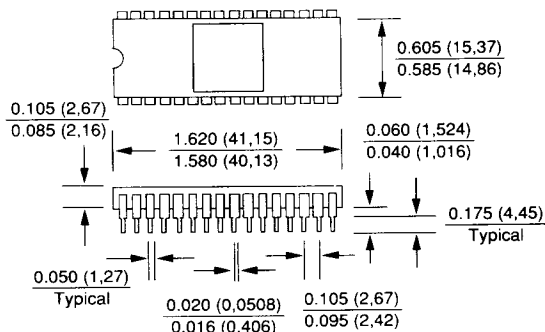
- Digital tuning
- Stopband attenuation >76dB at 3°C
- Built-in sample-hold
- Programmable gain of 1, 2, 4, 8
- Dynamic range of 85dB
- 12-Bit precision

DESCRIPTION

DATEL's Model FLT-C1 is a monolithic, 7th order, lowpass active filter for applications requiring sharp, fast attenuation rolloff. Exceptionally low noise performance of this switched capacitor filter permit it to be used in applications requiring 12-bit accuracy.

A combination of an 8-bit control input and the clock frequency set the corner frequency over a range of 78 Hz to 20 KHz. A 2-bit control input selects the gain. A built-in oscillator (less crystal) is provided for systems where a system clock is not available.

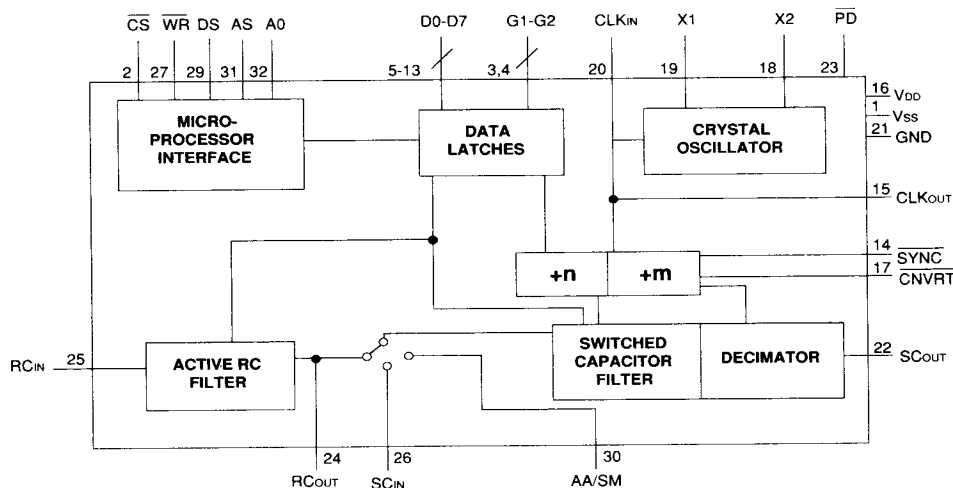
FLT-C1 Mechanical Dimensions



ORDERING INFORMATION

MODEL DESCRIPTION

FLT-C1 7th Order, Low-pass, Switched Capacitor Active Filter



FUNCTIONAL SPECIFICATIONS

Typical at 25 °C range unless otherwise noted. Specifications subject to change without notice.

FILTER CHARACTERISTICS	
Frequency Range	78 Hz to 20 KHz
Voltage Gain	1, 2, 4, or 8
Gain Accuracy (G=1)	±0.1%
Offset Voltage (G=1)	5 mV
Filter Response (Relative to DC Gain)	7-pole Chebychev
at 1.5 fc	-30 dB max.
at 2 fc	-52 dB max.
at 3 fc	-76 dB max.
Input Signal Level	±3V min.
Output Voltage	±3V
Output Current	±0.6 mA
Passband Ripple	±0.1dB
Band edge Tolerance	±0.5%
Wideband Noise, 20 KHz, BW	100 µVrms max.
Harmonic Distortion	-72 dB
Dynamic Range	85dB min.
CLOCK	
Input Clock Frequency ①	1 MHz min. 4 MHz typ.
DIGITAL INPUTS	
Input High	2.0V min.
Input Low	0.8V max.
Leakage Current	1 µA max.
Input Capacitance	10 pF max.
POWER SUPPLY REQUIREMENTS	
Supply Voltage	±5V (±5%)
Supply Current	±15 mA
Power Dissipation	150 mW

① Also internal clock frequency. Internal clock requires external crystal.

FUNCTIONAL DESCRIPTION

The FLT-C1 is made up of two programmable filter sections used in different combinations to meet various applications.

The **switched capacitor stage** (SCF), is a 7-pole, lowpass filter designed to provide an accurate, programmable passband for fixed or dynamic applications.

The switching frequency may be derived either from a crystal oscillator or from a system clock. Since the filter band edge can be programmed by varying the frequency of the clock which controls the filter's switches, it can track the sample rate of an external A/D converter. Digital programming allows for band edges of up to 20 KHz and gains of 1, 2, 4, or 8.

The **RC filter stage** is a low-order active filter with a band-edge accuracy of 5%. This accuracy is adequate because the filter sampling rate is 50 times greater than the band edge frequency.

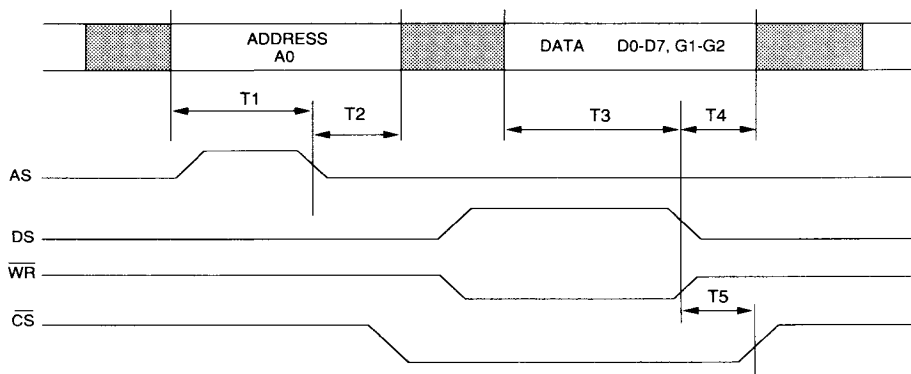
Pin Functions

Name	Function
Vss	Negative supply voltage.
CS	Chip select; active low.
G1-G2	The digital inputs that control the DC gain of the SC filter.
D0-D7	The digital inputs that control the RC filter band edge, SC filter band edge, and SC filter decimation rate.
SYNC	This digital input controls the sampling instant for the SC filter decimated output; active low.
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
CNVRT	This digital output indicates that the SCOUT output has settled and can now be converted or sampled (drive capability is 1 standard TTL load); active low.
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation.
CLKIN	The master clock input. Forcing CLKIN to Vss enables the on-chip oscillator (external crystal).
GND	Ground.
SCOUT	SC filter output.
PD	This digital input is used to power down the analog circuitry; active low.
RCOUT	RC filter output.
RCIN	RC filter input.
SCIN	SC filter input (only valid when AA/SM is forced low).
WR	Write strobe; active low.
DS	Data strobe.
AA/SM	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN.
AS	Address strobe.
A0	Register address select.

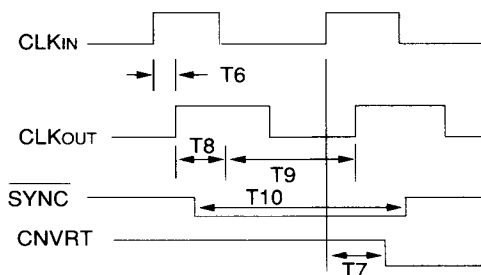
The band edge of the RC filter is programmable to insure sufficient rejection of any SC filter harmonics. Ratio matching of on-chip resistors and capacitors provides eight RC filter band-edges spanning a 12-to-1 range.

A decimator, placed at the output of the SC filter, samples the differential output and converts it to a single-ended signal. In addition, the decimator can be programmed to allow an integer decrease in the sampling rate by low filtering of the signal and keeping every Nth sample, similar to a programmable sample-and-hold. By choosing the proper decimation rate, the hold time at SCOUT will be long enough to allow an A/D conversion to take place without the need of external S/H components. An external S/H is recommended for hold times faster than 100 µs to prevent more than 1/2 LSB of droop for a 12-bit A/D conversion.

Microprocessor Interface Timing Characteristics



SC_{OUT} Synchronization Timing



μP Interface Timing	Ref.	Duration
CS Hold Time	T5	10 nSec. min.
Data Hold Time	T4	10 nSec. min.
Data Set-up Time	T3	100 nSec. min.
Address Hold Time	T2	10 nSec. min.
Address Set-up Time	T1	20 nSec. min.

SC _{OUT}	Ref.	Duration
Synchronization Timing		
SyncB Delay Time	T8	100 nSec. min.
SyncB Set-up Time	T9	75 nSec. min.
CLKIN To CLKOUT Delay	T6	50 nSec. max.
CLKIN To CNVRT Delay	T7	75 nSec. max.
Sync Pulse Width	T10	75 nSec. min.

RCF band edge				DC Gain		
RCF 3dB BW	D7	D6	D5	DC Gain	G1	G2
80 KHz	0	0	0	1	1	1
56KHz	0	0	1	2	1	0
40KHz	0	1	0	4	0	1
28KHz	0	1	1	8	0	0
14KHz	1	0	1			
10KHz	1	1	0			
7KHz	1	1	1			
Clock to SCF bandedge Divide Down Ratio				Decimator Sample Rate		
f_{CLK}/f_c	D0	D1	D2	f_{SH}/f_c	D3	D4
200	0	0	0	25.000	0	0
400	0	0	1	12.500	0	1
800	0	1	0	6.250	1	0
1,600	0	1	1	4.167	1	1
3,200	1	0	0			
6,400	1	0	1			
12,800	1	1	X			

f_c = 0.1dB Bandwidth of the SC filter.
f_{CLK} = Master clock frequency at CLKOUT
f_{SH} = Sample rate at SC_{OUT} output.

TOP VIEW

1	VSS	A0	32
2	CS	AS	31
3	G1	AA/SM	30
4	G2	DS	29
5	D5	N/C	28
6	D6	WR	27
7	D7	SC _{IN}	26
8	D0	RC _{IN}	25
9	D1	RC _{OUT}	24
10	D2	PD	23
11	D3	SC _{OUT}	22
12	N/C	GND	21
13	D4	CLK _{IN}	20
14	SYNC	X1	19
15	CLK _{OUT}	X2	18
16	VDD	CNVRT	17