Am7920

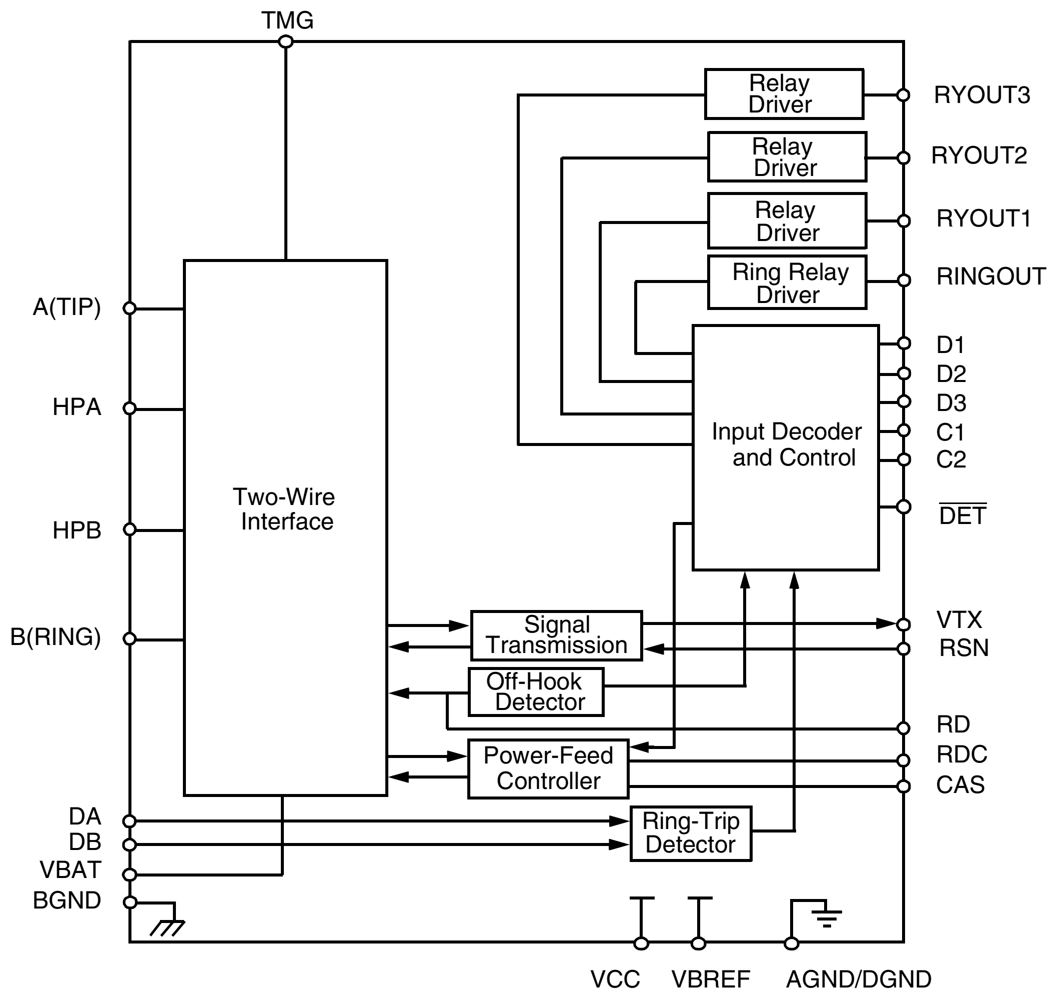
Subscriber Line Interface Circuit

The Am7920 Subscriber Line Interface Circuit implements the basic telephone line interface functions, and enables the design of low cost, high performance, POTS line interface cards.

DISTINCTIVE CHARACTERISTICS

- **Control states: Active, Ringing, Standby, and Disconnect**
- **Low standby power (35 mW)**
- **–19 V to –58 V battery operation**
- **On-hook transmission**
- **Two-wire impedance set by single external impedance**
- **Programmable constant-current feed**
- **Programmable loop-detect threshold**
- **Programmable ring-trip detect threshold**
- **No –5 V supply required**
- **Current Gain = 500**
- **On-chip Thermal Management (TMG) feature**
- **Four on-chip relay drivers and relay snubbers, 1 ringing and 3 general purpose (32 PLCC)**

BLOCK DIAGRAM



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Issue Date: **October 1999**

ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

Am7920 –1 S C

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)*

PACKAGE TYPE
J = 32-pin Plastic Leaded Chip Carrier (PL 032)
S = 28-pin Small Outline Integrated Circuit (SOW 028)

PERFORMANCE GRADE
–1 53 dB Longitudinal Balance
–2 63 dB Longitudinal Balance

DEVICE NUMBER/DESCRIPTION
Am7920
Subscriber Line Interface Circuit

Valid Combinations		
Am7920	–1 –2	JC SC

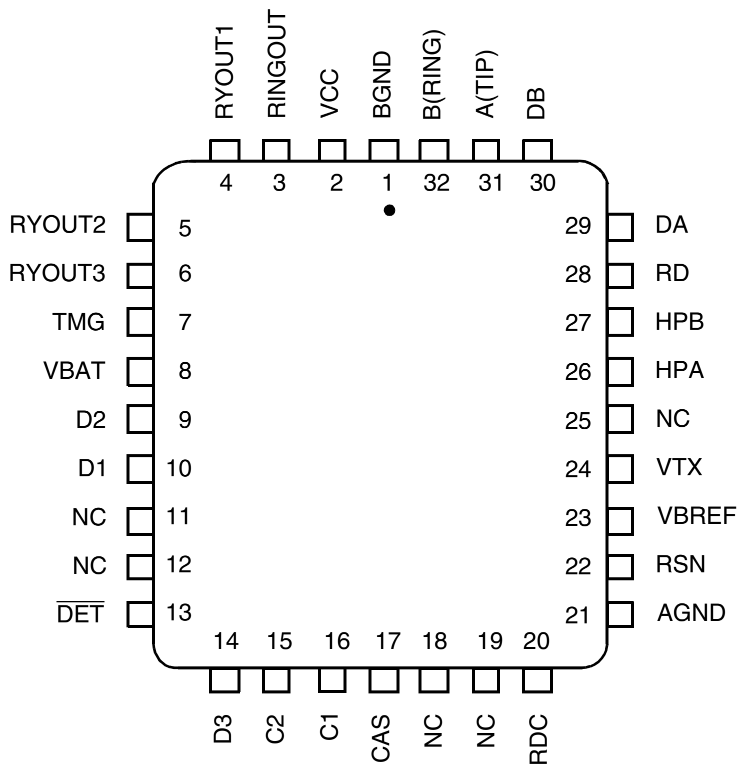
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military–grade products.

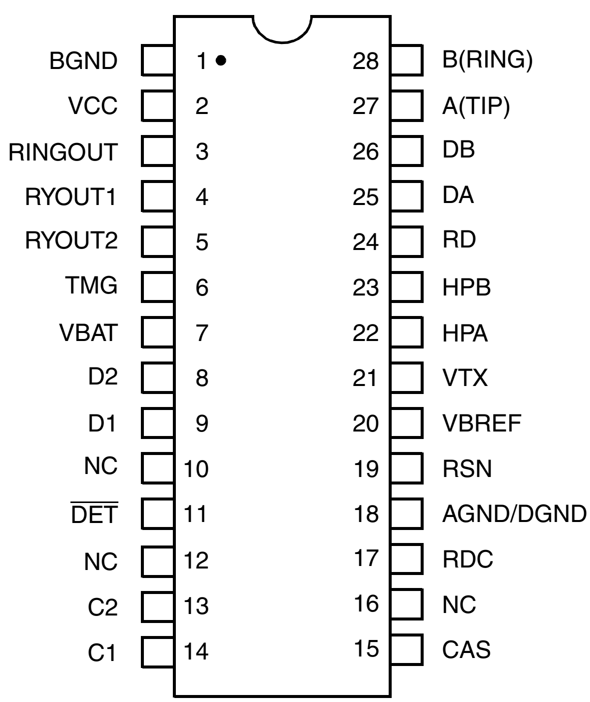
Note:
** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

CONNECTION DIAGRAMS

Top View



28-Pin SOIC



Notes:
1. Pin 1 is marked for orientation.
2. NC = No Connect

PIN DESCRIPTIONS

Pin Name	Type	Description
AGND/DGND	Ground	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Ground	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C2–C1	Inputs	Decoder. TTL compatible. C2 is MSB and C1 is LSB.
CAS	Capacitor	Anti-Saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
D3–D1	Input	Relay Driver Control. D3–D1 control the relay drivers RYOUT1, RYOUT2, and RYOUT3. Logic Low on D1 activates the RYOUT1 relay driver. Logic Low on D2 activates the RYOUT2 relay driver. Logic Low on D3 activates the RYOUT3 relay driver. TTL compatible.
DA	Input	Ring-trip negative. Negative input to ring-trip comparator.
DB	Input	Ring-trip positive. Positive input to ring-trip comparator.
DET	Output	Switchhook detector. Logic Low indicates that selected detector is tripped. Logic inputs C2–C1, E1, and E0 select the detector. Open-collector with a built-in 15 kΩ pull-up resistor.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No Connect. Pin not internally connected.
RD	Resistor	Detect resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open-collector driver with emitter internally connected to BGND.
RSN	Input	Receive Summing Node. The metallic current (both AC and DC) between A(TIP) and B(RING) is equal to 500 times the current into this pin. The networks that program receive gain, two-wire impedance, and feed resistance all connect to this node.
RYOUT1	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND.
RYOUT2	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND (PLCC only).
RYOUT3	Output	Relay/Switch Driver. Open-collector driver with emitter internally connected to BGND (PLCC only).
TMG	—	Thermal Management. External resistor connects between this pin and VBAT to offload power from SLIC.
VBAT	Battery	Battery supply and connection to substrate.
VBREF	—	This is an Legerity reserved pin and must always be connected to the VBAT pin.
VCC	Power	+5 V power supply.
VTX	Output	Transmit Audio. This output is a 0.50 gain version of the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

ABSOLUTE MAXIMUM RATINGS

Storage temperature .... –55°C to +150°C

V_{CC} with respect to AGND/DGND ..... –0.4 V to +7.0 V

V_{BAT} with respect to AGND/DGND:

Continuous.................................... +0.4 V to –70 V
10 ms .... +0.4 V to –75 V

BGND with respect to AGND/DGND........ +3 V to –3 V

A(TIP) or B(RING) to BGND:

Continuous .... V_{BAT} to +1 V
10 ms (f = 0.1 Hz) .... –70 V to +5 V
1 μs (f = 0.1 Hz) .... –80 V to +8 V
250 ns (f = 0.1 Hz) .... –90 V to +12 V

Current from A(TIP) or B(RING).................... ±150 mA

RINGOUT/RYOUT1,2,3 current........................ 50 mA

RINGOUT/RYOUT1,2,3 voltage .... BGND to +7 V

RINGOUT/RYOUT1,2,3 transient .... BGND to +10 V

DA and DB inputs

Voltage on ring-trip inputs.................... V_{BAT} to 0 V
Current into ring-trip inputs .... ±10 mA

C2–C1 and D3–D1

Input voltage .... –0.4 V to V_{CC} + 0.4 V

Maximum power dissipation, continuous,
T_A = 70°C, No heat sink (See note)

In 32-pin PLCC package............................... 1.7 W

Thermal Data:... θ_{JA}

In 32-pin PLCC package...................... 43°C/W typ

ESD immunity/pin (HBM) .... 1500 V

Note: *Thermal limiting circuitry on-chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability. See the SLIC Packaging Considerations for more information.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient temperature .... 0°C to +70°C*

V_{CC} .... 4.75 V to 5.25 V

V_{BAT} .... –19 V to –58 V

AGND/DGND .... 0 V

BGND with respect to
AGND/DGND .... –100 mV to +100 mV

Load resistance on VTX to ground .... 20 kΩ min

The operating ranges define those limits between which the functionality of the device is guaranteed.

** Functionality of the device from 0°C to +70°C is guaranteed by production testing. Performance from –40°C to +85°C is guaranteed by characterization and periodic sampling of production units.*

ELECTRICAL CHARACTERISTICS

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Transmission Performance						
2-wire return loss	200 Hz to 3.4 kHz	26			dB	1, 4
Analog output (VTX) impedance			3	20	Ω	4
Analog (VTX) output offset voltage		–50		+50	mV	
Overload level, 2-wire and 4-wire	Active state	2.5			Vpk	2a
Overload level	On hook, R_{LAC} = 600 Ω	0.77			Vrms	2b
THD, Total Harmonic Distortion	0 dBm +7 dBm		–64 –55	–50 –40	dB	5
THD, On hook	0 dBm, R_{LAC} = 600 Ω			–36	dB	5
Longitudinal Capability (See Test Circuit D)						
Longitudinal to metallic L-T, L-4 balance	200 Hz to 1 kHz 0°C to +70°C –1* 0°C to +70°C –2 –40°C to +85°C –1 –40°C to +85°C –2	 52 63 50 58			dB	 4 4
	1 kHz to 3.4 kHz 0°C to +70°C –1* 0°C to +70°C –2 –40°C to +85°C –1 –40°C to +85°C –2	 52 58 50 53			dB	 4 4
Longitudinal signal generation 4-L	200 Hz to 3.4 kHz	40			dB	
Longitudinal current per pin (A or B)	Active state	20	27	35	mArms	8
Longitudinal impedance at A or B	0 to 100 Hz		25		Ω/pin	
Idle Channel Noise						
C-message weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		7	+10 +12	dBrnc	4
Psophometric weighted noise	R_L = 600 Ω 0°C to +70°C R_L = 600 Ω –40°C to +85°C		–83	–80 –78	dBmp	4
Insertion Loss and Balance Return Signal (See Test Circuits A and B)						
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz	–0.20	0	+0.20	dB	
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz	–6.22	–6.02	–5.82	dB	
Gain accuracy, 4- to 2-wire	On hook	–0.35		+0.35	dB	4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On hook	–6.37	–6.02	–5.67	dB	4
Gain accuracy over frequency	300 to 3.4 kHz relative to 1 kHz	–0.15		+0.15	dB	
Gain tracking	+3 dBm to –55 dBm relative to 0 dBm	–0.15		+0.15	dB	
Gain tracking On hook	0 dBm to –37 dBm +3 dBm to 0 dBm	–0.15 –0.35		+0.15 +0.35	dB	
Group delay	0 dBm, 1 kHz		4		μs	4, 7

Note:
** Performance Grade*

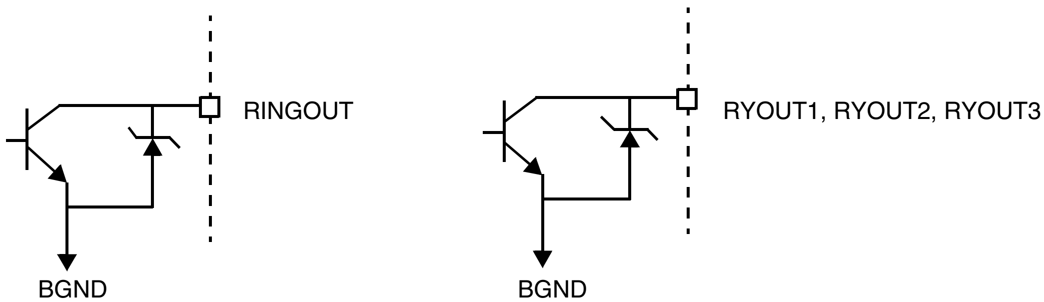
ELECTRICAL CHARACTERISTICS (continued)

Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Line Characteristics						
I_L, Short Loops, Active state	R_{LDC} = 600 Ω	20	23	26		
I_L, Long Loops, Active state	R_{LDC} = 1930 Ω, BAT = –42.75 V, T_A = 25°C	18	19			
I_L, Accuracy, Standby state	$I_L = \frac{\lvert BAT \rvert - 3\ V}{R_L + 400}$ $T_A = 25°C$	$0.7I_L$	I_L	$1.3I_L$	mA	
	Constant-current region	18	30			
I_L, Loop current, Disconnect state	R_L = 0			100	µA	
I_LLIM	Active, A and B to ground		85	120	mA	
VAB, Open Circuit voltage	V_{BAT} = –52 V	–42.75	–44		V	
Power Supply Rejection Ratio (V_{RIPPLE} = 100 mVrms), Active Normal State						
V_{CC}	50 Hz to 3.4 kHz	30	40		dB	5
V_{BAT}	50 Hz to 3.4 kHz	28	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	kΩ	4
Power Dissipation						
On hook, Disconnect state			25	70		
On hook, Standby state			35	100		
On hook, Active state			125	270	mW	
Off hook, Standby state	R_L = 600 Ω		860	1200		
Off hook, Active state	R_L = 300 Ω, R_{TMG} = 2350 Ω		450	800		
Supply Currents, Battery = –48V						
I_{CC}, On-hook V_{CC} supply current	Disconnect state Standby state Active state, BAT = –48 V		1.7 2.2 6.3	4.0 4.0 8.5	mA	
I_{BAT}, On-hook V_{BAT} supply current	Disconnect state Standby state Active state, BAT = –48 V		0.25 0.55 2.8	1.0 1.5 4.8		
RFI Rejection						
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	I_{RSN} = 0 mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C2–C1 and D3–D1)						
V_{IH}, Input High voltage		2.0			V	
V_{IL}, Input Low voltage				0.8		
I_{IH}, Input High current		–75		40	µA	
I_{IL}, Input Low current		–400				
Logic Output ($\overline{DET}$)						
V_{OL}, Output Low voltage	I_{OUT} = 0.3 mA, 15 kΩ to V_{CC}			0.40	V	
V_{OH}, Output High voltage	I_{OUT} = –0.1 mA, 15 kΩ to V_{CC}	2.4				
Ring-Trip Detector Input (DA, DB)						
Bias current		–500	–50		nA	
Offset voltage	Source resistance = 2 MΩ	–50	0	+50	mV	6

ELECTRICAL CHARACTERISTICS (continued)

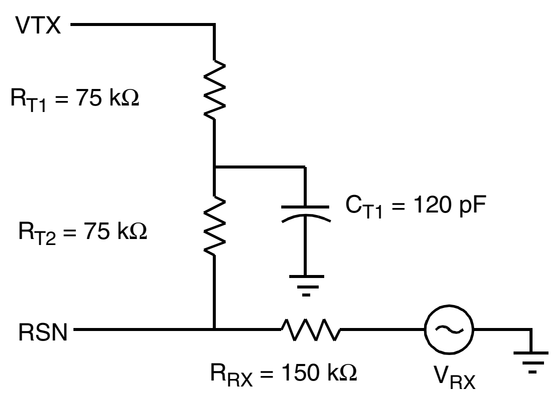
Description	Test Conditions (See Note 1)	Min	Typ	Max	Unit	Note
Loop Detector						
On threshold	R_D = 35.4 kΩ	11.5		17.3	mA	
Off threshold	R_D = 35.4 kΩ	9.4		14.1	mA	
Hysteresis	R_D = 35.4 kΩ	0		4.4	mA	
Relay Driver Output (RINGOUT, RYOUT1, RYOUT2, RYOUT3)						
On voltage	I_{OL} = 40 mA		+0.3	+0.7	V	
Off leakage	V_{OH} = +5 V			100	µA	
Zener breakover	I_Z = 100 µA	6	7.2		V	
Zener On voltage	I_Z = 30 mA		10		V	

RELAY DRIVER SCHEMATICS



Notes:

1. *Unless otherwise noted, test conditions are BAT = –52 V, V_{CC} = +5 V, R_L = 600 Ω, R_{DC1} = R_{DC2} = 27.17 kΩ, R_{TMG} = 2350 Ω, R_D = 35.4 kΩ, no fuse resistors, C_{HP} = 0.22 µF, C_{DC} = 0.1 µF, C_{CAS} = 0.33 µF, D1 = 1N400x, two-wire AC input impedance is a 600 Ω resistance synthesized by the programming network shown below.*



2. *a. Overload level is defined when THD = 1%.*
   b. Overload level is defined when THD = 1.5%.
3. *Balance return signal is the signal generated at V_{TX} by V_{RX}. This specification assumes that the two-wire, AC-load impedance matches the programmed impedance.*
4. *Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.*
5. *This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.*
6. *Tested with 0 Ω source impedance. 2 MΩ is specified for system design only.*
7. *Group delay can be greatly reduced by using a Z_T network such as that shown in Note 1. The network reduces the group delay to less than 2 µs and increases 2WRL. The effect of group delay on linecard performance also may be compensated for by synthesizing complex impedance with the QSLAC™ or DSLAC™ device.*
8. *Minimum current level guaranteed not to cause a false loop detect.*

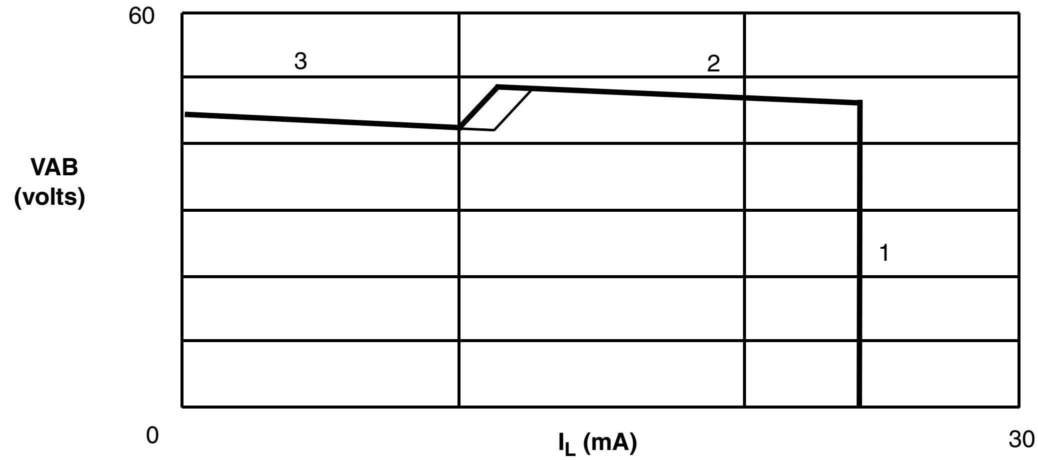
Table 1. SLIC Decoding

State	C2	C1	Two-Wire Status	$\overline{\text{DET}}$ Output
0	0	0	Disconnect	Ring trip
1	0	1	Ringing	Ring trip
2	1	0	Active	Loop detector
3	1	1	Standby	Loop detector

Table 2. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F, and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T, the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \bullet \frac{500Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from VRX to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{1250}{I_{LOOP}}$ $C_{DC} = 1.5\ \text{ms} \bullet \frac{R_{DC1} + R_{DC2}}{R_{DC1} \bullet R_{DC2}}$	R_{DC1}, R_{DC2}, and C_{DC} form the network connected to the R_{DC} pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant-current region.
$RD_{ON} = \frac{510}{I_T}$, $RD_{OFF} = \frac{415}{I_T}$, $C_D = \frac{0.5\ \text{ms}}{R_D}$	R_D and C_D form the network connected from R_D to AGND/DGND and I_T is the threshold current between on hook and off hook.
$C_{CAS} = \frac{1}{3.4 \bullet 10^5 \pi f_c}$	C_{CAS} is the regulator filter capacitor and f_c is the desired filter cut-off frequency.
$I_{STANDBY} = \frac{\lvert V_{BAT}\rvert - 3\ V}{400\ \Omega + R_L}$	Standby loop current (resistive region).
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \left(\frac{\lvert V_{BAT}\rvert - 6\ V}{I_{LOOP}} - 70\ \Omega\right)$	R_{TMG} is connected from TMG to VBAT and saves power within the SLIC in Active and Disconnect state constant-currents only.
$P_{RTMG} = \frac{(\lvert V_{BAT}\rvert - 6\ V - (I_L \bullet R_L))^2}{(R_{TMG} + 70\ \Omega)^2} \bullet R_{TMG}$	Power dissipated in the TMG resistor, R_{TMG}, during Active and Disconnect states.
$P_{SLIC} = \lvert V_{BAT}\rvert \bullet I_L - P_{RTMG} - R_L(I_L)^2 + 0.12\ W$	Power dissipated in the SLIC while in Active and Disconnect states.

DC FEED CHARACTERISTICS



$R_{DC} = R_{DC1} + R_{DC2} = 54.34\ k\Omega$

BAT = –48 V

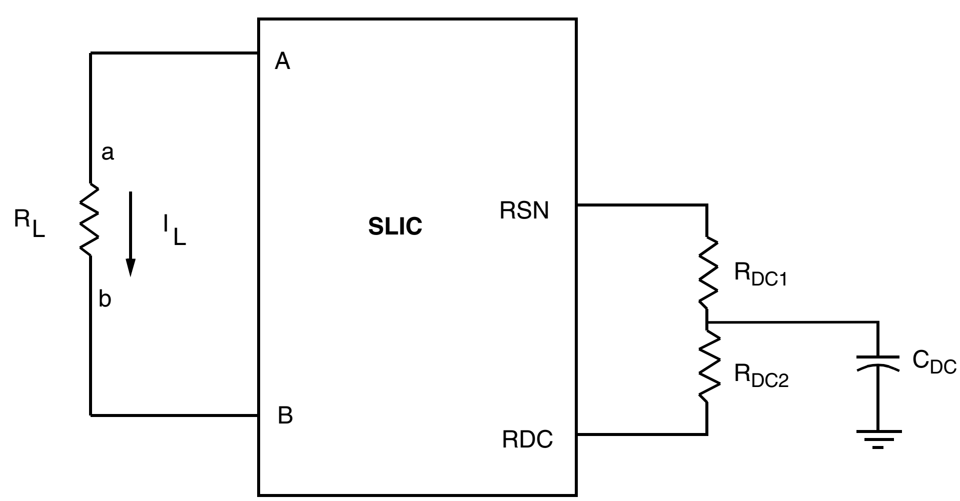
Notes:

1. $V_{AB} = I_L R_L' = \frac{1250}{R_{DC}} R_L'$, where $R_L' = R_L + 2R_F$

2. $V_{AB} = 0.857(|V_{BAT}| + 3.3) - I_L \frac{R_{DC}}{300}$

3. $V_{AB} = 0.857(|V_{BAT}| + 1.2) - I_L \frac{R_{DC}}{300}$

a. Load Line (Typical)

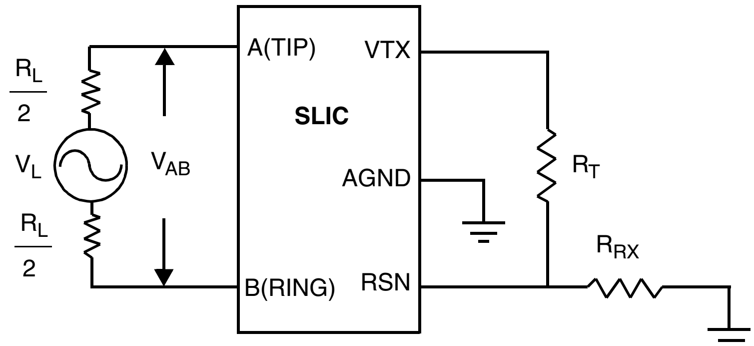


Feed current programmed by R_{DC1} and R_{DC2}

b. Feed Programming

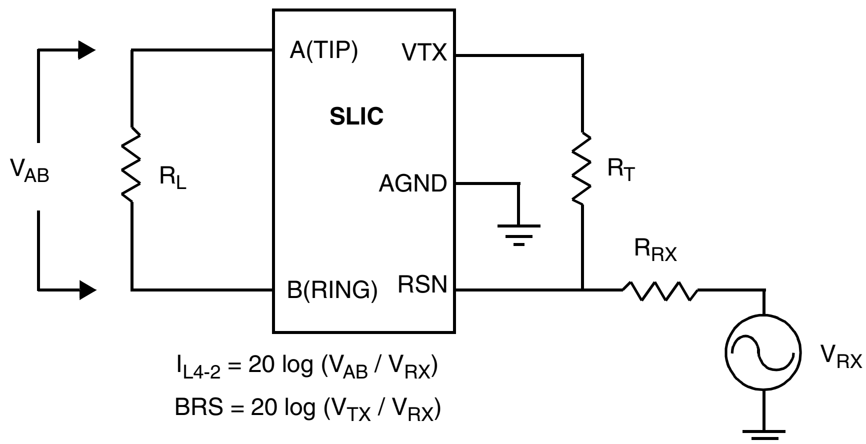
Figure 1. DC Feed Characteristics

TEST CIRCUITS



$I_{L2\text{-}4} = 20 \log (V_{TX} / V_{AB})$

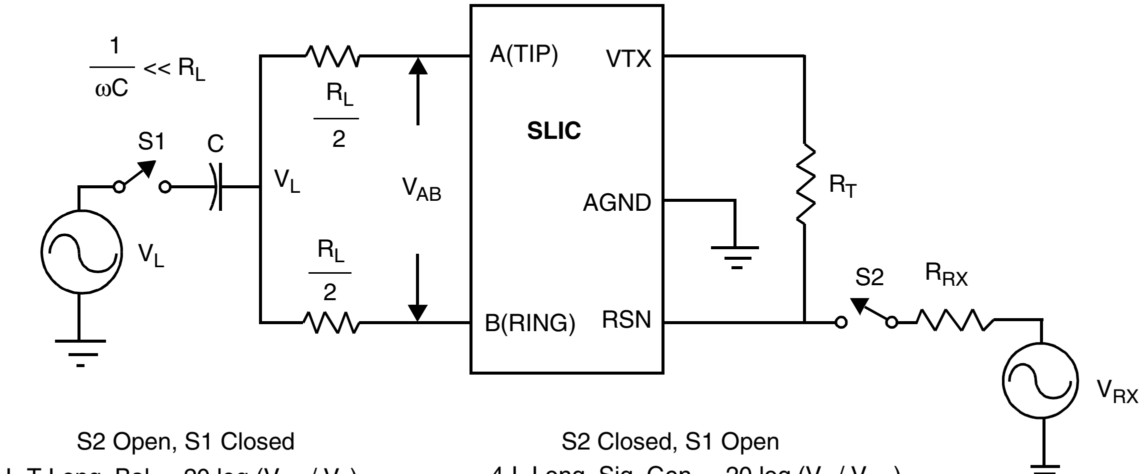
A. Two- to Four-Wire Insertion Loss



$I_{L4\text{-}2} = 20 \log (V_{AB} / V_{RX})$

$BRS = 20 \log (V_{TX} / V_{RX})$

B. Four- to Two-Wire Insertion Loss and Balance Return Signal



S2 Open, S1 Closed

L-T Long. Bal. $= 20 \log (V_{AB} / V_L)$

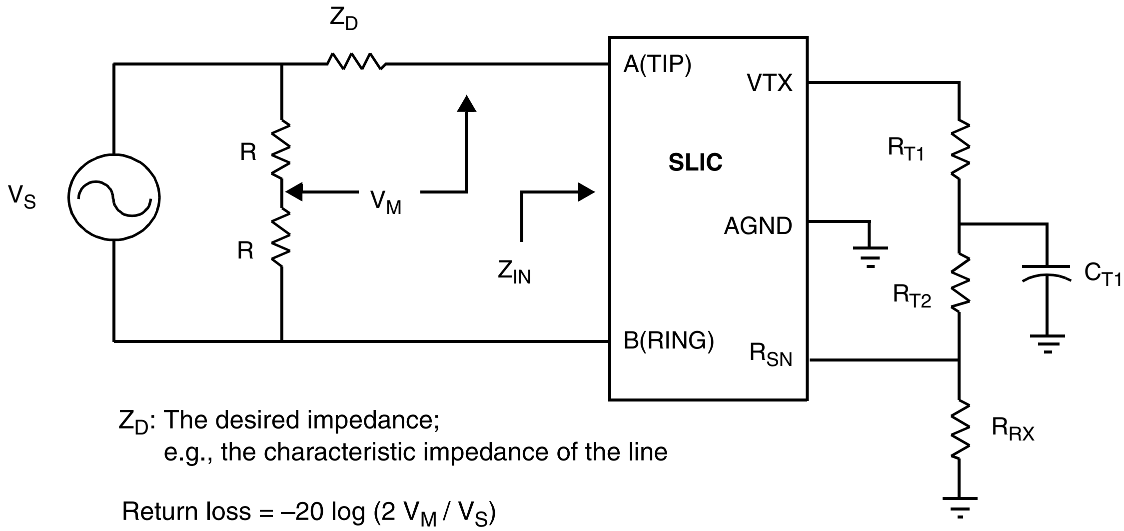
L-4 Long. Bal. $= 20 \log (V_{TX} / V_L)$

S2 Closed, S1 Open

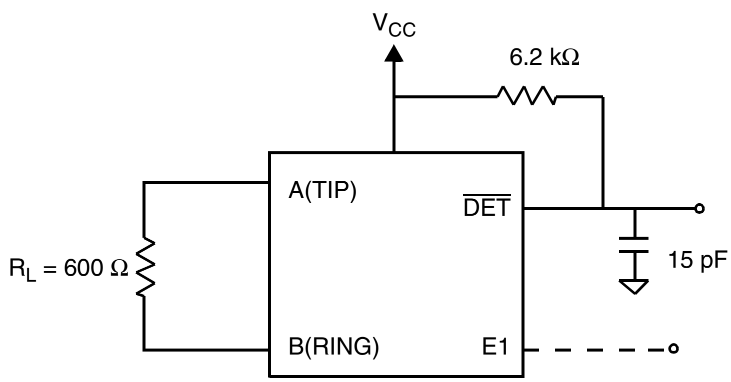
4-L Long. Sig. Gen. $= 20 \log (V_L / V_{RX})$

C. Longitudinal Balance

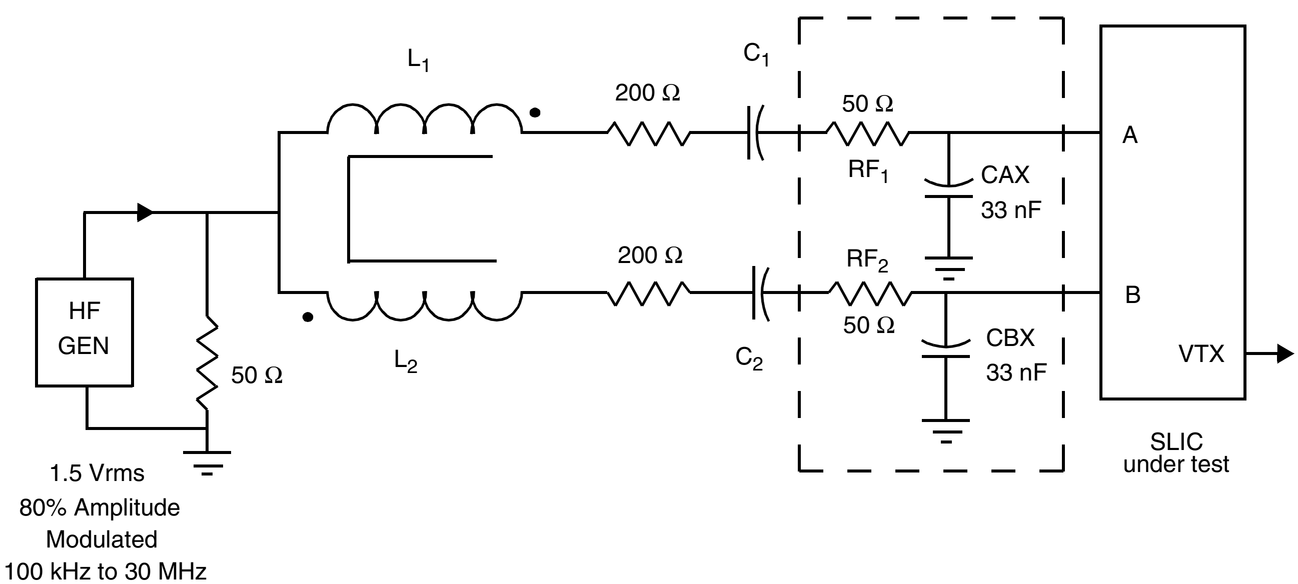
TEST CIRCUITS (continued)



D. Two-Wire Return Loss Test Circuit

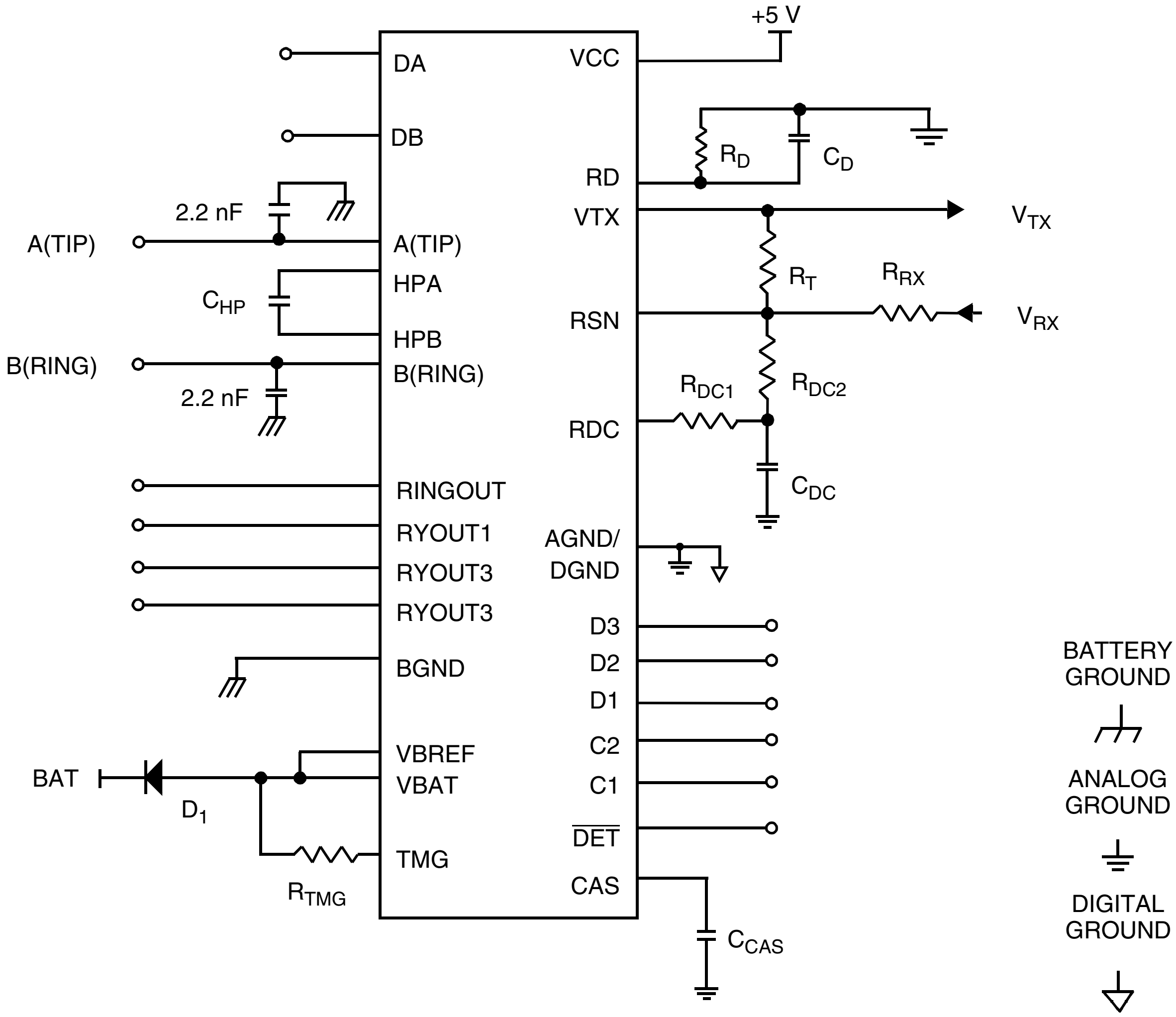


E. Loop-Detector Switching



F. RFI Test Circuit

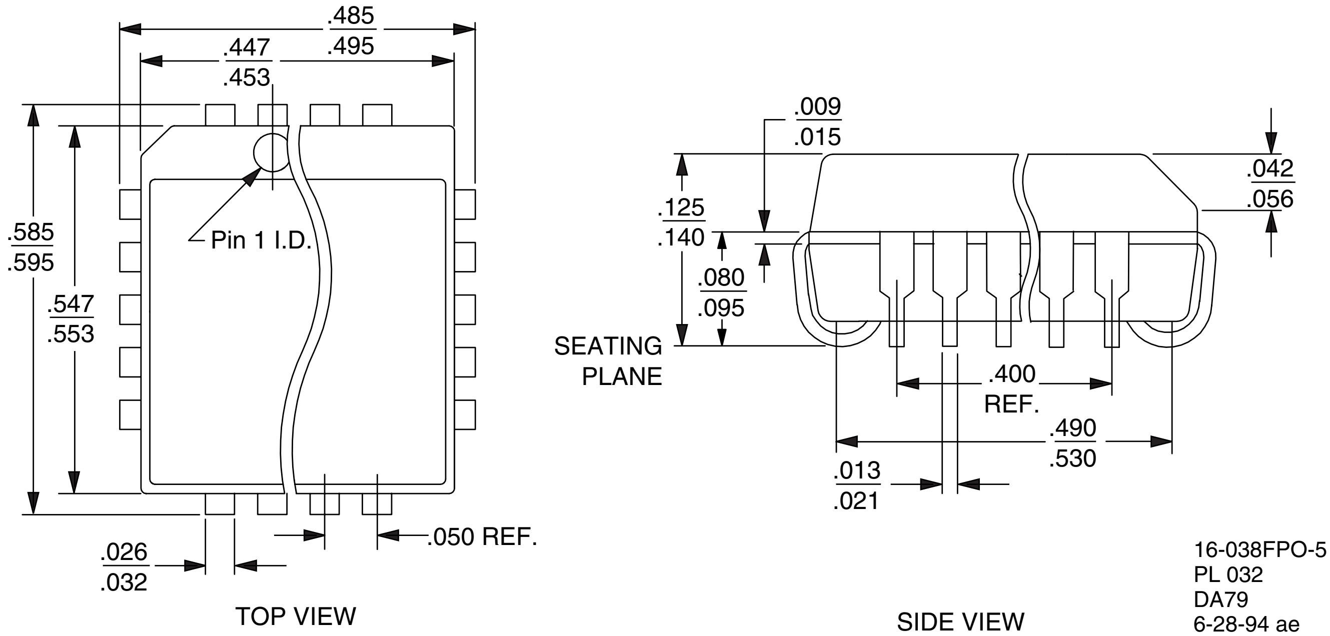
TEST CIRCUITS (continued)



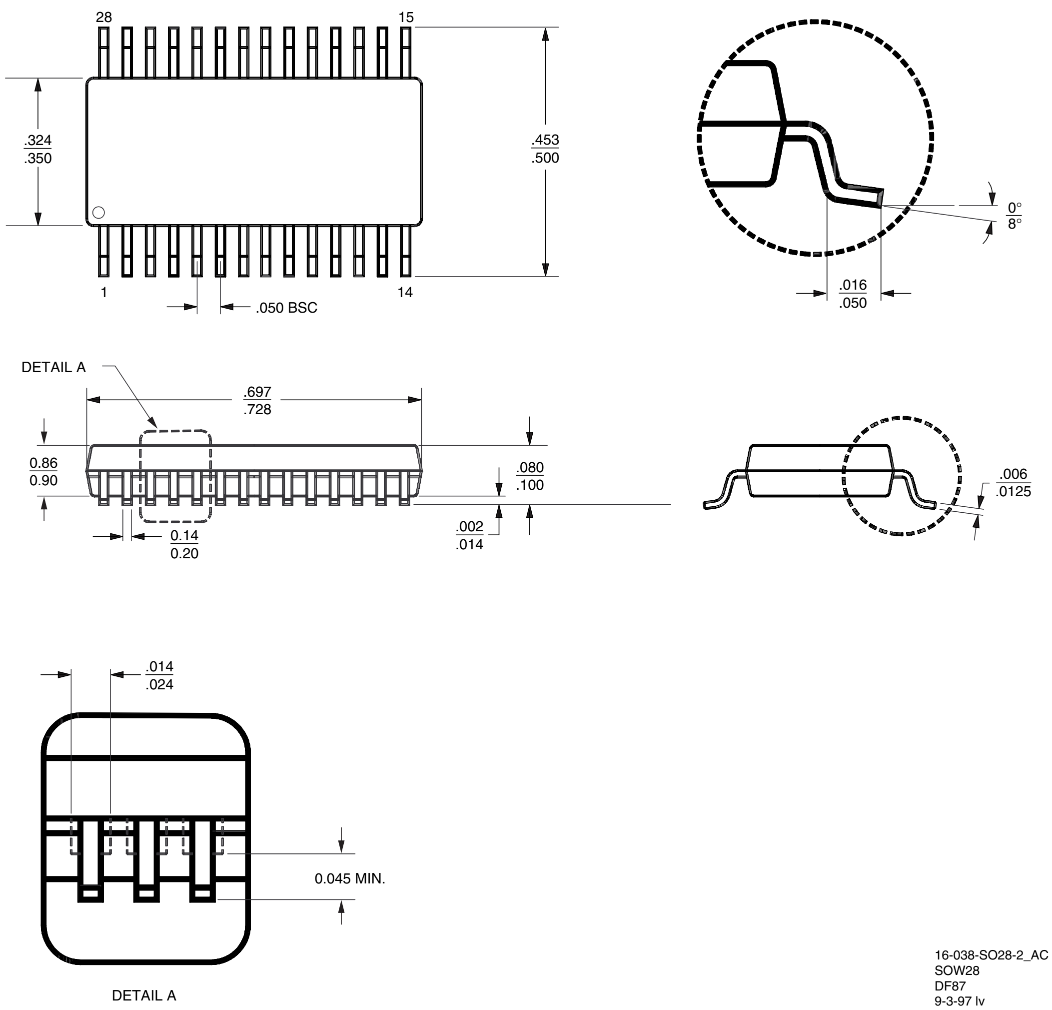
G. Am7920 Test Circuit

PHYSICAL DIMENSIONS

PL032



SOW028



REVISION SUMMARY

Revision C to Revision D

- Minor changes were made to the datasheet style and format to conform to Legerity standards.

Revision D to Revision E

- Absolute Maximum Ratings: Added ESD immunity specification.

Revision E to Revision F

- Added the 28-pin SOIC connection diagram and the SC option to the ordering information.

Revision F to Revision G

- The physical dimension (PL032) was added to the Physical Dimension section.

Revision G to Revision H

- Deleted the plastic DIP package and references to it.
- Updated the Pin Description table to correct inconsistencies.

Notes:

Notes:

Legerity provides silicon solutions that enhance the performance, speeds time-to-market, and lowers the system cost of our customers' products. By combining process, design, systems architecture, and a complete set of software and hardware support tools with unparalleled factory and worldwide field applications support, Legerity ensures its customers enjoy a smoother design experience. It is this commitment to our customers that places Legerity in a class by itself.

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