



## 1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

|                |                            |                             |                                |
|----------------|----------------------------|-----------------------------|--------------------------------|
| 5962-90658     | 01                         | J                           | X                              |
| Drawing number | Device type<br>(see 1.2.1) | Case outline<br>(see 1.2.2) | Lead finish per<br>MIL-M-38510 |

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

| Device type | Generic number | Circuit function   | Access time |
|-------------|----------------|--------------------|-------------|
| 01          | 57C43C-70      | 4K x 8-bit UVEPROM | 70 ns       |
| 02          | 57C43C-55      | 4K x 8-bit UVEPROM | 55 ns       |
| 03          | 57C43C-45      | 4K x 8-bit UVEPROM | 45 ns       |
| 04          | 57C43C-35      | 4K x 8-bit UVEPROM | 35 ns       |

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style                   |
|----------------|------------------------|-----------|---------------------------------|
| J              | GDIP1-T24 or CDIP2-T24 | 24        | Dual-in-line 1/                 |
| K              | GDFP2-F24 or CDFP3-F24 | 24        | Flat pack 1/                    |
| L              | GDIP3-T24 or CDIP4-T24 | 24        | Dual-in-line 1/                 |
| 3              | CQCC1-N28              | 28        | Square leadless chip carrier 1/ |

## 1.3 Absolute maximum ratings.

|                                                                  |                         |
|------------------------------------------------------------------|-------------------------|
| Voltage range on any pin with respect to ground . . . . .        | -0.6 V dc to +7.0 V dc  |
| $V_{DD}$ range with respect to ground . . . . .                  | -0.6 V dc to +14.0 V dc |
| Storage temperature range . . . . .                              | -65°C to +150°C         |
| Maximum power dissipation ( $P_D$ ) . . . . .                    | 1 W                     |
| Lead temperature (soldering, 10 seconds) . . . . .               | +300°C                  |
| Thermal resistance, junction-to-case ( $\theta_{JC}$ ) . . . . . | See MIL-STD-1835        |
| Junction temperature ( $T_J$ ) 2/ . . . . .                      | +150°C                  |
| Temperature (under bias) range . . . . .                         | -55°C to +125°C         |

## 1.4 Recommended operating conditions.

|                                                      |                        |
|------------------------------------------------------|------------------------|
| Supply voltage range ( $V_{CC}$ ) . . . . .          | +4.5 V dc to +5.5 V dc |
| Ground voltage (GND) . . . . .                       | 0 V dc                 |
| Input high voltage ( $V_{IH}$ ) . . . . .            | 2.0 V dc minimum       |
| Input low voltage ( $V_{IL}$ ) . . . . .             | 0.8 V dc maximum       |
| Case operating temperature range ( $T_C$ ) . . . . . | -55°C to +125°C        |

1/ Lid shall be transparent to permit ultraviolet light erasure.

2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

|                                                                                             |           |                |            |
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## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

### STANDARD

#### MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.  
MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-1835 - Microcircuit Case Outlines.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in groups A, B, C, or D (see 4.3), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of cells shall be programmed or at least 25 percent of the total number of cells to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

|                                                                                             |           |                |            |
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TABLE I. Electrical performance characteristics.

| Test                                  | Symbol           | Conditions<br>-55°C ≤ T <sub>C</sub> ≤ +125°C<br>4.5V ≤ V <sub>CC</sub> ≤ 5.5V<br>unless otherwise specified | Group A<br>subgroups | Device<br>types | Limits |                      | Units |
|---------------------------------------|------------------|--------------------------------------------------------------------------------------------------------------|----------------------|-----------------|--------|----------------------|-------|
|                                       |                  |                                                                                                              |                      |                 | Min    | Max                  |       |
| Input load current                    | I <sub>LI</sub>  | V <sub>IN</sub> = 5.5 V and GND                                                                              | 1,2,3                | ALL             | -10    | 10                   | μA    |
| Input leakage current                 | I <sub>IX</sub>  | V <sub>IN</sub> = V <sub>CC</sub> and GND                                                                    | 1,2,3                | ALL             | -10    | 10                   | μA    |
| Output leakage current                | I <sub>OZ</sub>  | V <sub>OUT</sub> = 5.5 V and GND                                                                             | 1,2,3                | ALL             | -10    | 10                   | μA    |
| V <sub>CC</sub> active current (CMOS) | I <sub>CC1</sub> | CMOS inputs:<br>0 ± 0.3 V or V <sub>CC</sub> ± 0.3 V 1/                                                      | 1,2,3                | ALL             |        | 35                   | mA    |
| V <sub>CC</sub> active current (TTL)  | I <sub>CC2</sub> | TTL inputs:<br>V <sub>IL</sub> ≤ 0.8 V, V <sub>IH</sub> ≥ 2.0 V 1/                                           | 1,2,3                | ALL             |        | 50                   | mA    |
| Input high level voltage              | V <sub>IH</sub>  |                                                                                                              | 1,2,3                | ALL             | 2.0    | V <sub>CC</sub> +0.3 | V     |
| Input low level voltage               | V <sub>IL</sub>  |                                                                                                              | 1,2,3                | ALL             | -0.1   | 0.8                  | V     |
| Output high voltage                   | V <sub>OH</sub>  | I <sub>OH</sub> = -4 mA                                                                                      | 1,2,3                | ALL             | 2.4    |                      | V     |
| Output low voltage                    | V <sub>OL</sub>  | I <sub>OL</sub> = 16 mA                                                                                      | 1,2,3                | ALL             |        | 0.4                  | V     |
| Functional tests                      |                  | See 4.3.1d                                                                                                   | 7,8A,8B              | ALL             |        |                      |       |
| Input capacitance                     | C <sub>IN</sub>  | V <sub>IN</sub> = 0 V 2/                                                                                     | 4                    | ALL             |        | 6                    | pF    |
| Output capacitance                    | C <sub>OUT</sub> | V <sub>OUT</sub> = 0 V 2/                                                                                    |                      |                 |        |                      |       |
| Address to output delay               | t <sub>ACC</sub> | See figures 3 and 4                                                                                          | 9,10,11              | 01              |        | 70                   | ns    |
|                                       |                  |                                                                                                              |                      | 02              |        | 55                   |       |
|                                       |                  |                                                                                                              |                      | 03              |        | 45                   |       |
|                                       |                  |                                                                                                              |                      | 04              |        | 35                   |       |
| CS1/V <sub>pp</sub> to output delay   | t <sub>CS</sub>  |                                                                                                              | 9,10,11              | 01-03           |        | 25                   | ns    |
|                                       |                  |                                                                                                              |                      | 04              |        | 20                   |       |
| Output disable to output float        | t <sub>DF</sub>  | 3/ See figures 3 and 4                                                                                       | 9,10,11              | ALL             |        | 25                   | ns    |
| Address to output hold                | t <sub>OH</sub>  | See figures 3 and 4                                                                                          | 9,10,11              | ALL             | 0      |                      | ns    |

1/ Add 3 mA/MHz for ac power component.

2/ Tested initially and after any design or process changes that affect this parameter, and therefore shall be guaranteed to the limits specified in table I.

3/ May not be tested, but shall be guaranteed to the limits specified in table I.

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| Device types    | All                                          |                                              |
|-----------------|----------------------------------------------|----------------------------------------------|
| Case outlines   | J, K, and L                                  | 3                                            |
| Terminal number | Terminal symbol                              |                                              |
| 1               | A <sub>7</sub>                               | NC                                           |
| 2               | A <sub>6</sub>                               | A <sub>7</sub>                               |
| 3               | A <sub>5</sub>                               | A <sub>6</sub>                               |
| 4               | A <sub>4</sub>                               | A <sub>5</sub>                               |
| 5               | A <sub>3</sub>                               | A <sub>4</sub>                               |
| 6               | A <sub>2</sub>                               | A <sub>3</sub>                               |
| 7               | A <sub>1</sub>                               | A <sub>2</sub>                               |
| 8               | A <sub>0</sub>                               | A <sub>1</sub>                               |
| 9               | O <sub>0</sub>                               | A <sub>0</sub>                               |
| 10              | O <sub>1</sub>                               | NC                                           |
| 11              | O <sub>2</sub>                               | O <sub>0</sub>                               |
| 12              | GND                                          | O <sub>1</sub>                               |
| 13              | O <sub>3</sub>                               | O <sub>2</sub>                               |
| 14              | O <sub>4</sub>                               | GND                                          |
| 15              | O <sub>5</sub>                               | NC                                           |
| 16              | O <sub>6</sub>                               | O <sub>3</sub>                               |
| 17              | O <sub>7</sub>                               | O <sub>4</sub>                               |
| 18              | CS2                                          | O <sub>5</sub>                               |
| 19              | A <sub>11</sub>                              | O <sub>6</sub>                               |
| 20              | $\overline{\text{CS1}}/\text{V}_{\text{PP}}$ | O <sub>7</sub>                               |
| 21              | A <sub>10</sub>                              | NC                                           |
| 22              | A <sub>9</sub>                               | CS2                                          |
| 23              | A <sub>8</sub>                               | A <sub>11</sub>                              |
| 24              | V <sub>CC</sub>                              | $\overline{\text{CS1}}/\text{V}_{\text{PP}}$ |
| 25              | ---                                          | A <sub>10</sub>                              |
| 26              | ---                                          | A <sub>9</sub>                               |
| 27              | ---                                          | A <sub>8</sub>                               |
| 28              | ---                                          | V <sub>CC</sub>                              |

FIGURE 1. Terminal connections.

|                                                                                                       |                   |                       |                    |
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| Mode           | V <sub>CC</sub> | $\overline{CS1}/V_{PP}$ | CS2                 | O <sub>0</sub> -O <sub>7</sub> |
|----------------|-----------------|-------------------------|---------------------|--------------------------------|
| Read           | 5.0 V $\pm$ 10% | V <sub>IL</sub>         | V <sub>IH</sub>     | D <sub>OUT</sub>               |
| Output disable | 5.0 V $\pm$ 10% | V <sub>IH</sub>         | X $\underline{1}$ / | High Z                         |
| Output disable | 5.0 V $\pm$ 10% | X $\underline{1}$ /     | V <sub>IL</sub>     | High Z                         |
| Program        | V <sub>CC</sub> | V <sub>PP</sub>         | X $\underline{1}$ / | D <sub>IN</sub>                |
| Program verify | V <sub>CC</sub> | V <sub>IL</sub>         | V <sub>IH</sub>     | D <sub>OUT</sub>               |

$\underline{1}$ / X can be V<sub>IL</sub> or V<sub>IH</sub>.

FIGURE 2. Truth table.

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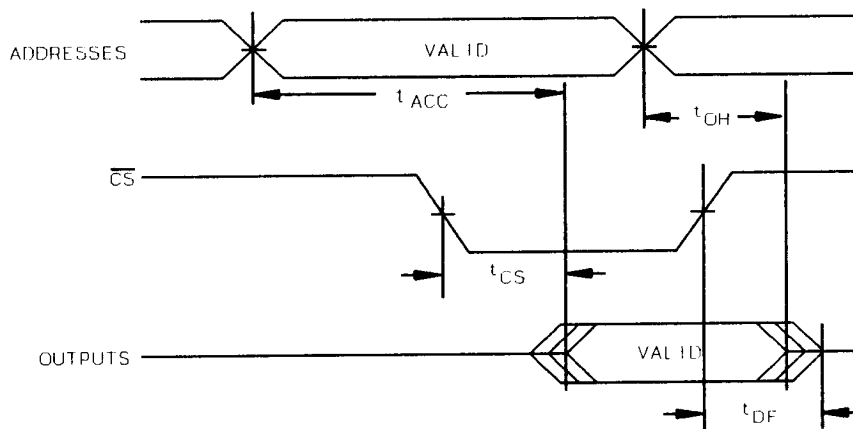
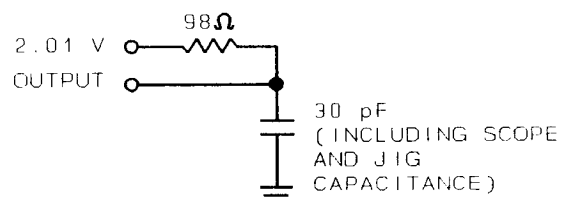


FIGURE 3. AC read timing diagram.

|                                                                                             |           |                |            |
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Test conditions (ac):

Input pulse levels: GND to 3.0 V  
 Input rise and fall times:  $\leq 5$  ns  
 Input timing reference levels: 1.5 V  
 Output reference levels: 1.5 V

FIGURE 4. Test load circuit.

|                                                                                                       |                   |                       |                    |
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3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.6.1 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4 herein.

3.6.2 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 herein.

3.6.3 Verification of erasure of programmed EPROMS. When specified, devices shall be verified as either programmed to specified program or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.9 Notification of change. Notification of change to DESC-EC of change of product (see 6.3 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.10 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.11 Endurance. A reprogrammability test shall be completed as part of the vendor's reliability monitors. This reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

- a. All devices selected for testing shall be programmed in accordance with 3.2.3.2 herein.
- b. Verify pattern (see 3.6.3).
- c. Erase (see 3.6.1).
- d. Verify pattern erasure (see 3.6.3).

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

|                                                                                             |           |                |            |
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TABLE II. Electrical test requirements.

| MIL-STD-883 test requirements                                                  | Subgroups<br>(per method<br>5005, table 1) |
|--------------------------------------------------------------------------------|--------------------------------------------|
| Interim electrical parameters<br>(method 5004)                                 | 1                                          |
| Final electrical test parameters for<br>for unprogrammed devices (method 5004) | 1*,2,3,7*,8A,8B,<br>9,10,11                |
| Final electrical test parameters for<br>programmed devices (method 5004)       | 1,2,3,7*,8A,8B,<br>9,10,11                 |
| Group A test requirements<br>(method 5005)                                     | 1,2,3,4**,7***,<br>8***,9,10,11            |
| Groups C and D end-point<br>electrical parameters (method 5005)                | 2,3,7,8A,8B                                |

\* PDA applies to subgroups 1 and 7.

\*\* See 4.3.1e.

\*\*\* See 4.3.1d.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D using the circuit submitted with the certificate of compliance (see 3.7 herein).

(2)  $T_A = +125^\circ\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

c. A data retention stress shall be included as part of the screening procedure and shall consist of the following steps:

Margin test method. 4/

- (1) At  $+25^\circ\text{C}$ , program greater than 95 percent of the bit locations, including the slowest programming cell. The remaining bits shall provide a worst case speed pattern.
- (2) Bake, unbiased, for 72 hours at  $+140^\circ\text{C}$  or for 32 hours at  $+150^\circ\text{C}$  or for 8 hours at  $+200^\circ\text{C}$ .
- (3) At  $+25^\circ\text{C}$ , perform a margin test using  $V_m = +5.8\text{ V}$  to loose timing (i.e.,  $t_{ACC} = 1\text{ }\mu\text{s}$ ).
- (4) Perform dynamic burn-in accordance with 4.2a.
- (5) At  $+25^\circ\text{C}$ , perform a margin test using  $V_m = +5.8\text{ V}$ .
- (6) Perform electrical test in accordance with 4.2b.
- (7) Erase in accordance with 3.6.1. Devices may be submitted to quality conformance inspection.
- (8) Verify erasure in accordance with 3.6.3.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4/ Steps 1 through 3 may be performed at the wafer level.

|                                                                                                       |                   |                       |                     |
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#### 4.3.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
- c. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified except devices being submitted to groups B, C, and D testing.
- d. As a minimum, subgroups 7 and 8 shall consist of verifying the EPROM pattern specified.
- e. Subgroup 4 ( $C_{IN}$  and  $C_{OUT}$  measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is 15 devices with no failures, and all input and output terminals tested.

#### 4.3.2 Groups C and D inspections.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Steady-state life test conditions, method 1005 of MIL-STD-883.
  - (1) Test condition D using the circuit submitted with the certificate of compliance (see 3.7 herein).
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
  - (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- c. All devices submitted for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

4.4 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms ( $\text{\AA}$ ). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of  $25 \text{ Ws/cm}^2$ . The erasure time with this dosage is approximately 35 minutes using an ultraviolet lamp with a  $12,000 \text{ }\mu\text{W/cm}^2$  power rating. The device should be placed within 1 inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is  $7258 \text{ Ws/cm}^2$  (1 week at  $12,000 \text{ }\mu\text{W/cm}^2$ ). Exposure of the device to high intensity UV light for long periods may cause permanent damage.

4.5 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

|                                                                                             |           |                |             |
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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6021.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.7 herein) has been submitted to and accepted by DESC-ECS.

|                                                                                             |           |                |             |
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