SILICON LABORATORIES

Si5540

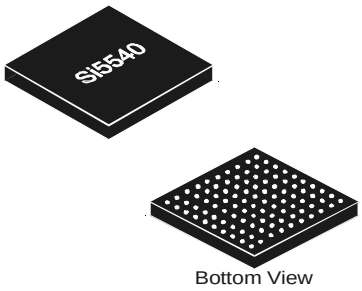
PRELIMINARY DATA SHEET

SiPHY™ OC-192/STM-64 TRANSMITTER

Features

Complete SONET/SDH transmitter for OC-192/STM-64 data rates with integrated 16:1 multiplexer and DSPLL™ based clock multiplier unit:

- Data Rates Supported: OC-192/STM-64, 10GbE, and 10.7 Gbps FEC
- Low Power Operation 0.6 W (typ)
- Small Footprint: 99-Pin BGA Package (11 x 11 mm)
- DSPLL™ Based Clock Multiplier Unit w/ selectable loop filter bandwidths
- OIF SFI-4 Compliant Interface
- Output Clock Powerdown
- Operates with 155 or 622 MHz Reference Sources
- Optional 3.3 V Supply Pin for LVTTL Compatible Outputs
- Single 1.8 V Supply Operation



Bottom View

Ordering Information:

See page 17.

Applications

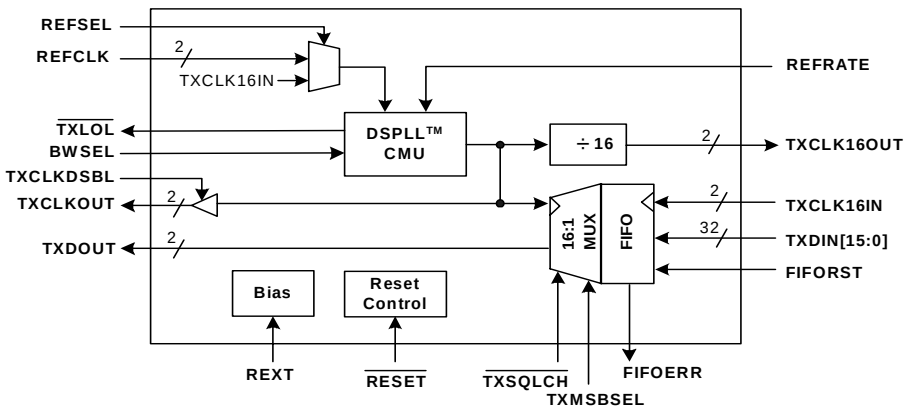
- Sonet/SDH/ATM Routers
- Add/Drop Multiplexers
- Digital Cross Connects
- Optical Transceiver Modules
- Sonet/SDH Test Equipment

Description

The Si5540 is a fully integrated low-power transmitter for high-speed serial communication systems. It combines high speed clock generation with a 16:1 multiplexer to serialize data for OC-192/STM-64 applications. The Si5540 is based on Silicon Laboratories' DSPLL™ technology which eliminates the external loop filter components required by traditional clock multiplier units. In addition, selectable loop filter bandwidths are provided to ensure superior jitter performance while relaxing the jitter requirements on external clock distribution subsystems. Support for data streams up to 10.7 Gbps is also provided for applications that employ forward error correction (FEC).

The Si5540 represents a new standard in low jitter, low power and small size for 10 Gbps serial transmitters. It operates from a single 1.8 V supply over the industrial temperature range (–40°C to 85°C).

Functional Block Diagram



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SILICON LABORATORIES

Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min*	Typ	Max*	Unit
Ambient Temperature	T_A		–40	25	85	°C
LVTTL Output Supply Voltage	V_{DD33}		1.71	—	3.47	V
Si5540 Supply Voltage	V_{DD}		1.71	1.8	1.89	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25°C unless otherwise stated.

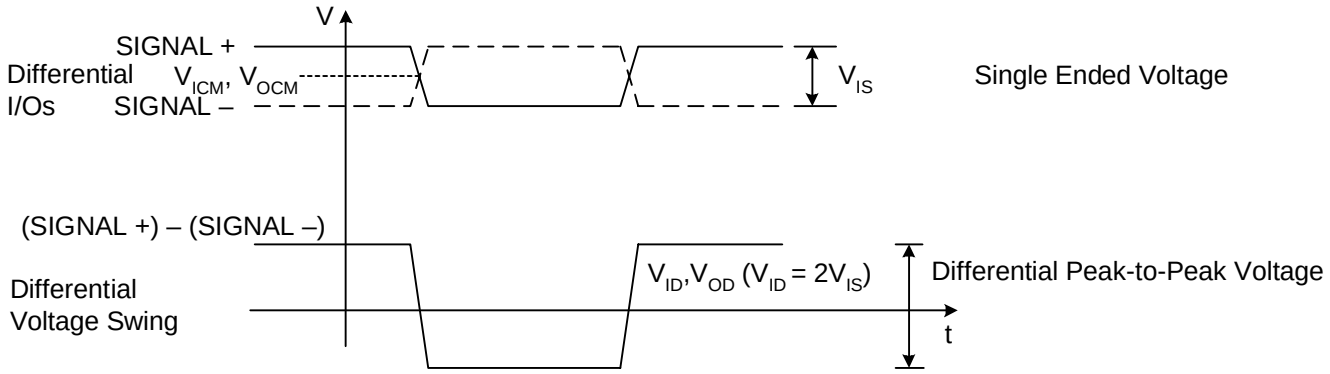


Figure 1. Differential Voltage Measurement (TXDIN, TXDOUT, TXCLK16IN, TXCLK16OUT)

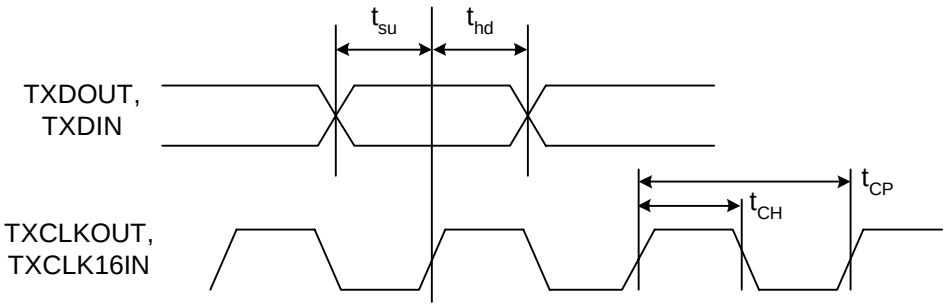


Figure 2. Data to Clock Delay

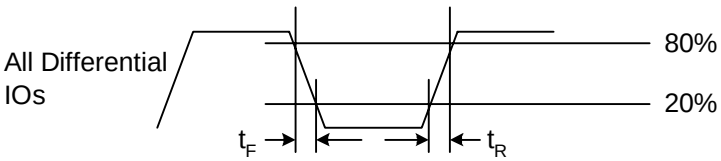


Figure 3. Rise/Fall Time Measurement

Table 2. DC Characteristics, V_{DD} = 1.8 V

(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	333	TBD	mA
Power Dissipation	P_D		—	0.6	TBD	W
Common Mode Output Voltage (TXDOUT,TXCLKOUT)	V_{OCM}		.8	0.9	1.0	V
Differential Output Voltage Swing (TXDOUT,TXCLKOUT), Differential pk-pk	V_{OD}	See Figure 1	800	1000	1200	mV (pk-pk)
LVPECL Input Voltage High (REFCLK)	V_{IH}		1.975	2.3	2.59	V
LVPECL Input Voltage Low (REFCLK)	V_{IL}		1.32	1.6	1.99	V
LVPECL Input Voltage Swing (REFCLK), Differential pk-pk	V_{ID}		250	—	2600	mV (pk-pk)
LVPECL Input Common Mode (REFCLK)	V_{ICM}		1.65	1.95	2.30	V
Input Impedance (REFCLK, TXDIN, TXCLK16IN)	R_{IN}	Each input to common mode	42	50	58	Ω
LVDS Input High Voltage (TXDIN, TXCLK16IN)	V_{IH}		—	—	2.4	V
LVDS Input Low Voltage (TXDIN, TXCLK16IN)	V_{IL}		0.0	—	—	V
LVDS Input Voltage, Single Ended pk-pk (TXDIN, TXCLK16IN)	V_{ISE}		100	—	600	mV (pk-pk)
LVDS Input Common Mode Voltage (TXDIN, TXCLK16IN)	V_{ICM}		.8	2.0	2.4	V
LVDS Output High Voltage (TXCLK16OUT)	V_{OH}	100 Ω Load Line-to-Line	TBD	—	1.475	V
LVDS Output Low Voltage (TXCLK16OUT)	V_{OL}	100 Ω Load Line-to-Line	0.925	—	TBD	V
LVDS Output Voltage, Single Ended pk-pk (TXCLK16OUT)	V_{OSE}	100 Ω Load Line-to-Line, See Figure 1	250	400	550	mV (pk-pk)
LVDS Output Common Mode Voltage (TXCLK16OUT)	V_{OCM}		1.125	1.20	1.275	V
Output Short to GND (TXCLK16OUT, TXDOUT, TXCLKOUT)	I_{SC-}		—	25	TBD	mA
Output Short to V_{DD} (TXCLK16OUT, TXDOUT, TXCLKOUT)	I_{SC+}		TBD	–100	—	µA
LVTTL Input Voltage Low (TXCLKDSBL, FIFORST, $\overline{\text{TXSQLCH}}$, BWSEL, REFRATE, REFSEL, TXMSBSEL, $\overline{\text{RESET}}$)	V_{IL2}		—	—	0.8	V

Table 2. DC Characteristics, V_{DD} = 1.8 V (Continued)

(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage High (TXCLKDSBL, FIFORST, $\overline{\text{TXSQLCH}}$, BWSEL, REFRATE, REFSEL, TXMSBSEL, $\overline{\text{RESET}}$)	V_{IH2}		2.0	—	—	V
Input Low Current (TXCLKDSBL, FIFORST, $\overline{\text{TXSQLCH}}$, BWSEL, REFRATE, REFSEL, TXMSBSEL, $\overline{\text{RESET}}$)	I_{IL}		—	—	10	µA
Input High Current (TXCLKDSBL, FIFORST, $\overline{\text{TXSQLCH}}$, BWSEL, REFRATE, REFSEL, TXMSBSEL, $\overline{\text{RESET}}$)	I_{IH}		—	—	10	µA
Input Impedance (TXCLKDSBL, FIFORST, $\overline{\text{TXSQLCH}}$, BWSEL, REFRATE, REFSEL, TXMSBSEL, $\overline{\text{RESET}}$)	R_{IN}		10	—	—	kΩ
LVTTL Output Voltage Low (FIFOERR, $\overline{\text{TXLOL}}$)	V_{OL2}	VDD33 = 1.8 V	—	—	0.4	V
		VDD33 = 3.3 V	—	—	0.4	
LVTTL Output Voltage High (FIFOERR, $\overline{\text{TXLOL}}$)	V_{OH2}	VDD33 = 1.8 V	1.4	—	—	V
		VDD33 = 3.3 V	2.4	—	—	

Table 3. AC Characteristics (TXCLK16OUT, TXCLK16IN, TXCLKOUT, TXDIN, TXDOUT)
(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
TXCLKOUT Frequency	f_{clkout}		—	9.95	10.7	GHz
TXCLKOUT Duty Cycle		tch/tcp, Figure 2	45	—	55	%
Output Rise Time (TXCLKOUT, TXDOUT)	t_R	Figure 3	—	25	—	ps
Output Fall Time (TXCLKOUT, TXDOUT)	t_F	Figure 3	—	25	—	ps
TXCLKOUT Setup to TXDOUT	t_{su}	Figure 2	25	—	—	ps
TXCLKOUT Hold From TXDOUT	t_{hd}	Figure 2	25	—	—	ps
Output Return Loss		400 kHz–10 GHz 10 GHz–16 GHz	TBD TBD	— —	— —	dB dB
TXCLK16OUT Frequency	f_{CLKIN}	Figure 2	—	622	667	MHz
TXCLK16OUT Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK16OUT Rise & Fall Times	t_R, t_F		100	—	300	ps
TXDIN Setup to TXCLK16IN	t_{DSIN}		—	—	300	ps
TXDIN Hold from TXCLK16IN	t_{DHIN}		—	—	300	ps
TXCLK16IN Frequency	f_{CLKIN}		—	622	667	MHz
TXCLK16IN Duty Cycle		tch/tcp, Figure 2	40	—	60	%
TXCLK16IN Rise & Fall Times	t_R, t_F		100	—	300	ps

Table 4. AC Characteristics (Clock Multiplier Characteristics)
(V_{DD} = 1.8 V ±5%, T_A = –40°C to 85°C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Jitter Generation—Deterministic	$J_{DET(PP)}$	PRBS-23	—	0.020	TBD	UI_{PP}
Jitter Generation—Random	$J_{GEN(RMS)}$		—	0.005	TBD	UI_{RMS}
Jitter Transfer Bandwidth	J_{BW}	BWSEL = 0	—	—	12	kHz
		BWSEL = 1	—	—	50	kHz
Jitter Transfer Peaking			—	0.05	0.1	dB
Acquisition Time	T_{AQ}	Valid REFCLK	—	15	20	ms
Input Reference Clock Frequency	RC_{FREQ}	REFRATE = 1	—	622	667	MHz
		REFRATE = 0	—	155	167	MHz
Input Reference Clock Duty Cycle	RC_{DUTY}		40	—	60	%
Input Reference Clock Frequency Tolerance	RC_{TOL}		–100	—	100	ppm
Note: Bellcore specifications: GR-1377-CORE, Issue 5, December 1998.						

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.0	V
LVTTL Input Voltage	V_{DD33}	–0.5 to 3.6	V
Differential Input Voltages	V_{DIF}	–0.3 to (V_{DD}+ 0.3)	V
Maximum Current any output PIN		±50	mA
Operating Junction Temperature	T_{JCT}	–55 to 150	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C
Package Temperature (soldering 10 seconds)		275	°C
ESD HBM Tolerance (100 pf, 1.5 kΩ)		TBD	V

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance Junction to Ambient	φ_{JA}	Still Air	35	°C/W

Functional Description

The Si5540 is a fully integrated, low power, SONET/SDH transmitter for OC-192/STM-64 applications. It combines a high performance clock multiplier unit (CMU) with a 16:1 serializer that has a low-speed interface compliant with the Optical Interface Forum (OIF) SFI-4 standard.

The CMU uses a phase-locked loop (PLL) architecture based on Silicon Laboratories' proprietary DSPLL™ technology. This technology is used to generate ultra-low jitter clock and data outputs that provide significant margin to the SONET/SDH specifications. The DSPLL architecture also utilizes a digitally implemented loop filter that eliminates the need for external loop filter components. As a result, sensitive noise coupling nodes that typically cause degraded jitter performance in crowded PCB environments are removed.

The DSPLL also reduces the complexity and performance requirements of reference clock distribution strategies for OC-192/STM-64 optical port cards. This is possible because the DSPLL provides selectable wideband and narrowband loop filter settings that allow the user to set the jitter attenuation characteristics of the CMU to accommodate reference clock sources that have a high jitter content. Unlike traditional analog PLL implementations, the loop filter bandwidth is controlled by a digital filter inside the DSPLL and can be changed without any modification to external components.

DSPLL™ Clock Multiplier Unit

The Si5540's clock multiplier unit (CMU) uses Silicon Laboratories' proprietary DSPLL technology to generate a low jitter, high frequency clock source capable of producing a high speed serial clock and data output with significant margin to the SONET/SDH specifications. This is achieved by using a digital signal processing (DSP) algorithm to replace the loop filter commonly found in analog PLL designs. This algorithm processes the phase detector error term and generates a digital control value to adjust the frequency of the voltage controlled oscillator (VCO). Because external loop filter components are not required, sensitive noise entry points are eliminated, thus making the DSPLL less susceptible to board-level noise sources. Therefore, SONET/SDH jitter compliance is easier to attain in the application.

Programmable Loop Filter Bandwidth

The digital loop filter in the Si5530 provides two bandwidth settings that support either wideband or narrowband jitter transfer characteristics. The filter bandwidth is selected via the BWSEL control input. In traditional PLL implementations, changing the loop filter bandwidth would require changing the values of external loop filter components.

In narrowband mode, a loop filter cutoff of 12 kHz is provided. This setting makes the Si5540 more tolerant of jitter on the reference clock source. As a result, the complexity of the clock distribution circuitry used to generate the physical layer reference clocks can be simplified without compromising jitter margin to the SONET/SDH specification.

In wideband mode, the loop filter provides a cutoff of 50 kHz. This setting is desirable in applications where the reference clock is provided by a low jitter source like the Si5364 Clock Synchronization IC or Si5320 Precision Clock Multiplier/Jitter Attenuator IC. This allows the DSPLL to more closely track the precision reference source resulting in the best possible jitter performance.

Reference Clock

The CMU within the Si5530 is designed to operate with reference clock sources that are either 1/16th or 1/64th the desired output data rate. The CMU will support operation with data rates between 9.9 Gbps and 10.7 Gbps and the reference clock should be scaled accordingly. For example, to support 10.66 Gbps operation the reference clock source would be approximately 167 MHz or 666 MHz. The REFRATE input pin is used to configure the device for operation with one of the two supported reference clock submultiples of the data rate.

The Si5540 supports operation with two selectable reference clock sources. The first configuration uses an externally provided reference clock that is input via REFCLK. The second configuration uses the parallel data clock, TXCLK16IN, as the reference clock source. When using TXCLK16IN as the reference source, the narrowband loop filter setting may be preferable to remove jitter that may be present on the data clock. The selection of reference clock configuration is controlled via the REFSEL input. The Si5540 will drive the $\overline{\text{TXLOL}}$ output high to indicate the DSPLL has locked to the selected reference source.

Serialization

The Si5540 includes serialization circuitry that combines a FIFO with a parallel to serial shift register. Low speed data on the parallel input bus, TXDIN[15:0], is latched into the FIFO on the rising edge of TXCLK16IN. The data in the FIFO is clocked into the

shift register by an output clock, TXCLK16OUT, that is produced by dividing down the high speed transmit clock, TXCLKOUT, by a factor of 16. The TXCLK16OUT clock output is provided to support 16 bit word transfers between the Si5540 and upstream devices using a counter clocking scheme. The high-speed serial data stream is clocked out of the shift register using TXCLKOUT.

Input FIFO

The Si5540 integrates a FIFO to decouple data transferred into the FIFO via TXCLK16IN from data transferred into the shift register via TXCLK16OUT. The FIFO is eight parallel words deep and accommodates any static phase delay that may be introduced between TXCLK16OUT and TXCLK16IN in counter clocking schemes. Further, the FIFO will accommodate a phase drift or wander between TXCLK16IN and TXCLK16OUT of up to three parallel data words.

The FIFO circuitry indicates an overflow or underflow condition by asserting FIFOERR high. This output can be used to recenter the FIFO read/write pointers by tieing it directly to the FIFORST input. The Si5540 will also recenter the read/write pointers after the device's power on reset, external reset via $\overline{\text{RESET}}$, and each time the DSPLL transitions from an out of lock state to a locked state ($\overline{\text{TXLOL}}$ transitions from low to high).

Parallel Input To Serial Output Relationship

The Si5540 provides the capability to select the order in which data on the parallel input bus is transmitted serially. Data on this bus can be transmitted MSB first or LSB first depending on the setting of TXMSBSEL. If TXMSBSEL is tied low, TXDIN0 is transmitted first followed in order by TXDIN1 through TXDIN15. If TXMSBSEL is tied high, TXDIN15 is transmitted first followed in order by TXDIN14 through TXDIN0. This feature simplifies board routing when ICs are mounted on both sides of the PCB.

Transmit Data Squelch

To prevent the transmission of corrupted data into the network, the Si5540 provides a control pin that can be used to force the high speed data output, TXDOUT, to 0. By driving $\overline{\text{TXSQLCH}}$ low TXDOUT will be forced to 0.

Reset

A device reset can be forced by holding the $\overline{\text{RESET}}$ pin low for at least 1 µs. When $\overline{\text{RESET}}$ is asserted low, the input FIFO pointers reset and the digital control circuitry initializes. When RESET transitions high to start normal operation, the DSPLL will be calibrated.

Clock Disable

The Si5540 provides a clock disable pin, TXCLKDSBL, that is used to disable the high-speed serial data clock output, TXCLKOUT. When the TXCLKDSBL pin is asserted, the positive and negative terminals of CLKOUT are tied to 1.5 V through 50 Ω on-chip resistors. This feature is used to reduce power consumption in applications that do not use the high speed transmit data clock.

Bias Generation Circuitry

The Si5540 makes use of an external resistor to set internal bias currents. The external resistor allows precise generation of bias currents which significantly reduces power consumption versus traditional implementations that use an internal resistor. The bias generation circuitry requires a 3.09 kΩ (1%) resistor connected between REXT and GND.

Differential Output Circuitry

The Si5540 utilizes a current-mode logic (CML) architecture to drive the high speed serial output clock and data on TXCLKOUT and TXDOUT. An example of output termination with ac coupling is shown in Figure 4. In applications where direct dc coupling is possible, the 250 nF capacitors may be omitted. The differential peak-to-peak voltage swing of the CML architecture is listed in Table 2 on page 5.

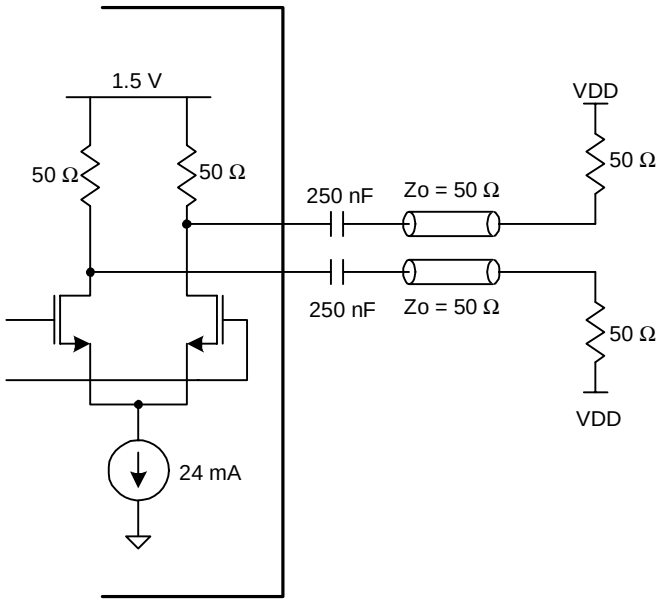
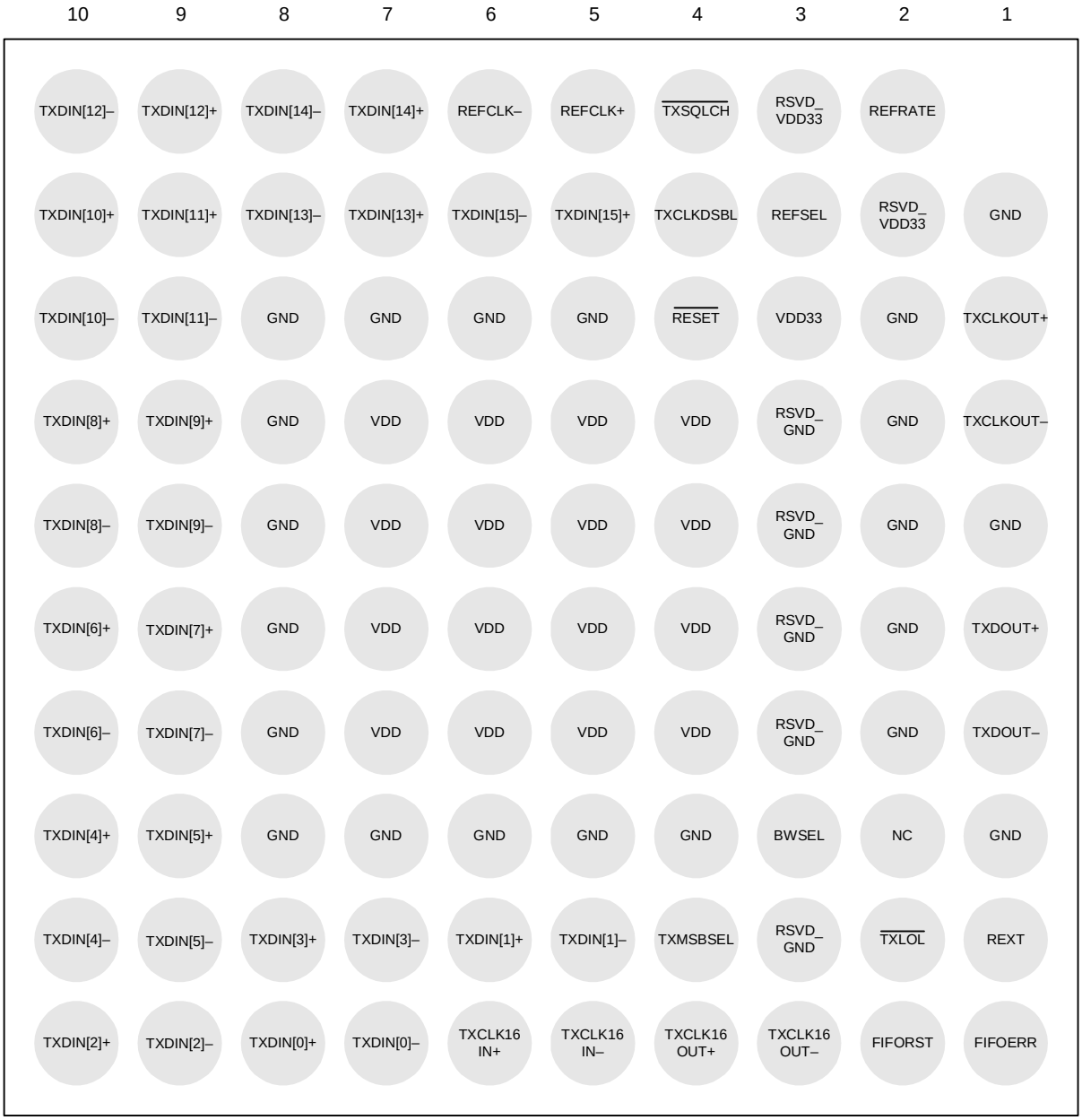


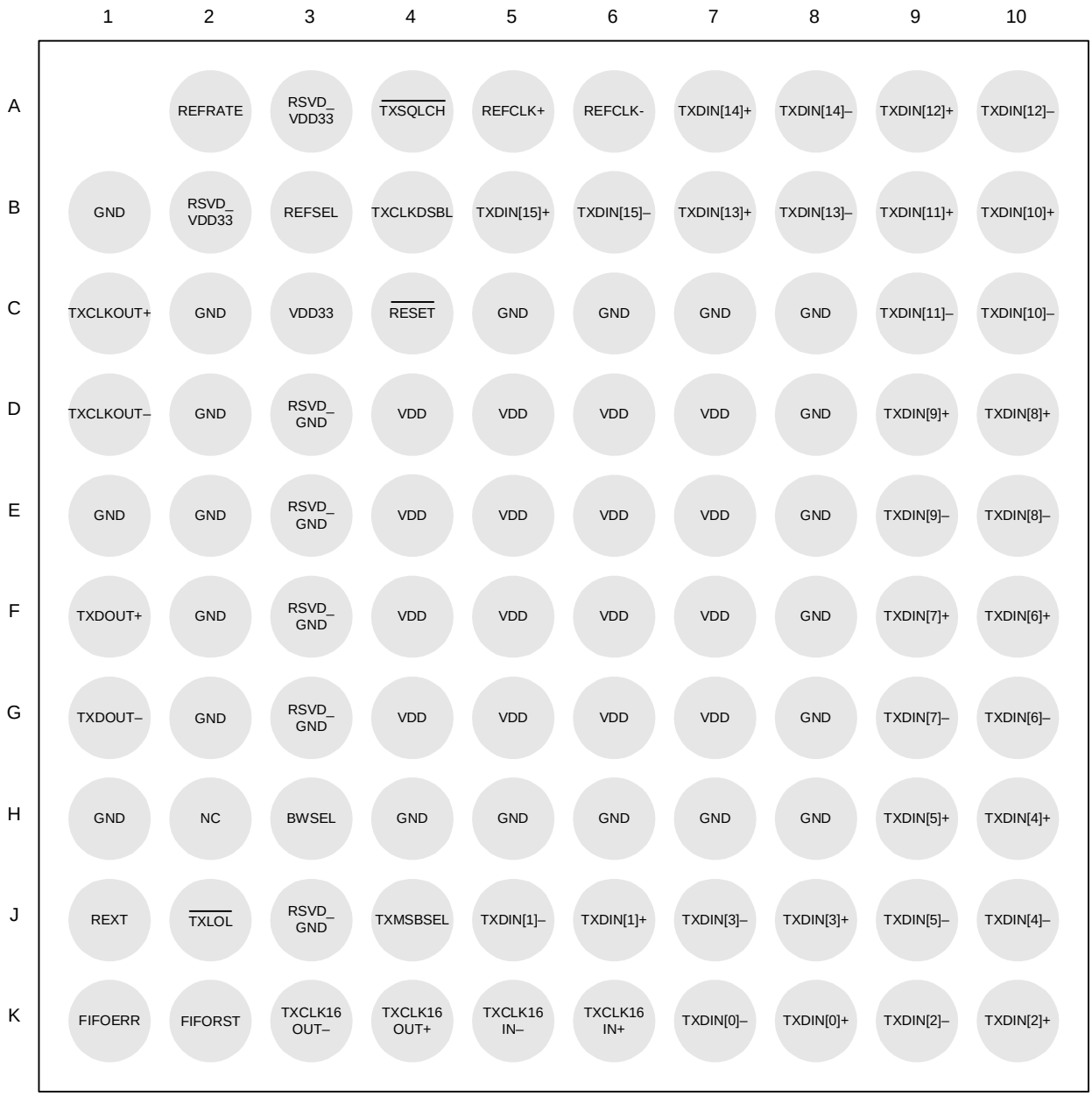
Figure 4. CML Output Driver Termination (TXCLKOUT, TXDOUT)

Si5540 Pinout: 99 BGA



Bottom View

Figure 5. Si5540 Pin Configuration (Bottom View)



Top View

Figure 6. Si5540 Pin Configuration (Transparent Top View)

Pin Descriptions: Si5540

Pin Number(s)	Pin Name	I/O	Signal Level	Description
H3	BWSEL	I	LVTTL	**Bandwidth Select DSPLL.** This input selects loop bandwidth of the DSPLL. BWSEL = 0: Loop bandwidth set to 12 kHz BWSEL = 1: Loop bandwidth set to 50 kHz.
K1	FIFOERR	O	LVTTL	**FIFO Error.** This output is driven high when a FIFO overflow/underflow has occurred. This output will stick high until reset by asserting FIFORST.
K2	FIFORST	I	LVTTL	**FIFO Reset.** This input, when asserted high, resets the read/write FIFO pointers to their initial state.
B1, C5–8, C2, D8, D2, E8, E1–2, F8, F2, G8, G2, H4–8, H1	GND	GND		**GND.**
H2	NC	—		**No Connect.** Reserved for device testing; leave electrically unconnected.
A5–6	REFCLK+, REFCLK–	I	LVPECL	**Differential Reference Clock.** The reference clock sets the operating frequency of the PLL used to generate the output clock frequency. The Si5540 will operate with reference clock frequencies that are either 1/16th or 1/64th the output clock rate.
A2	REFRATE	I	LVTTL	**Reference Frequency Select.** This input configures the CMU to operate with one of two possible reference clock frequencies. When REFRATE = 1, the CMU will operate with a reference that is 1/16th the output clock rate. When REFRATE = 0, the CMU will operate with a reference that is 1/64th the output clock rate.
B3	REFSEL	I	LVTTL	**Reference Clock Selection.** This inputs selects the reference clock source used by the CMU. When REFSEL = 0, the low speed data input clock, TXCLK16IN, is used as the CMU reference. When REFSEL = 1, the reference clock provided on REFCLK is used.
C4	$\overline{\text{RESET}}$	I	LVTTL	**Device Reset.** Forcing this input low for at least 1 µs will cause a device reset. For normal operation, this pin should be held high.

Pin Number(s)	Pin Name	I/O	Signal Level	Description
J1	REXT			**External Bias Resistor.** This resistor is used by onboard circuitry to establish bias currents within the device. This pin must be connected to GND through a 3.09 kΩ (1%) resistor.
D3, E3, F3, G3, J3	RSVD_GND	—		**Reserved Tie to Ground.** Must tie directly to GND for proper operation.
A3, B2	RSVD_VDD33	—		**Reserved Tie to VDD33.** Must tie directly to VDD33 for proper operation.
K5–6	TXCLK16IN–, TXCLK16IN+	I	LVDS	**Differential Data Clock Input.** The rising edge of this input clocks data present on TXDIN into the device.
K3–4	TXCLK16OUT+, TXCLK16OUT–	O	LVDS	**Divided Down Output Clock.** This clock output is generated by dividing down the high speed output clock, TXCLKOUT, by a factor of 16. It is intended for use in counter clocking schemes that transfer data between the system ASIC and the Si5540.
B4	TXCLKDSBL	I	LVTTL	**High Speed Clock Disable.** When this input is high, the output driver for TXCLKOUT is disabled. In applications that do not require the output data clock, the output clock driver should be disabled to save power.
C1, D1	TXCLKOUT+, TXCLKOUT–	O	CML	**High Speed Clock Output.** The high speed output clock, TXCLKOUT, is generated by the PLL in the clock multiplier unit. It's frequency is nominally 16 or 64 times the selected reference source.
A7–10, B5–10, C9–10, D9–10, E9–10, F9–10, G9–10, H9–10, J5–10, K7–10	TXDIN[15:0]–, TXDIN[15:0]+	I	LVDS	**Differential Parallel Data Input.** The 16-bit data word present on these pins is multiplexed into a high speed serial stream and output on TXDOUT. The data on these inputs is clocked into the device by the rising edge of TXCLKIN.
F1, G1	TXDOUT+, TXDOUT–	O	CML	**Differential High Speed Data Output.** The 16-bit word input on TXDIN[15:0] is multi-plexed into a high speed serial stream that is output on these pins. This output is updated by the rising edge of TXCLKOUT.
J2	$\overline{\text{TXLOL}}$	O	LVTTL	**CMU Loss-of-Lock.** The output is asserted low when the CMU is not phase locked to the selected reference source.

Pin Number(s)	Pin Name	I/O	Signal Level	Description
J4	TXMSBSEL	I	LVTTL	**Data Bus Transmit Order.** For TXMSBSEL = 0, data on TXDIN[0] is transmitted first followed by TXDIN[1] through TXDIN[15]. For TXMSBSEL = 1, TXDIN[15] is transmitted first followed by TXDIN[14] through TXDIN[0].
A4	$\overline{\text{TXSQLCH}}$	I	LVTTL	**Transmit Data Squelch.** If $\overline{\text{TXSQLCH}}$ is asserted low, the output data stream on TXDOUT will be forced to 0. If $\overline{\text{TXSQLCH}}$ = 1, TX squelching is turned off.
D4–7, E4–7, F4–7, G4–7,	VDD	VDD	1.8 V	**Supply Voltage.** Nominally 1.8 V.
C3	VDD33	VDD33	1.8 V or 3.3 V	**Digital Output Supply.** Must be tied to either 1.8 V or 3.3 V. When tied to 3.3 V, LVTTL compatible output voltage swings on $\overline{\text{TXLOL}}$ and FIFOERR are supported.

Ordering Guide

Table 7. Ordering Guide

Part Number	Package	Temperature
Si5540-BC	99 BGA	–40°C to 85°C

Package Outline

Figure 7 illustrates the package details for the Si5540. Table 8 lists the values for the dimensions shown in the illustration.

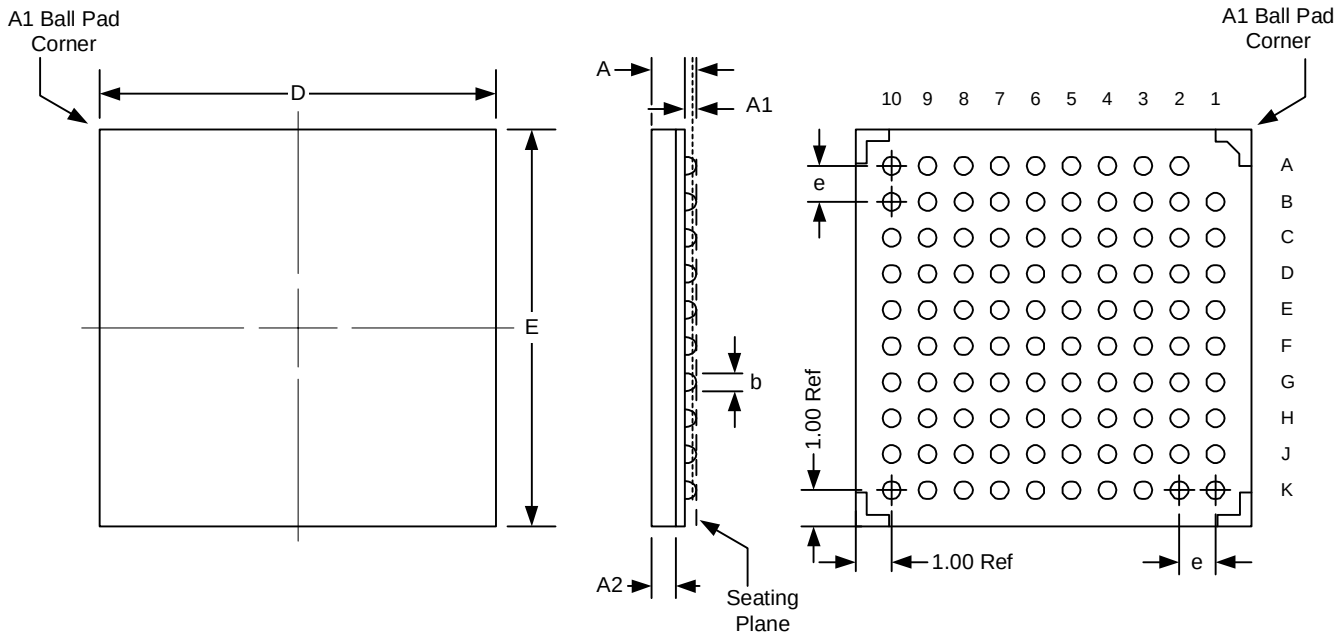


Figure 7. 99-Ball Grid Array (BGA)

Table 8. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	1.30	1.40	1.50
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	—	0.46	—
D	—	11.00	—
E	—	11.00	—
e	—	1.00	—

NOTES:

Contact Information

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