HM6709SH Series

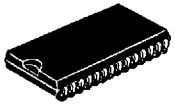
Preliminary

65,536-words x 4-Bit High Speed Static Random Access Memory

T-46-23-10

■ FEATURES

- 65,536-words x 4 bit organization
- Directly TTL compatible input and output
- 0.8 µm Hi-BiCMOS process
- +5V single supply
- Completely static memory
- No clock or timing strobe
- Low power dissipation (DC) operating: 400mW typ
- Super fast access time: 10/12ns (max)



(CP-28DN)

■ ORDERING INFORMATION

Type No.	Organ-ization	Access Time	Package
HM6709SH-10 HM6709SH-12	64kx4 with $\overline{OE}$	10 ns 12 ns	300 mil 28 pin Plastic SOJ (CP-28DN)

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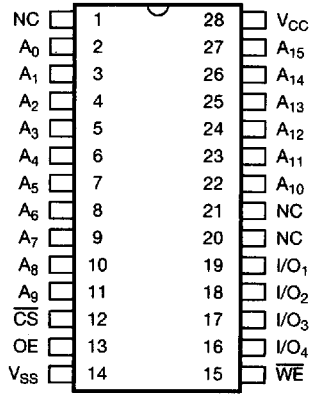
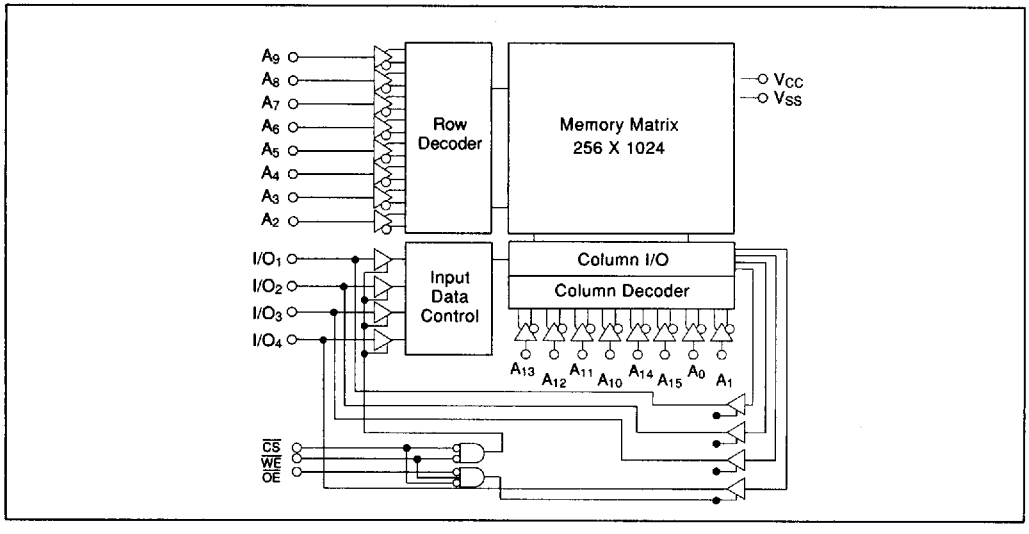


(Top View)

■ PIN DESCRIPTION

Pin Name	Function
A0–A15	Address Input
I/O1–I/O4	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
VSS	Ground
NC	Not Connect

■ BLOCK DIAGRAM



■ TRUTH TABLE

Input			Output	Mode	V_{CC} Current	Ref. Cycle
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$				
H	X	X	High Z	Not Selected	I_{SB}, I_{SB1}	–
L	H	H	High Z	Output Disable	I_{CC}, I_{CC1}	–
L	H	L	Data In	Read	I_{CC}, I_{CC1}	Read Cycle (1), (2), (3)
L	L	H	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (1), (2), (3), (4)
L	L	L	Data In	Write	I_{CC}, I_{CC1}	Write Cycle (5), (6)

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Rating	Unit
Supply Voltage[1]	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_t	-0.5 to V_{CC} +0.5	V
Power Dissipation	P_t	1.0	W
Operating Temperature Range	T_{ppr}	0 to +70	°C
Storage Temperature Range (with bias)	T_{stg} (bias)	–10 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Note: 1. With respect to V_{SS}.

■ RECOMMENDED DC OPERATING CONDITIONS ($0°C \le T_a \le 70°C$)

Item	Symbol	Min.	Typ	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0.0	0.0	0.0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
	V_{IL}	-3.0[1]	—	0.8	V

Note: 1. Pulse width 10 ns, DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5.0V ± 10%, V_{SS} = 0V, T_a = 0°C to +70°C)

Item	Symbol	Test Conditions	-10			-12			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Leakage	$I_{IL}I$	V_{CC} = 5.5V, V_{IN}=0V to V_{CC}	–	–	2	–	–	2	µA
Output Leakage Current	$I_{ILO}I$	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $\overline{WE}$ = V_{IL} V_{IO} = 0V to V_{CC}	–	–	10	–	–	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	–	60	100	–	60	100	mA
Average Operating Current	I_{CC1}	15ns cycle, $I_{I/O}$ = 0mA	–	130	180	–	120	175	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, V_{IN} =V_{IH} or V_{IL}	–	–	40	–	–	40	mA
	I_{SB1}	$\overline{CS}$ ≥ V_{CC} = 0.2V V_{IN} ≤ 0.2Vor V_{IN} ≥ V_{CC} = 0.2V	–	–	30	–	–	30	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA	–	–	0.4	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = .4mA	2.4	–	–	2.4	–	–	V

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■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0°C to +70°C, unless otherwise noted.)

• Read Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	10	–	12	–	ns
Address Access Time	t_{AA}	–	10	–	12	ns
Chip Select Access Time	t_{ACS}	–	10	–	12	ns
Chip Selection to Output in Low Z	t_{LZ}[1, 2]	3	–	4	–	ns
Output Enable to Output Valid	t_{OE}	–	5	–	6	ns
Output Enable to Output in Low Z	t_{OLZ}[1,2]	0	–	0	–	ns
Chip Deselection to Output in High Z	t_{HZ}[1,2]	0	5	0	5	ns
Output Hold from Address Change	t_{OH}	3	–	4	–	ns

Notes: 1. This parameter is sampled and not 100% tested.
2. Transition is measured ± 200 mV from steady state voltage with specified loading in Load (B).

2

• Write Cycle

Item	Symbol	-10		-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}[1]	11	–	12	–	ns
Chip Selection to End of Write	t_{CW}	8	–	9	–	ns
Address Valid to End of Write	t_{AW}	10	–	11	–	ns
Address Setup Time	t_{AS}	0	–	0	–	ns
Write Pulse Width	t_{WP}	8	–	9	–	ns
Write Recovery Time	t_{WR}	0	–	0	–	ns
Data Valid to End of Write	t_{DW}	6	–	6	–	ns
Data Hold Time	t_{DH}	0	–	0	–	ns
Write Enable to Output in High Z	t_{WZ}[2,3]	0	5	0	6	ns
Output Disable to Output in High Z	t_{OHZ}[2,3]	0	6	0	6	ns
Output Active from End of Write	t_{OW}[2,3]	4	–	4	–	ns

Notes: 1. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
2. This parameter is sampled and not 100% tested.
3. Transition is measured in ± 200 mV from steady state voltage with specified loading in load (B).

• **Capacitance**

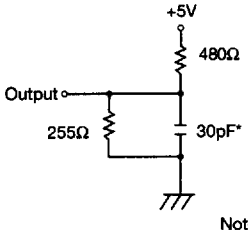
Item	Symbol	Max.	Unit	Test Condition
Input Capacitance	C_{in}[1]	6	pF	V_{IN} = 0V
Input/Output Capacitance	$C_{I/O}$[1]	10	pF	$V_{I/O}$ = 0V

■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = to 70°C)

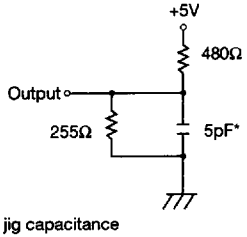
Test Conditions

- Input pulse levels: V_{SS} to 3.0V
- Input timing reference levels: 1.5V
- Output Load: See figure
- Input rise and fall times: 4ns
- Output reference levels: 1.5V

Output load (A)



Output Load (B)
(for t_{HZ}, t_{LZ}, t_{OHZ}, t_{OLZ}, t_{WZ}, & t_{OW})



Note: * Including scope and jig capacitance

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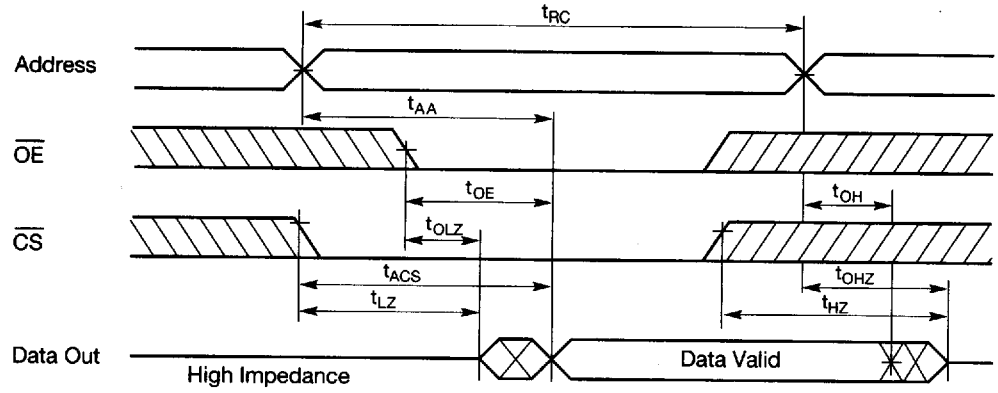
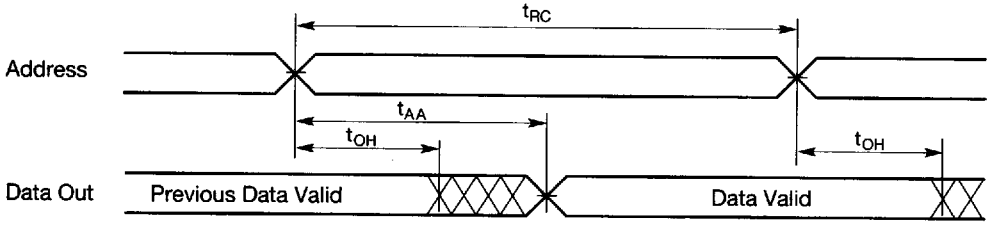
■ READ CYCLE (1)[1]



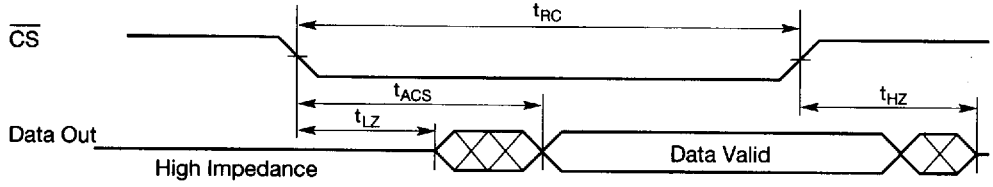
Notes: 1. $\overline{WE}$ = V_{IH}

■ READ CYCLE (2)[1,2,3]



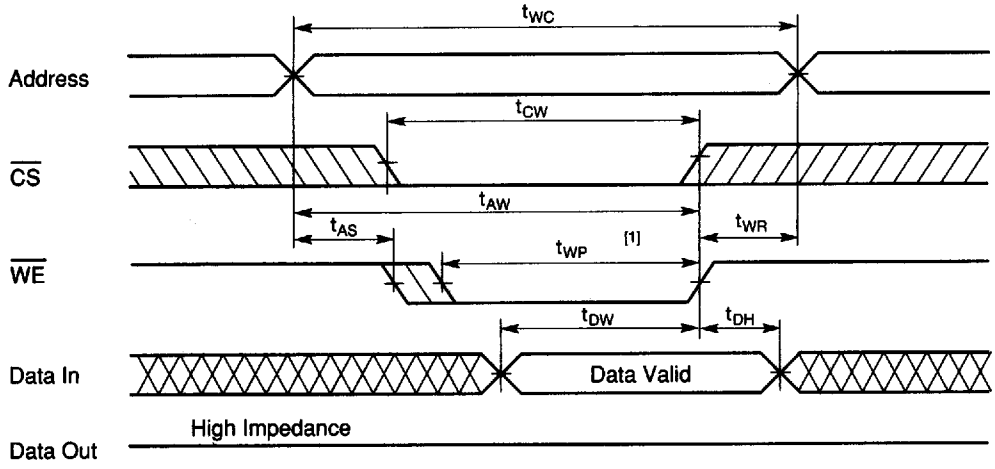
Notes: 1. $\overline{WE}$ = V_{IH}
2. $\overline{CS}$ = V_{IL}
3. $\overline{OE}$ = V_{IL}

■ READ CYCLE (3)[1,2,3]



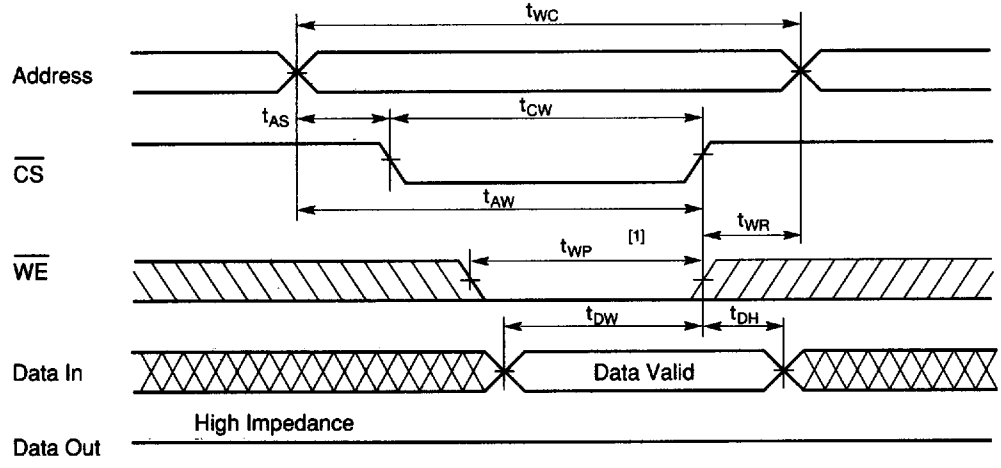
Notes: 1. $\overline{WE}$ = V_{IH}
2. OE = V_{IL}
3. Address valid prior to or coincident with $\overline{CS}$ transition low.

■ WRITE CYCLE (1)[1] ($\overline{OE}$ = H, $\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

■ WRITE CYCLE (2)[1] ($\overline{OE}$ = H, $\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

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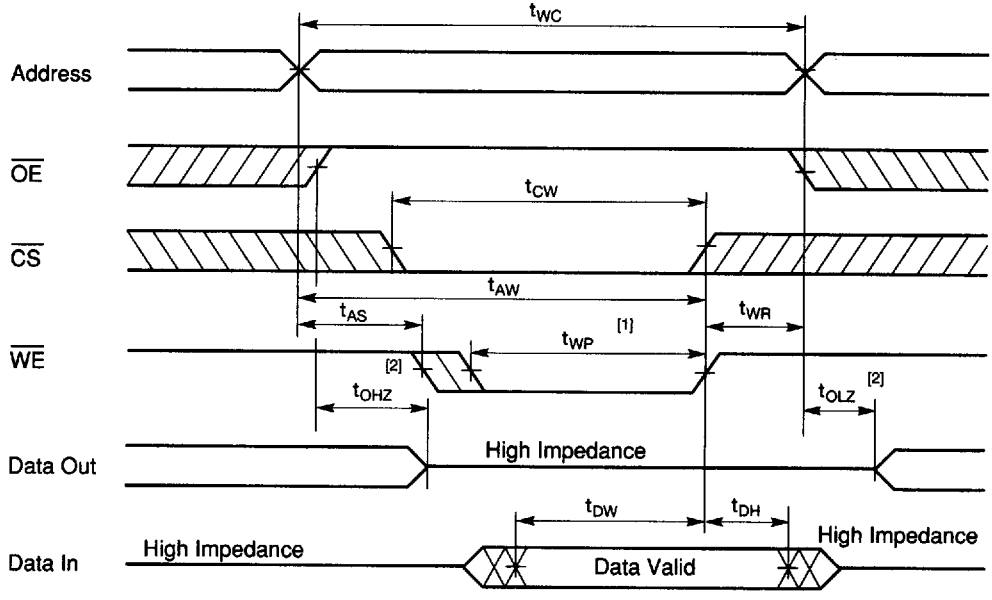
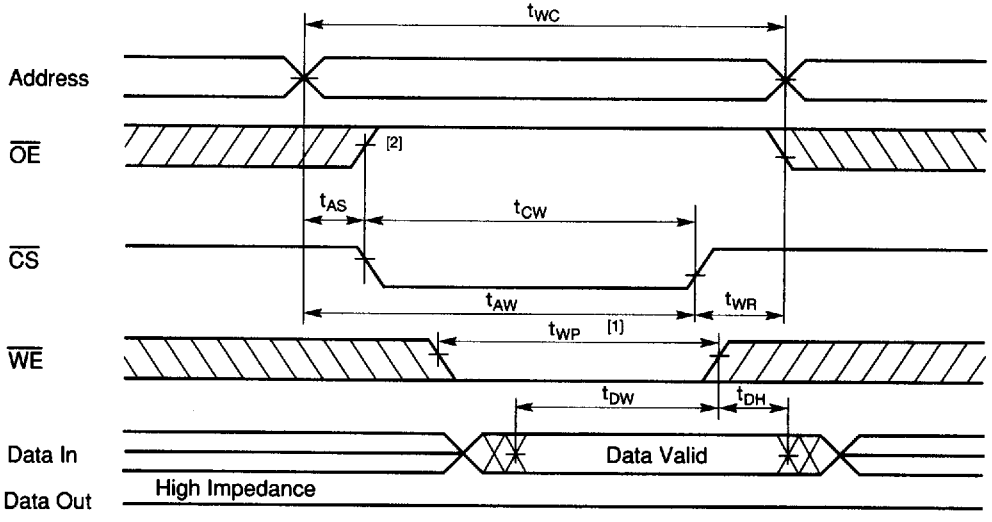
■ WRITE CYCLE (3)[1,2] ($\overline{OE}$ = Clocked, $\overline{WE}$ Controlled)



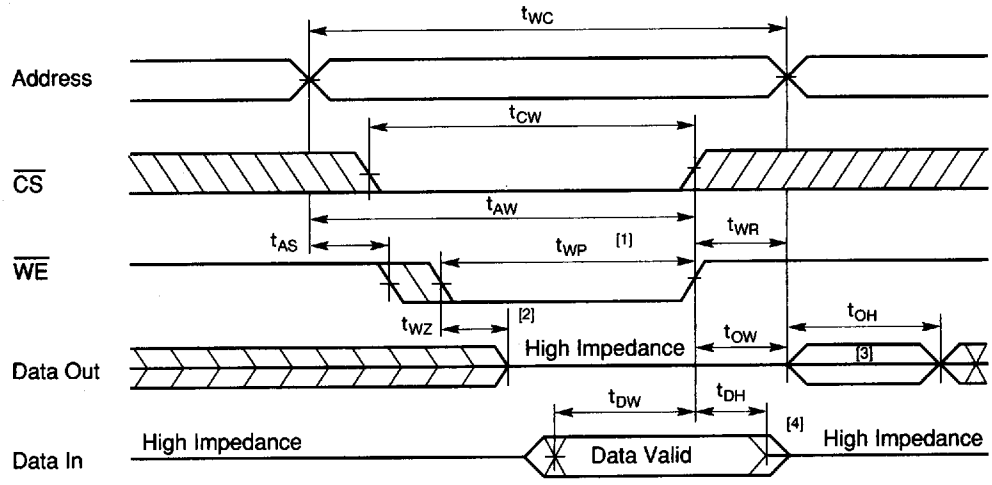
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. During this period, I/O pins are in the output state so that the input state of opposite phase to the outputs must not be applied.

■ WRITE TIMING WAVEFORM (4)[1,2] ($\overline{OE}$ = Clocked $\overline{CS}$ Controlled)



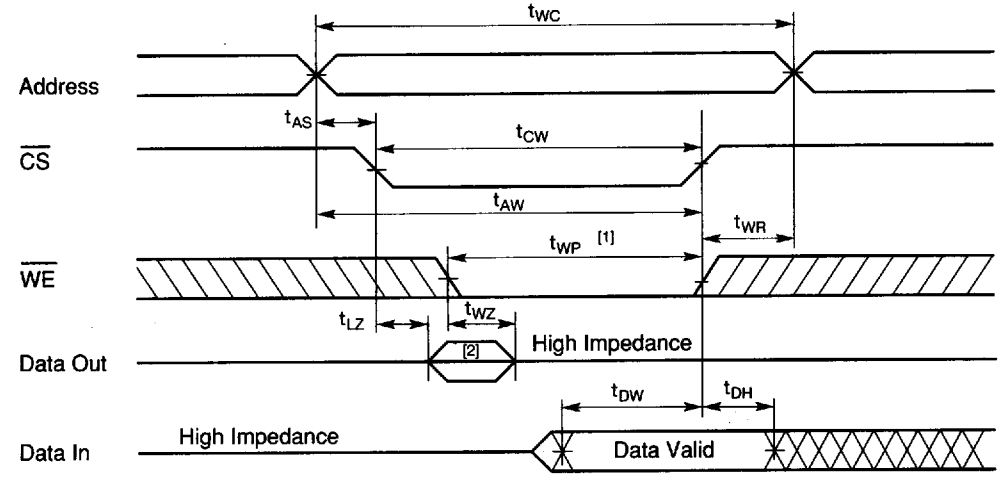
Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).

■ WRITE CYCLE (5)[1,2,3,4] ($\overline{OE}$ = L, $\overline{WE}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. During this period, I/O pins are output state so that the input signals of opposite phase to the outputs must not be applied.
3. Output data is the same phase of write data of this write cycle.
4. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

■ WRITE CYCLE (6)[1,2,3,4] ($\overline{OE}$ = L, $\overline{CS}$ Controlled)



Notes: 1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$ (twp).
2. If the $\overline{CS}$ low transition occurs after the $\overline{WE}$ low transition, output remain in a high impedance state.