HARRIS

HI-222/883

T-51-11

January 1989

High Frequency/Video Switch

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Wideband Operation .... 150 MHz**
- **Differential Gain .... 0.03% (Typ) 0.1% (Max)**
- **Differential Phase .... 0.003 Degrees (Typ) 0.01 Degrees (Max)**
- **Switching Speed .... 100ns (Typ) 200ns (Max)**
- **R_{ON} .... 35Ω (Typ) 75Ω (Max)**
- **Off Isolation @ 10 MHz .... -65dB (Typ) -60dB (Max)**
- **Crosstalk @ 10 MHz .... -80dB (Typ) -75dB (Max)**

Applications

- **Routing Switchers**
- **Production Mixers**
- **High Definition TV**
- **Radar Signal Conditioning**
- **Medical Imaging**
- **Heads-Up Displays**
- **Simulators**
- **Sonar**

Description

The HI-222/883 is a high frequency analog switch that complements the Harris family of high speed op amps and buffers. Fabricated with our Dielectric Isolation process and using silicon gate technology, many key parameters have been enhanced.

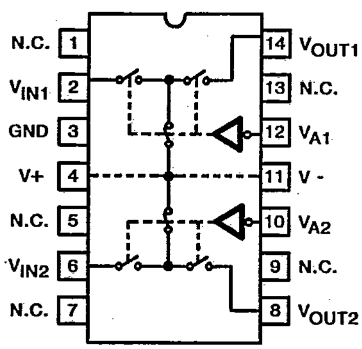
Crosstalk and off isolation are optimized with a T-switch configuration and the use of nonconnected pins for extended shielding. Other features of the HI-222/883 include wideband operation, low R_{ON}, fast switching speeds and low differential gain and phase. The characteristics of this TTL compatible device make it ideal for designs where improved switching performance is required.

The primary application of this dual SPST switch is the routing of high frequency signals in equipment ranging from video production mixers to military RF circuits.

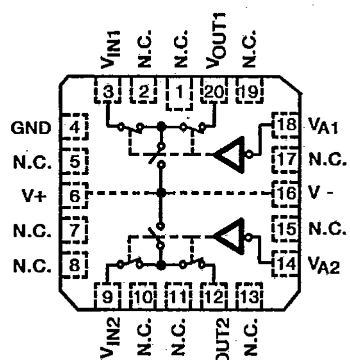
The HI-222/883 is available in a 14 pin Ceramic DIP or a 20 pin Ceramic LCC and is specified over the -55°C to +125°C temperature range.

Pinouts

HI1-222/883 (CERAMIC DIP)
LOGIC "1" INPUT
TOP VIEW



HI4-222/883 (CERAMIC LCC)
LOGIC "0" INPUT
TOP VIEW



NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance. All nonconnected pins should be tied to ground.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
$\pm V_{SUPPLY}$ to Ground (V+, V-) .... ±18V
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $+V_{SUPPLY}$ +2V
$-V_{SUPPLY}$ -2V
Peak Current (Source to Drain)
(Pulse at 0.8ms, 10% Duty Cycle Max) 100mA
Peak Current (Any Pin, 50% Duty Cycle) 28mA
Continuous Current (Any Pin) 15mA
Junction Temperature .... +175°C
Storage Temperature Range .... -65°C to +150°C
ESD Rating .... < 2000V
Lead Temperature (Soldering 10 sec) .... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C
Ceramic DIP Package 1.0W
Ceramic LCC Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package .... 13.4mW/°C
Ceramic LCC Package .... 13.2mW/°C

CAUTION: Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Operating Supply Voltage .... ±15V
Analog Input Voltage (V_S) .... $\pm V_{SUPPLY}$
Address Low Level (V_{AL}) .... 0V to 0.8V
Address High Level (V_{AH}) .... 2.0V to +5.0V
Ground All Nonconnected Pins.

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = +0.8V, Unused Pins are Grounded.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Switch "ON" Resistance	R_{DS}	V_D = 5V, I_S = 7.5mA S1/S2	1	+25°C	-	60	Ω
			2, 3	-55°C to +125°C	-	75	Ω
		V_D = -5V, I_S = -7.5mA S1/S2	1	+25°C	-	60	Ω
			2, 3	-55°C to +125°C	-	75	Ω
Source "OFF" Leakage Current	$I_{S(OFF)}$	V_S = 5V, V_D = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_S = -5V, V_D = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Drain "OFF" Leakage Current	$I_{D(OFF)}$	V_D = 5V, V_S = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = -5V, V_S = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Channel "ON" Leakage Current	$I_{D(ON)}$	V_D = V_S = 5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
		V_D = V_S = -5V S1/S2	1	+25°C	-2.5	2.5	nA
			2, 3	-55°C to +125°C	-200	200	nA
Low Level Address Current	I_{AL}	V_A = 0.8V A_1, A_2	1	+25°C	-	1.0	µA
			2, 3	-55°C to +125°C	-	1.0	µA
High Level Address Current	I_{AH}	V_A = 2.0V A_1, A_2	1	+25°C	-	1.0	µA
			2, 3	-55°C to +125°C	-	1.0	µA
Positive Supply Current	$+I_{CC}$	V_A = 0.8V, 2.0V A_1, A_2	1	+25°C	-	4.0	mA
			2, 3	-55°C to +125°C	-	6.0	mA
Negative Supply Current	$-I_{CC}$	V_A = 0.8V, 2.0V A_1, A_2	1	+25°C	-4.0	-	mA
			2, 3	-55°C to +125°C	-6.0	-	mA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = 0.8V, Ground All Nonconnected Pins.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Turn "ON" Time	t_{ON}	V_S = 5V, C_L = 35pF, R_L = 2kΩ	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	200	ns
Turn "OFF" Time	t_{OFF}	V_S = 5V, C_L = 35pF, R_L = 2kΩ	9	+25°C	-	150	ns
			10, 11	-55°C, +125°C	-	200	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: Supply Voltage = ±15V, V_{AH} = 2.0V, V_{AL} = 0.8V, Ground All Nonconnected Pins.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
"On" Resistance Match (Channel to Channel)	R_{ON} Match	V_D = ±5V, I_D = 7.5mA	1	+25°C	-	5	Ω
Address Capacitance	C_A	V_A = 2.0V, 0.8V	1	+25°C	-	10	pF
Switch Input Capacitance	$C_{S(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	25	pF
Switch Output Capacitance	$C_{D(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	60	pF
	$C_{D(ON)}$	Switch On: V_A = 0.8V	1	+25°C	-	150	pF
Drain to Source Capacitance	$C_{DS(OFF)}$	Switch Off: V_A = 2.0V	1	+25°C	-	2.0	pF
Off Isolation	V_{ISO}	V_S = 300mV_{P-P} @ f = 10MHz, R_L = 50Ω	1	+25°C	-	-60	dB
Crosstalk	V_{CT}	V_S = 300mV_{P-P} @ f = 10MHz, R_L = 50Ω	1	+25°C	-	-75	dB
Gain Tolerance	Av±	V_S = 300mV_{P-P} R_L = 50Ω @ 1MHz	1	+25°C	-	-0.1	dB
		V_S = 300mV_{P-P} R_L = 50Ω @ 8MHz	1	+25°C	-	-0.5	dB
Differential Gain	A_{DIFF}	V_S = 300mV_{P-P}, R_L = 2kΩ, V_{OFFSET} = 0V to 1V, f = 3.58MHz and 4.43MHz	1	+25°C	-	0.1	%
Differential Phase	Δ_{DIFF}		1	+25°C	-	0.01	Degrees

NOTE 1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

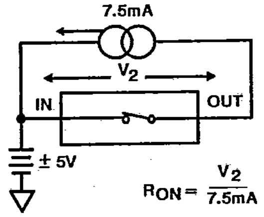
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

* PDA applies to Subgroup 1 only.

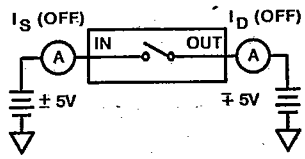
Test Circuits

R_{DS}



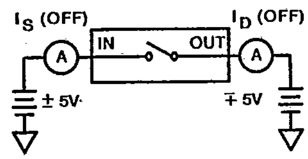
$V_{IN} = \pm5V$, $I = 7.5mA$, $V_A = 0.8V$

$I_{S(OFF)}$



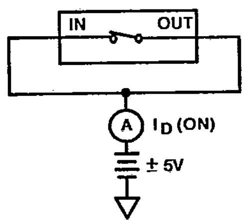
$V_{IN} = \pm5V$, $V_{OUT} = \mp5V$, $V_A = 2.0V$

$I_{D(OFF)}$



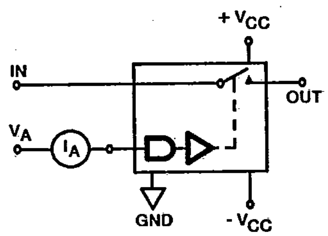
$V_{IN} = \pm5V$, V_{OUT} $\mp5V$, $V_A = 2.0V$

$I_{D(ON)}$



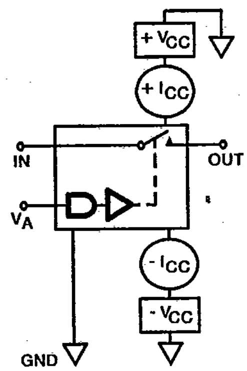
$V_{IN} = \pm5V$, $V_{OUT} = \pm5V$, $V_A = 0.8V$

ADDRESS CURRENT



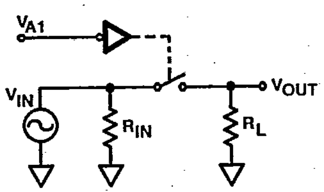
$V_{AH} = 2.0V$, $V_{AL} = 0.8V$

SUPPLY CURRENTS



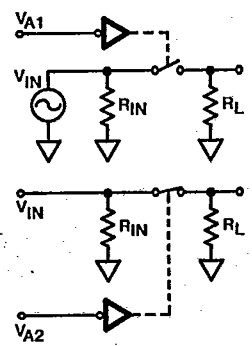
$V_A = 0.8V, 2.0V$

OFF ISOLATION



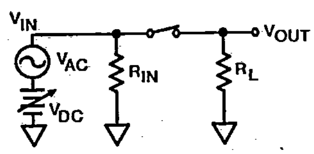
$V_{IN} = 300mV_{p-p}$, $f = 10MHz$, $R_{IN} = R_L = 50\Omega$, $V_{A1} = 2.0V$

CROSSTALK



$V_{IN} = 300mV_{p-p}$, $f = 10MHz$, $R_{IN} = R_L = 50\Omega$
$V_{A1} = 2.0V$, $V_{A2} = 0.8V$

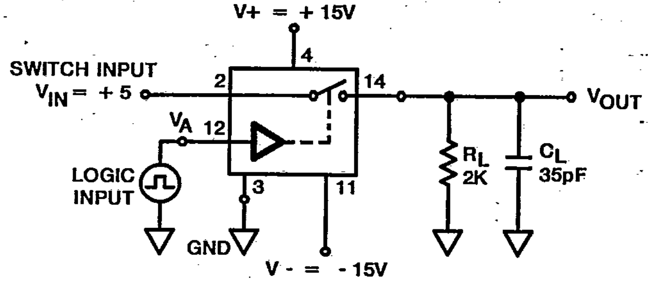
DIFFERENTIAL GAIN, PHASE



$V_{AC} = 300mV_{p-p}$, $f = 3.58MHz$ and $4.43MHz$,
$V_{DC} = 0.0V$ to $1.0V$, $R_L = 2k\Omega$, $R_{IN} = 50\Omega$

Test Circuit

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1})

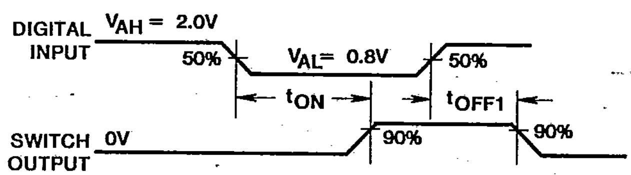


$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

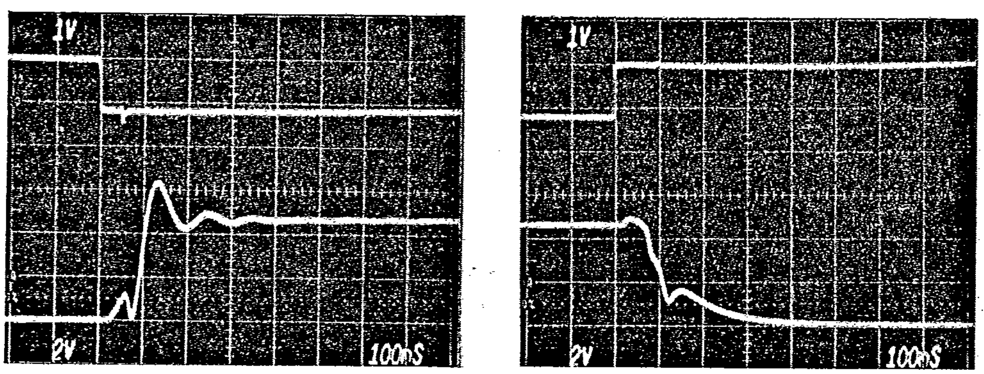
C_L Includes $C_{FIXTURE}$ + C_{PROBE}

Switching Waveforms

LOGIC "0" = SWITCH ON



t_{ON}, t_{OFF} (TTL INPUT), V_{AL} = 0.8V, V_{AH} = 2.0V



Top: TTL Input (1V/Div.)
Bottom: Output (2V/Div.)
Horizontal: 100ns/Div.

Burn-In Circuits

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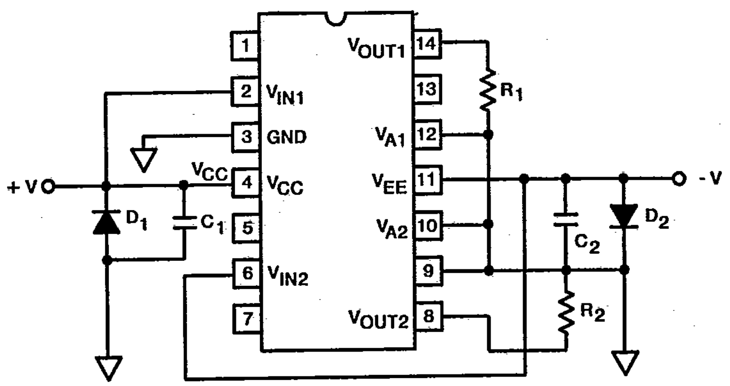
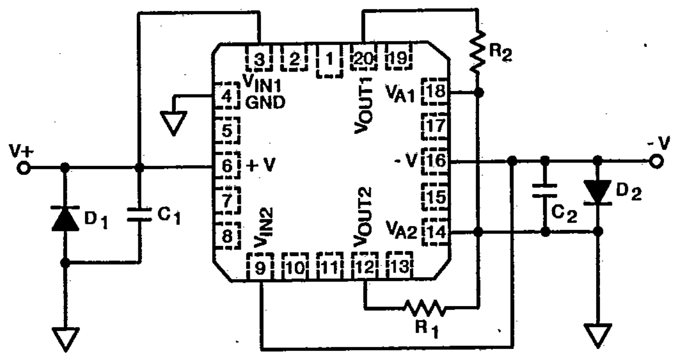
HI-222/883 CERAMIC DIP

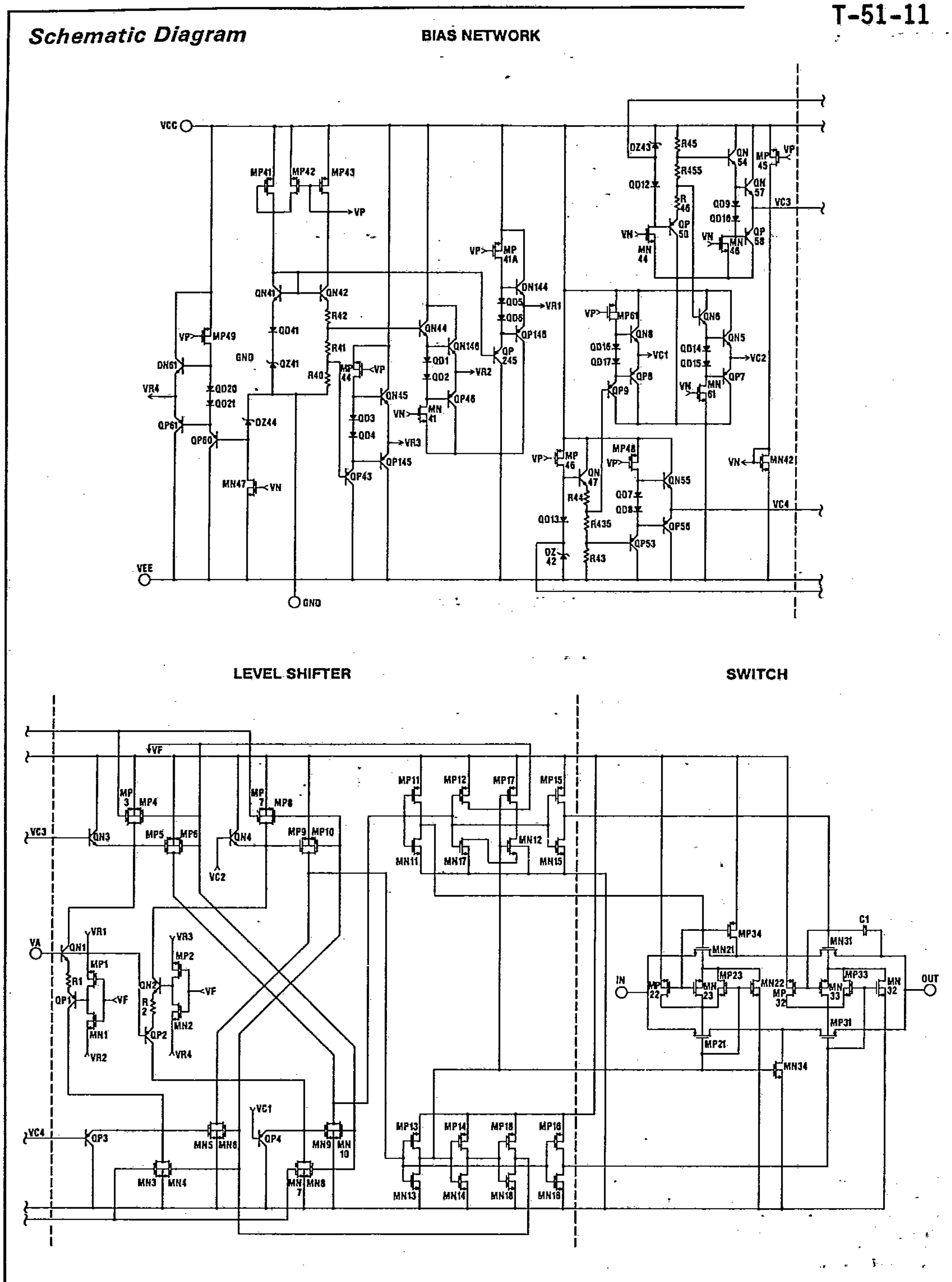


HI-222/883 CERAMIC LCC



NOTES:
Both Switches Are On, One Sourcing 1.5mA and the Other Sinking 1.5mA.
$R_1 = R_2 = 10k\Omega$, ±5%, per Socket, 1/4W (Min)
C_1, C_2 = 0.01μF/Socket (Min) or 0.1μF/Row, (Min)
D_1, D_2 = IN4002 or Equivalent/Board
$|(V+) - (V-)| = 30V$
Pin 9 May Be Tied to Ground or Left Open on Ceramic DIP Circuit.

Schematic Diagram



Die Characteristics

DIE DIMENSIONS:
124 x 79 x 19 mils
(3120 x 1440 x 480 μm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
0.93×10^5 A/cm^2 at 15mA (Continuous)

GLASSIVATION:
Type: Nitride
Thickness: 7.0kÅ ± 0.75kÅ

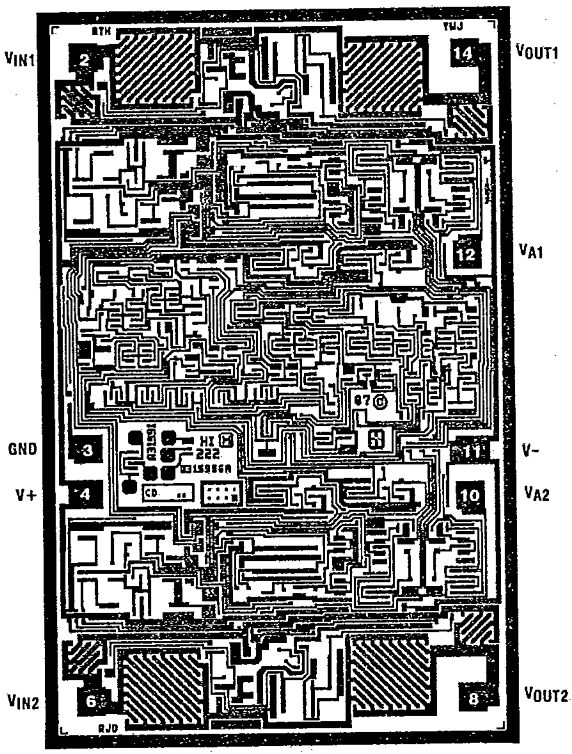
DEVICE COUNT: 183

PROCESS: Silicon Gate/DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

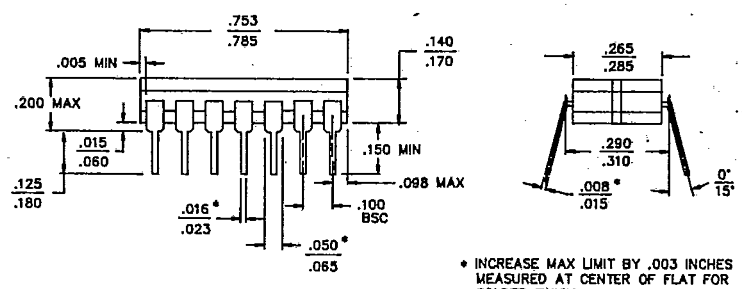
HI-222/883



NOTE: Pin Numbers Correspond to Ceramic DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

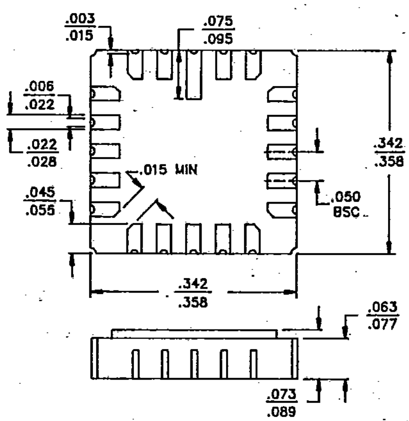


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

HARRIS

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DESIGN INFORMATION

High Frequency/Video Switch

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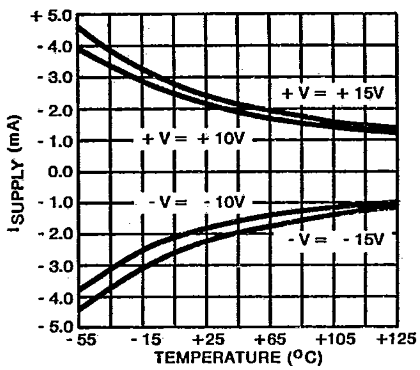
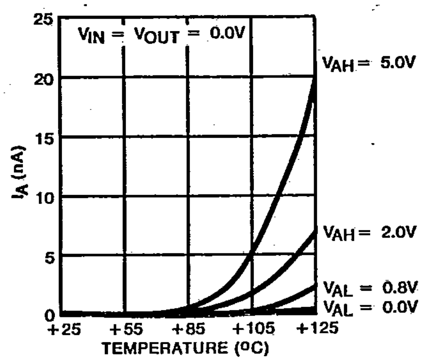
Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

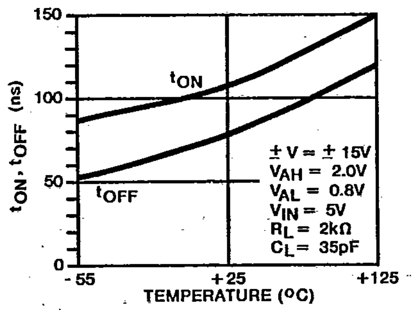
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



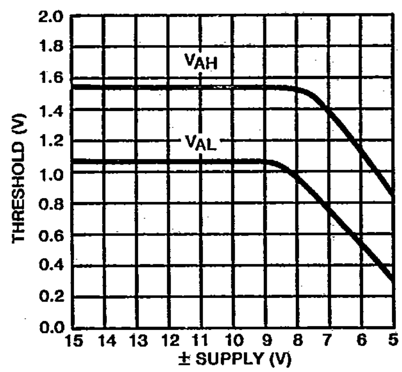
STEADY STATE ADDRESS INPUT CURRENT vs. TEMPERATURE



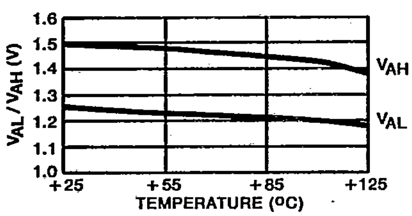
SWITCHING TIME vs. TEMPERATURE



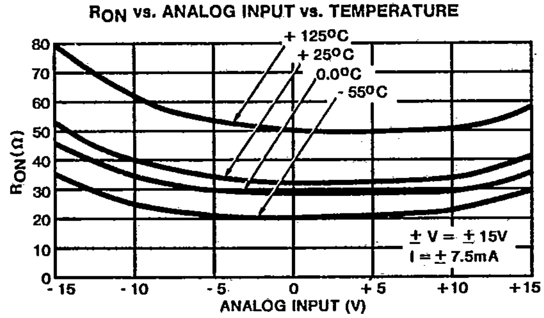
SWITCHING THRESHOLD vs. ± SUPPLY VOLTAGE



ADDRESS INPUT THRESHOLD vs. TEMPERATURE



R_{ON} vs. ANALOG INPUT vs. TEMPERATURE



DESIGN INFORMATION (Continued)

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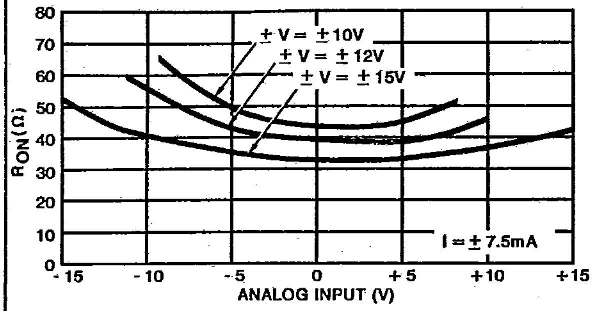
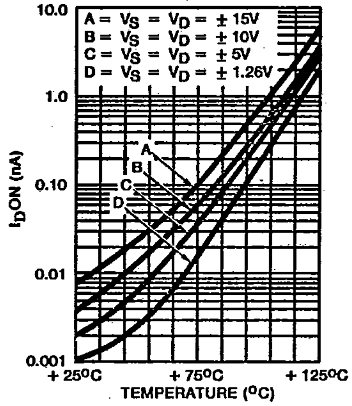
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

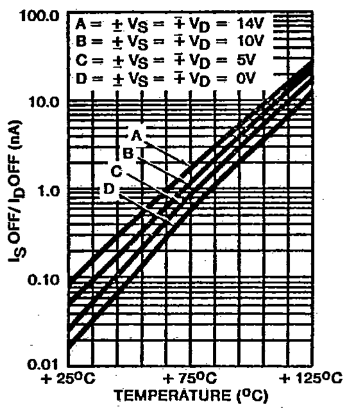
R_{ON} vs. ANALOG INPUT vs. SUPPLY VOLTAGE



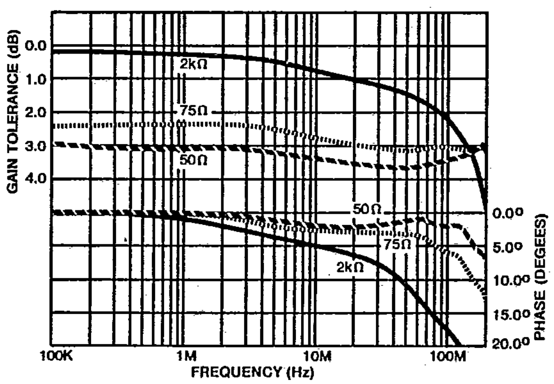
I_{SOFF}/I_{DOFF} vs. TEMPERATURE vs. ANALOG INPUT



I_DON vs. TEMPERATURE vs. ANALOG INPUT



BANDWIDTH



DESIGN INFORMATION (Continued)

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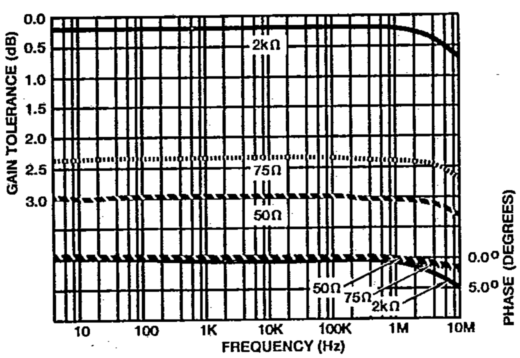
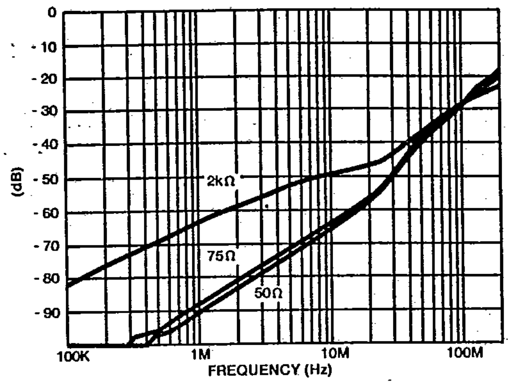
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

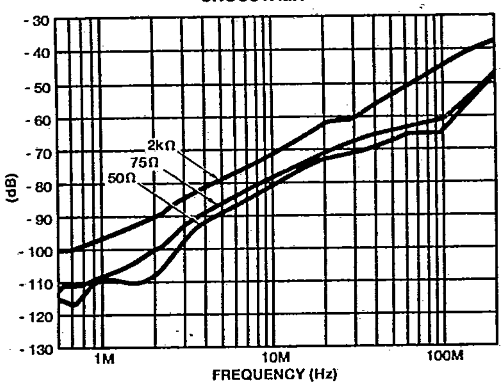
GAIN TOLERANCE



OFF ISOLATION



CROSSTALK



TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, $R_L = 50\Omega$, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	UNITS
Differential Gain	$V_S = 300mV_{P-P}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 2k\Omega$	+25°C	0.03	%
	$V_S = 300mV_{P-P}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 50\Omega$	+25°C	0.3	%
Differential Phase	$V_S = 300mV_{P-P}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 2k\Omega$	+25°C	0.003	Degrees
	$V_S = 300mV_{P-P}$, $V_{Offset} = 0.0V$ to 1.0V f = 3.58MHz, 4.43MHz @ $R_L = 50\Omega$	+25°C	0.2	Degrees