

## Radiation Hardened, SEGR Resistant N-Channel Power MOSFET



Intersil Star\*Power Rad Hard MOSFETs have been specifically developed for high performance applications in a commercial or military space environment.

Star\*Power MOSFETs offer the system designer both extremely low  $r_{DS(ON)}$  and Gate Charge allowing the development of low loss Power Subsystems. Star\*Power Gold FETs combine this electrical capability with total dose radiation hardness up to 100 krad while maintaining the guaranteed performance for Single Event Effects (SEE) which the Intersil FS families have always featured.

The Intersil family of Star\*Power FETs includes a series of devices in various voltage, current and package styles. The portfolio consists of Star\*Power and Star\*Power Gold products. Star\*Power FETs are optimized for total dose and  $r_{DS(ON)}$  while exhibiting SEE capability at full rated voltage up to an LET of 37. Star\*Power Gold FETs have been optimized for SEE and Gate Charge combining SEE performance to 80% of the rated voltage for an LET of 82 with extremely low gate charge characteristics.

This MOSFET is an enhancement-mode silicon-gate power field effect transistor of the vertical DMOS (VDMOS) structure. It is specifically designed and processed to be radiation tolerant. The MOSFET is well suited for applications exposed to radiation environments such as switching regulation, switching converters, power distribution, motor drives and relay drivers as well as other power control and conditioning applications. As with conventional MOSFETs these Radiation Hardened MOSFETs offer ease of voltage control, fast switching speeds and ability to parallel switching devices.

Reliability screening is available as either TXV or Space equivalent of MIL-PRF-19500.

Formerly available as type TA45222W.

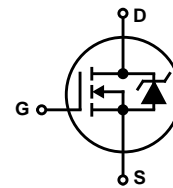
### Ordering Information

RAD LEVEL	SCREENING LEVEL	PART NUMBER/BRAND
10K	Engineering Samples	FSGYE033D1
100K	TXV	FSGYE033R3
100K	Space	FSGYE033R4

### Features

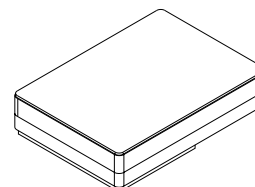
- 20A (Current Limited by Package), 30V,  $r_{DS(ON)} = 0.014\Omega$
- UIS Rated
- Total Dose
  - Meets Pre-RAD Specifications to 100 krad (Si)
- Single Event
  - Safe Operating Area Curve for Single Event Effects
  - SEE Immunity for LET of 82MeV/mg/cm<sup>2</sup> with  $V_{DS}$  up to 80% of Rated Breakdown
- Dose Rate
  - Typically Survives 3E9 RAD (Si)/s at 80%  $BV_{DSS}$
  - Typically Survives 2E12 if Current Limited to  $I_{AS}$
- Photo Current
  - 1.0nA Per-RAD (Si)/s Typically
- Neutron
  - Maintain Pre-RAD Specifications for 3E13 Neutrons/cm<sup>2</sup>
  - Usable to 3E14 Neutrons/cm<sup>2</sup>

### Symbol



### Packaging

SMD.5



# FSGYE033R

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	FSGYE033R	UNITS
Drain to Source Voltage	30	V
Drain to Gate Voltage ( $R_{GS} = 20\text{k}\Omega$ )	30	V
Continuous Drain Current		
$T_C = 25^\circ\text{C}$	20 (Note)	A
$T_C = 100^\circ\text{C}$	20 (Note)	A
Pulsed Drain Current	80	A
Gate to Source Voltage	$\pm 24$	V
Maximum Power Dissipation		
$T_C = 25^\circ\text{C}$	75	W
$T_C = 100^\circ\text{C}$	30	W
Linear Derating Factor	0.60	W/ $^\circ\text{C}$
Single Pulsed Avalanche Current, $L = 100\mu\text{H}$ , (See Test Figure)	70	A
Continuous Source Current (Body Diode)	20	A
Pulsed Source Current (Body Diode)	80	A
Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
Lead Temperature (During Soldering) (Distance $>0.063\text{in}$ (1.6mm) from Case, 10s Max)	300	$^\circ\text{C}$
Weight (Typical)	1.0 (Typical)	g

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE: Current limited by package.

## Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 1\text{mA}$ , $V_{GS} = 0\text{V}$	30	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 1\text{mA}$	$T_C = -55^\circ\text{C}$	-	-	5.5	V
			$T_C = 25^\circ\text{C}$	2.0	-	4.5	V
			$T_C = 125^\circ\text{C}$	1.0	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 24\text{V}$ , $V_{GS} = 0\text{V}$	$T_C = 25^\circ\text{C}$	-	-	25	$\mu\text{A}$
			$T_C = 125^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 24\text{V}$	$T_C = 25^\circ\text{C}$	-	-	100	nA
			$T_C = 125^\circ\text{C}$	-	-	200	nA
Drain to Source On-State Voltage	$V_{DS(ON)}$	$V_{GS} = 12\text{V}$ , $I_D = 20\text{A}$	-	-	0.280	V	
Drain to Source On Resistance	$r_{DS(ON)12}$	$I_D = 20\text{A}$ , $V_{GS} = 12\text{V}$	$T_C = 25^\circ\text{C}$	-	0.012	0.014	$\Omega$
			$T_C = 125^\circ\text{C}$	-	-	0.023	$\Omega$
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = 15\text{V}$ , $I_D = 20\text{A}$ , $R_L = 0.75\Omega$ , $V_{GS} = 12\text{V}$ , $R_{GS} = 7.5\Omega$	-	-	20	ns	
Rise Time	$t_r$		-	-	55	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	-	30	ns	
Fall Time	$t_f$		-	-	15	ns	
Total Gate Charge	$Q_{g(12)}$	$V_{GS} = 0\text{V}$ to $12\text{V}$	$V_{DD} = 15\text{V}$ , $I_D = 20\text{A}$	-	35	38	nC
Gate Charge Source	$Q_{gs}$			-	11	14	nC
Gate Charge Drain	$Q_{gd}$			-	8	10	nC
Gate Charge at 20V	$Q_{g(20)}$	$V_{GS} = 0\text{V}$ to $20\text{V}$		-	60	-	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0\text{V}$ to $2\text{V}$		-	4	-	nC
Plateau Voltage	$V_{(PLATEAU)}$	$I_D = 20\text{A}$ , $V_{DS} = 15\text{V}$	-	5.5	-	V	
Input Capacitance	$C_{ISS}$	$V_{DS} = 25\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$	-	1850	-	pF	
Output Capacitance	$C_{OSS}$		-	1120	-	pF	
Reverse Transfer Capacitance	$C_{RSS}$		-	35	-	pF	
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.67	-	$^\circ\text{C/W}$

**Source to Drain Diode Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	$V_{SD}$	$I_{SD} = 20A$	-	-	1.2	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 20A, dI_{SD}/dt = 100A/\mu s$	-	-	80	ns
Reverse Recovery Charge	$Q_{RR}$		-	100	-	nC

**Electrical Specifications up to 100K RAD**  $T_C = 25^\circ C$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Drain to Source Breakdown Volts (Note 3)	$BV_{DSS}$	$V_{GS} = 0, I_D = 1mA$	30	-	V
Gate to Source Threshold Volts (Note 3)	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 1mA$	2.0	4.5	V
Gate to Body Leakage (Notes 2, 3)	$I_{GSS}$	$V_{GS} = \pm 24V, V_{DS} = 0V$	-	100	nA
Zero Gate Leakage (Note 3)	$I_{DSS}$	$V_{GS} = 0, V_{DS} = 24V$	-	25	$\mu A$
Drain to Source On-State Volts (Notes 1, 3)	$V_{DS(ON)}$	$V_{GS} = 12V, I_D = 20A$	-	0.280	V
Drain to Source On Resistance (Notes 1, 3)	$r_{DS(ON)12}$	$V_{GS} = 12V, I_D = 20A$	-	0.014	$\Omega$

NOTES:

1. Pulse test, 300 $\mu s$  Max.
2. Absolute value.
3. Insitu Gamma bias must be sampled for both  $V_{GS} = 12V, V_{DS} = 0V$  and  $V_{GS} = 0V, V_{DS} = 80\% BV_{DSS}$ .

**Single Event Effects (SEB, SEGR)** Note 4

TEST	SYMBOL	ENVIRONMENT (NOTE 5)		APPLIED $V_{GS}$ BIAS (V)	(NOTE 7) MAXIMUM $V_{DS}$ BIAS (V)
		(NOTE 6) TYPICAL LET (MeV/mg/cm <sup>2</sup> )	TYPICAL RANGE ( $\mu$ )		
Single Event Effects Safe Operating Area	SEESOA	37	36	-5	30
		60	32	-2	30
		60	32	-5	22.5
		82	28	0	24
		82	28	-2	22.5

NOTES:

4. Testing conducted at Brookhaven National Labs or Texas A&M.
5. Fluence = 1E5 ions/cm<sup>2</sup> (Typ), T = 25 $^\circ C$ .
6. Ion Species: LET = 37, Br or Kr; LET = 60, I or Xe; LET = 82, Au.
7. Does not exhibit Single Event Burnout (SEB) or Single Event Gate Rupture (SEGR).

**Performance Curves** Unless Otherwise Specified

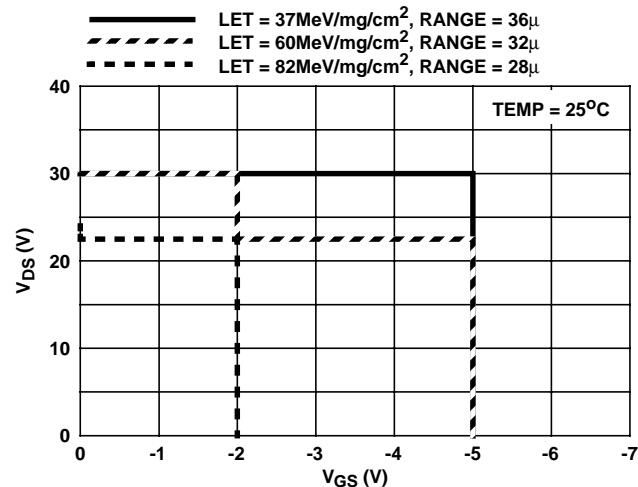


FIGURE 1. SINGLE EVENT EFFECTS SAFE OPERATING AREA

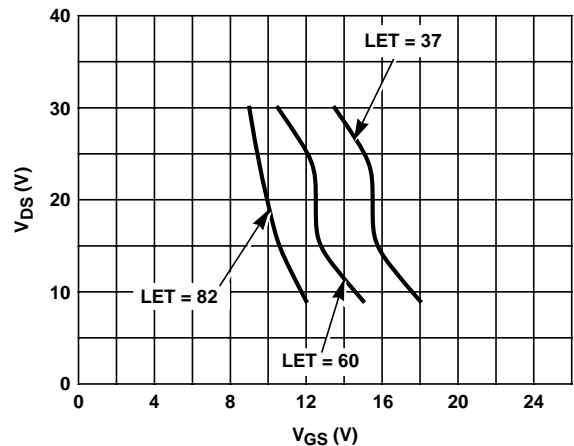


FIGURE 2. TYPICAL SEE SIGNATURE CURVE

Performance Curves Unless Otherwise Specified (Continued)

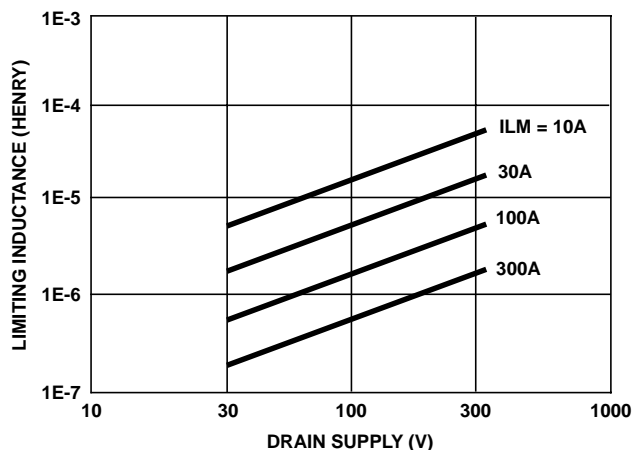


FIGURE 3. TYPICAL DRAIN INDUCTANCE REQUIRED TO LIMIT GAMMA DOT CURRENT TO  $I_{AS}$

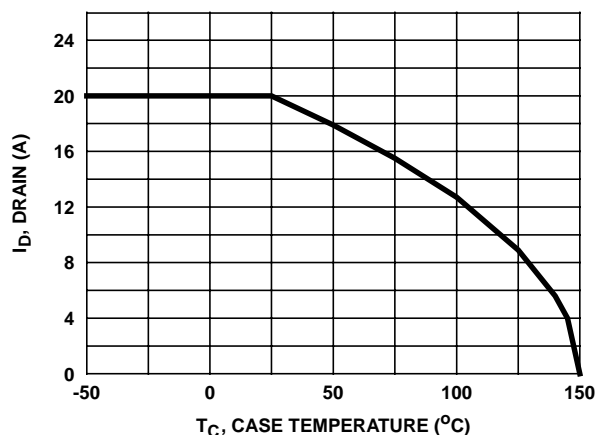


FIGURE 4. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

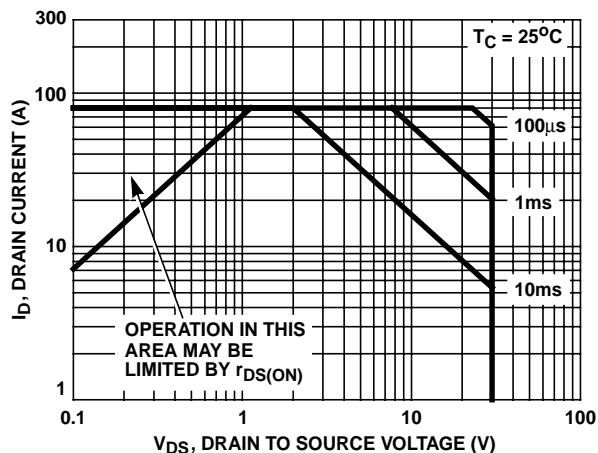


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

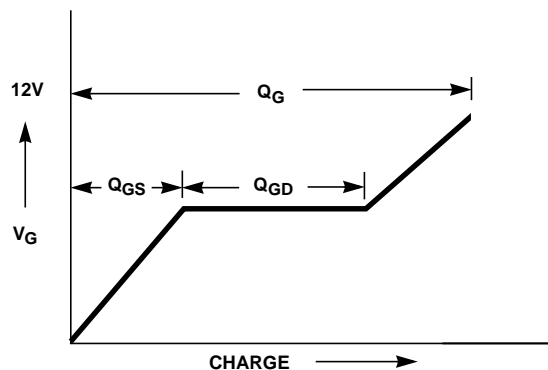


FIGURE 6. BASIC GATE CHARGE WAVEFORM

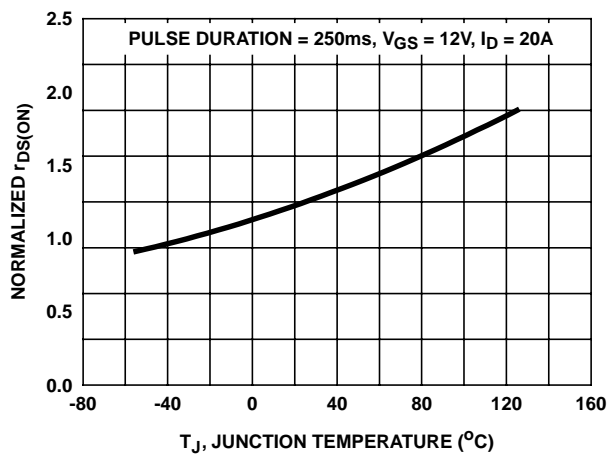


FIGURE 7. TYPICAL NORMALIZED  $r_{DS(ON)}$  vs JUNCTION TEMPERATURE

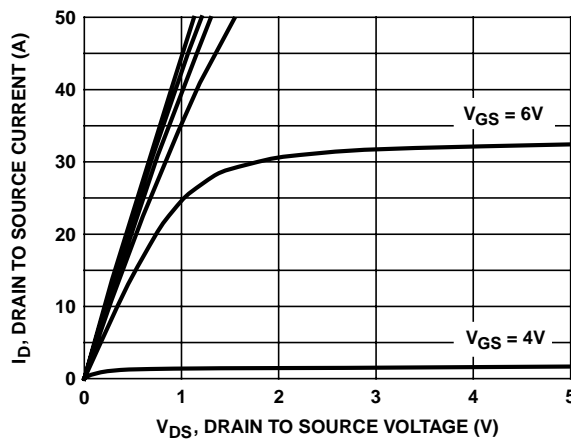


FIGURE 8. TYPICAL OUTPUT CHARACTERISTICS

Performance Curves Unless Otherwise Specified (Continued)

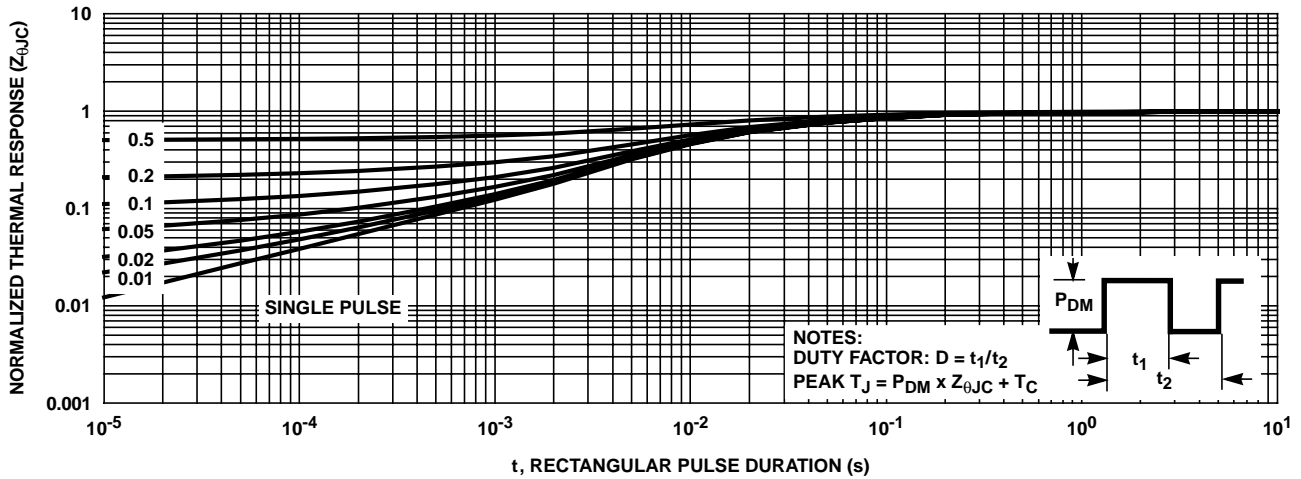


FIGURE 9. NORMALIZED MAXIMUM TRANSIENT THERMAL RESPONSE

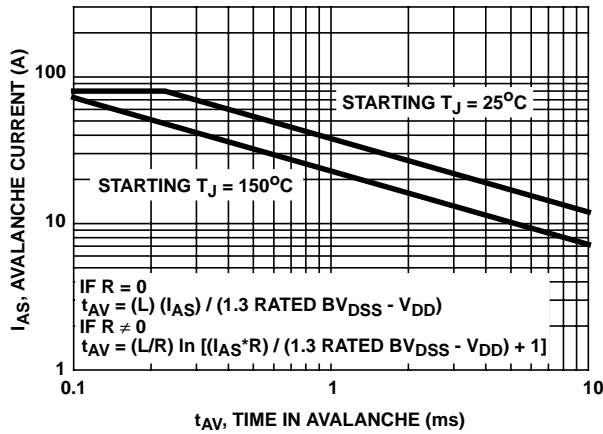


FIGURE 10. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

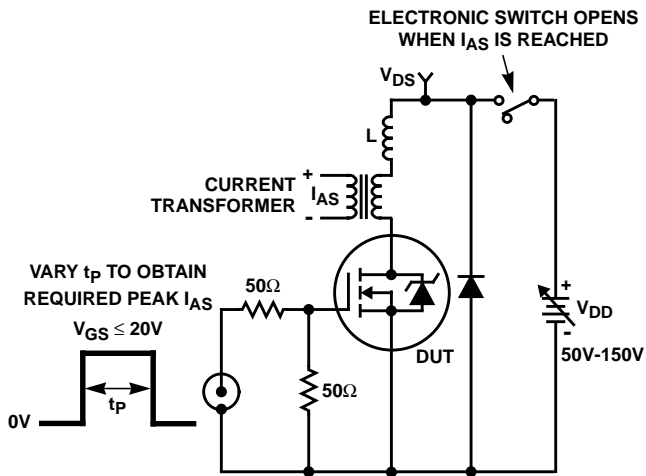


FIGURE 11. UNCLAMPED ENERGY TEST CIRCUIT

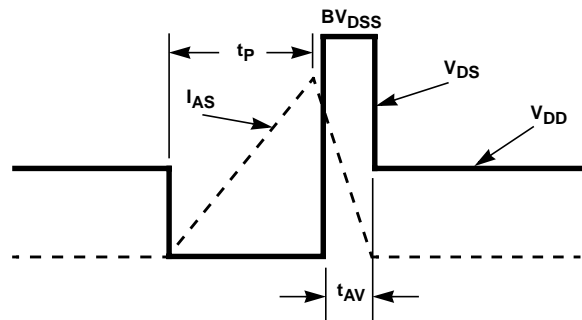


FIGURE 12. UNCLAMPED ENERGY WAVEFORMS

**Test Circuits and Waveforms** (Continued)

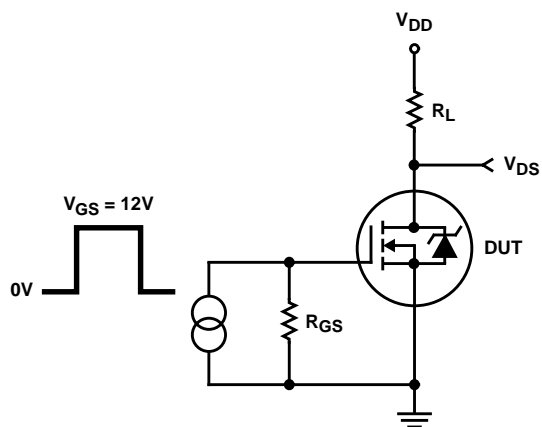


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT

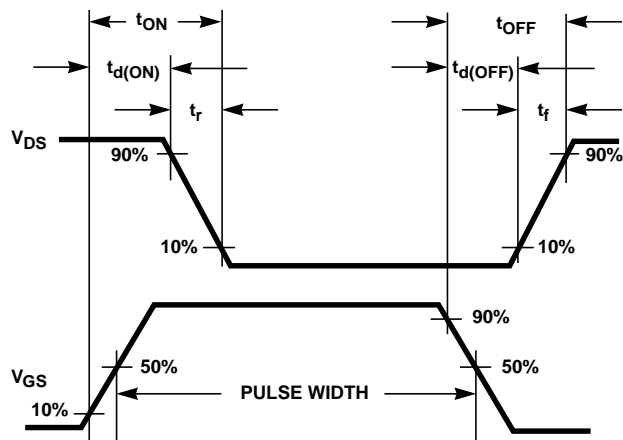


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

**Screening Information**

Screening is performed in accordance with the latest revision in effect of MIL-PRF-19500, (Screening Information Table).

**Delta Tests and Limits (JANTXV Equivalent, JANS Equivalent)  $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified**

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 24\text{V}$	$\pm 20$ (Note 7)	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\%$ Rated Value	$\pm 25$ (Note 7)	$\mu\text{A}$
Drain to Source On Resistance	$r_{DS(ON)}$	$T_C = 25^\circ\text{C}$ at Rated $I_D$	$\pm 20\%$ (Note 8)	$\Omega$
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0\text{mA}$	$\pm 20\%$ (Note 8)	V

NOTES:

- 8. Or 100% of Initial Reading (whichever is greater).
- 9. Of Initial Reading.

**Screening Information**

TEST	JANTXV EQUIVALENT	JANS EQUIVALENT
Unclamped Inductive Switching	$V_{GS(PEAK)} = 20\text{V}$ , $L = 0.1\text{mH}$ ; Limit = 70A	$V_{GS(PEAK)} = 20\text{V}$ , $L = 0.1\text{mH}$ ; Limit = 70A
Thermal Response	$t_H = 10\text{ms}$ ; $V_H = 25\text{V}$ ; $I_H = 1\text{A}$ ; LIMIT = 74mV	$t_H = 10\text{ms}$ ; $V_H = 25\text{V}$ ; $I_H = 1\text{A}$ ; LIMIT = 74mV
Gate Stress	$V_{GS} = 36\text{V}$ , $t = 250\mu\text{s}$	$V_{GS} = 36\text{V}$ , $t = 250\mu\text{s}$
Pind	Optional	Required
Pre Burn-In Tests (Note 9)	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at $25^\circ\text{C}$ )	MIL-PRF-19500 Group A, Subgroup 2 (All Static Tests at $25^\circ\text{C}$ )
Steady State Gate Bias (Gate Stress)	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$ , Time = 48 hours	MIL-PRF-750, Method 1042, Condition B $V_{GS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$ , Time = 48 hours
Interim Electrical Tests (Note 9)	All Delta Parameters Listed in the Delta Tests and Limits Table	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$ , Time = 160 hours	MIL-PRF-750, Method 1042, Condition A $V_{DS} = 80\%$ of Rated Value, $T_A = 150^\circ\text{C}$ , Time = 240 hours
PDA	10%	5%
Final Electrical Tests (Note 9)	MIL-PRF-19500, Group A, Subgroup 2	MIL-PRF-19500, Group A, Subgroups 2 and 3

NOTE:

- 10. Test limits are identical pre and post burn-in.

**Additional Tests**

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 24\text{V}$ , $t = 10\text{ms}$	6.8	A
Thermal Impedance	$\Delta V_{SD}$	$t_H = 100\text{ms}$ ; $V_H = 25\text{V}$ ; $I_H = 1\text{A}$	165	mV

**Rad Hard Data Packages - Intersil Power Transistors**

**TXV Equivalent**

**1. RAD HARD TXV EQUIVALENT - STANDARD DATA PACKAGE**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
- F. Group C - Attributes Data Sheet
- G. Group D - Attributes Data Sheet

**2. RAD HARD TXV EQUIVALENT - OPTIONAL DATA PACKAGE**

- A. Certificate of Compliance
- B. Assembly Flow Chart
- C. Preconditioning - Attributes Data Sheet
  - Pre and Post Burn-In Read and Record Data
- D. Group A - Attributes Data Sheet
- E. Group B - Attributes Data Sheet
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
  - Bond Strength Data (Subgroup B3)
  - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
- F. Group C - Attributes Data Sheet
  - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
  - Bond Strength Data (Subgroup C6)
- G. Group D - Attributes Data Sheet
  - Pre and Post RAD Read and Record Data

**Class S - Equivalents**

**1. RAD HARD "S" EQUIVALENT - STANDARD DATA PACKAGE**

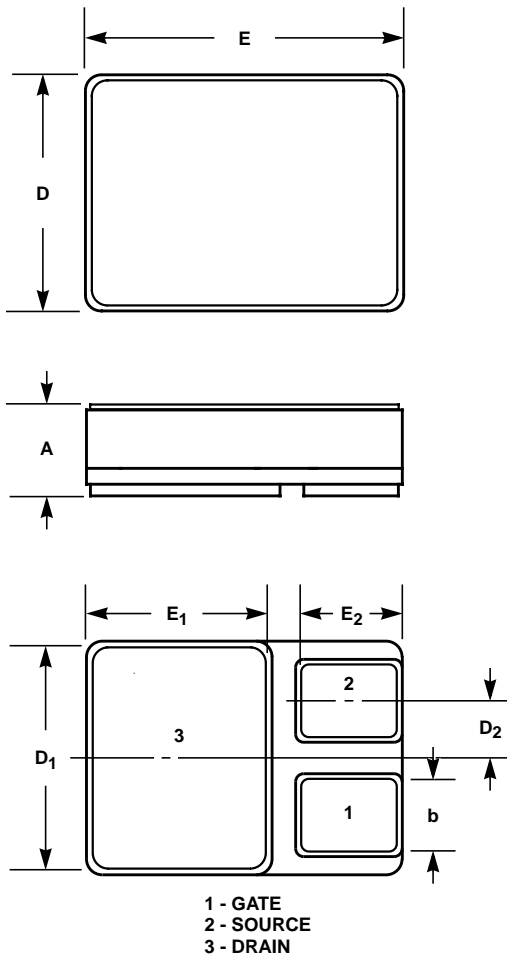
- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
- F. Group A - Attributes Data Sheet
- G. Group B - Attributes Data Sheet
- H. Group C - Attributes Data Sheet
- I. Group D - Attributes Data Sheet

**2. RAD HARD MAX. "S" EQUIVALENT - OPTIONAL DATA PACKAGE**

- A. Certificate of Compliance
- B. Serialization Records
- C. Assembly Flow Chart
- D. SEM Photos and Report
- E. Preconditioning - Attributes Data Sheet
  - HTRB - Hi Temp Gate Stress Post Reverse Bias Data and Delta Data
  - HTRB - Hi Temp Drain Stress Post Reverse Bias Delta Data
  - X-Ray and X-Ray Report
- F. Group A - Attributes Data Sheet
  - Subgroups A2, A3, A4, A5 and A7 Data
- G. Group B - Attributes Data Sheet
  - Subgroups B1, B3, B4, B5 and B6 Data
- H. Group C - Attributes Data Sheet
  - Subgroups C1, C2, C3 and C6 Data
- I. Group D - Attributes Data Sheet
  - Pre and Post Radiation Data

**SMD.5**

**3 PAD CERAMIC LEADLESS CHIP CARRIER**



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.112	0.124	2.84	3.15	3
b	0.090	0.100	2.28	2.54	-
D	0.291	0.301	7.39	7.64	-
D <sub>1</sub>	0.281	0.291	7.13	7.39	-
D <sub>2</sub>	0.070	0.080	1.78	2.03	-
E	0.395	0.405	10.03	10.28	-
E <sub>1</sub>	0.220	0.230	5.58	5.84	-
E <sub>2</sub>	0.115	0.125	2.92	3.17	-

NOTES:

1. No current JEDEC outline for this package.
2. Controlling dimension: Inch.
3. Measurement prior to pre-solder coating the mounting pads.
4. Revision 4 dated 5-00.

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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**Sales Office Headquarters**

**NORTH AMERICA**

Intersil Corporation  
P. O. Box 883, Mail Stop 53-204  
Melbourne, FL 32902  
TEL: (321) 724-7000  
FAX: (321) 724-7240

**EUROPE**

Intersil SA  
Mercure Center  
100, Rue de la Fusee  
1130 Brussels, Belgium  
TEL: (32) 2.724.2111  
FAX: (32) 2.724.22.05

**ASIA**

Intersil Ltd.  
8F-2, 96, Sec. 1, Chien-kuo North,  
Taipei, Taiwan 104  
Republic of China  
TEL: 886-2-2515-8508  
FAX: 886-2-2515-8369