CY7C1062AV25

512K x 32 Static RAM

Features

- **High speed**
  - **— t_{AA} = 10 ns**
- **Low active power**
  - **— 745 mW (max.)**
- **Operating voltages of 2.5 ± 0.2V**
- **1.5V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ features**
- **Available in non Pb-free 119-ball pitch ball grid array package**

Functional Description

The CY7C1062AV25 is a high-performance CMOS Static RAM organized as 524,288 words by 32 bits.

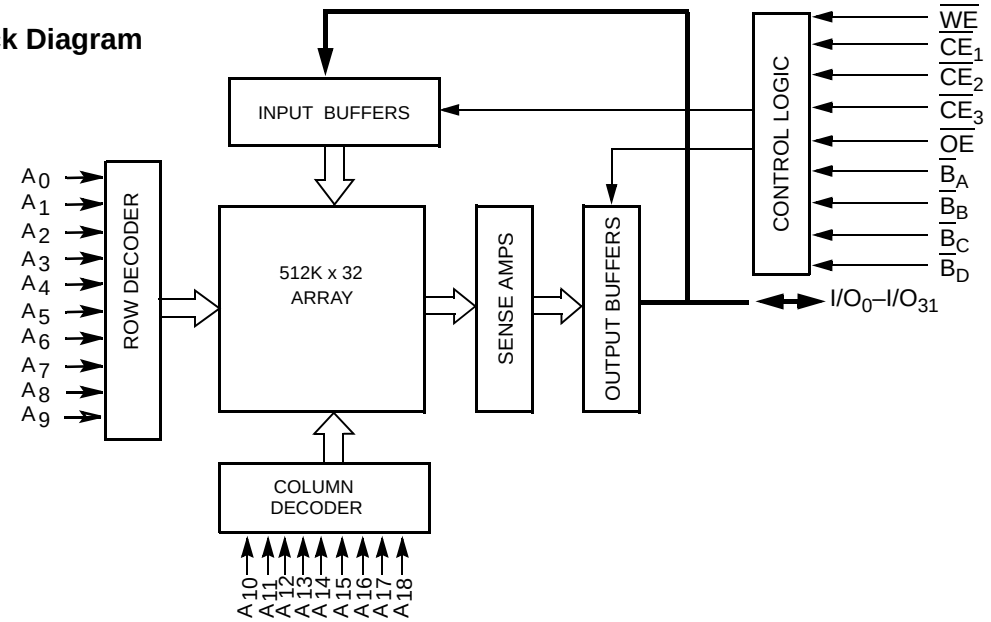
Writing to the device is accomplished by enabling the chip ($\overline{CE}_1$, CE_2 and $\overline{CE}_3$ LOW) and forcing the Write Enable ($\overline{WE}$) input LOW. If Byte Enable A ($\overline{B}_A$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte Enable B ($\overline{B}_B$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}). Likewise, $\overline{B}_C$ and $\overline{B}_D$ correspond with the I/O pins I/O_{16} to I/O_{23} and I/O_{24} to I/O_{31}, respectively.

Reading from the device is accomplished by enabling the chip ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$ LOW) while forcing the Output Enable ($\overline{OE}$) LOW and Write Enable ($\overline{WE}$) HIGH. If the first Byte Enable ($\overline{B}_A$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte Enable B ($\overline{B}_B$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. Similarly, $\overline{B}_c$ and $\overline{B}_D$ correspond to the third and fourth bytes. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{31}) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$, CE_2or $\overline{CE}_3$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the byte selects are disabled ($\overline{B}_{A\text{-}D}$ HIGH), or during a write operation ($\overline{CE}_1$, CE_2, and $\overline{CE}_3$ LOW, and $\overline{WE}$ LOW).

The CY7C1062AV25 is available in a 119-ball pitch ball grid array (PBGA) package.

Logic Block Diagram



Selection Guide

		–10	Unit
Maximum Access Time		10	ns
Maximum Operating Current	Com'l/Ind'l	275	mA
Maximum CMOS Standby Current	Com'l/Ind'l	50	mA

Pin Configuration

119-ball PBGA
(Top View)

	1	2	3	4	5	6	7
A	I/O_{16}	A	A	A	A	A	I/O_0
B	I/O_{17}	A	A	$\overline{CE_1}$	A	A	I/O_1
C	I/O_{18}	$\overline{B_c}$	$\overline{CE_2}$	NC	$\overline{CE_3}$	$\overline{B_a}$	I/O_2
D	I/O_{19}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_3
E	I/O_{20}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_4
F	I/O_{21}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_5
G	I/O_{22}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_6
H	I/O_{23}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_7
J	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	DNU
K	I/O_{24}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_8
L	I/O_{25}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_9
M	I/O_{26}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{10}
N	I/O_{27}	V_{SS}	V_{DD}	V_{SS}	V_{DD}	V_{SS}	I/O_{11}
P	I/O_{28}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	I/O_{12}
R	I/O_{29}	A	$\overline{B_d}$	NC	$\overline{B_b}$	A	I/O_{13}
T	I/O_{30}	A	A	$\overline{WE}$	A	A	I/O_{14}
U	I/O_{31}	A	A	$\overline{OE}$	A	A	I/O_{15}

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND[1] .... –0.5V to +3.6V

DC Voltage Applied to Outputs in High-Z State[1] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[1]..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.5V ± 0.2V
Industrial	–40°C to +85°C	

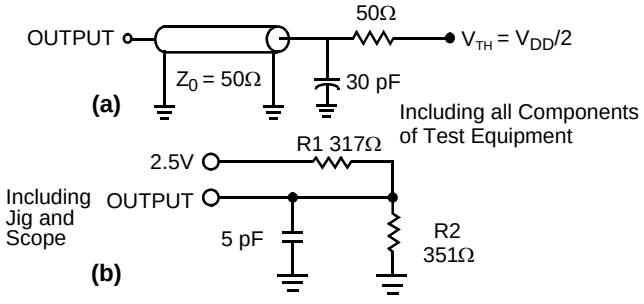
DC Electrical Characteristics Over the Operating Range

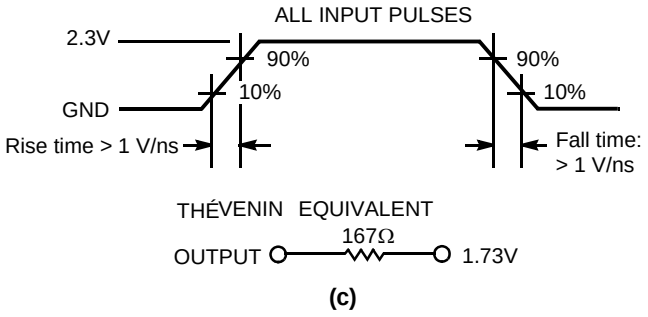
Parameter	Description	Test Conditions		–10 Min.	–10 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 1.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l/Ind'l		275	mA
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}	Com'l/Ind'l		100	mA
I_{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com'l/Ind'l		50	mA

Capacitance[2]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 2.5V	8	pF
C_{OUT}	I/O Capacitance		10	pF

AC Test Loads and Waveforms[3]





Notes:

1. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
2. Tested initially and after any design or process changes that may affect these parameters.
3. Valid SRAM operation does not occur until the power supplies have reached the minimum operating V_{DD} (2.3V). As soon as 1ms (T_{power}) after reaching the minimum operating V_{DD}, normal SRAM operation can begin including reduction in V_{DD} to the data retention (V_{CCDR}, 1.5V) voltage.

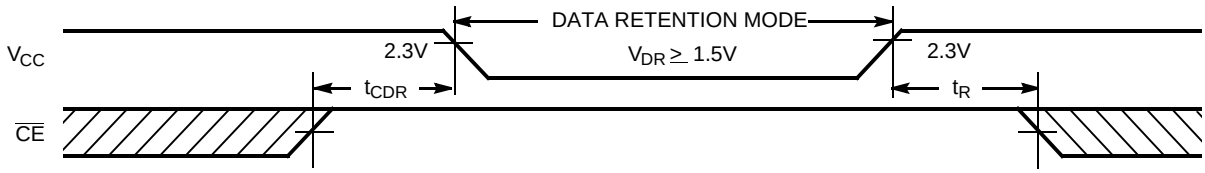
AC Switching Characteristics Over the Operating Range[4]

Parameter	Description	–10		Unit
		Min.	Max.	
Read Cycle				
t_{power}	V_{CC} (typical) to the first access[5]	1		ms
t_{RC}	Read Cycle Time	10		ns
t_{AA}	Address to Data Valid		10	ns
t_{OHA}	Data Hold from Address Change	3		ns
t_{ACE}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Data Valid		10	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[6]	1		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6]		5	ns
t_{LZCE}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Low-Z[6]	3		ns
t_{HZCE}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to High-Z[6]		5	ns
t_{PU}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Power-up[7]	0		ns
t_{PD}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ HIGH to Power-down[7]		10	ns
t_{DBE}	Byte Enable to Data Valid		5	ns
t_{LZBE}	Byte Enable to Low-Z[6]	1		ns
t_{HZBE}	Byte Disable to High-Z[6]		5	ns
Write Cycle[8, 9]				
t_{WC}	Write Cycle Time	10		ns
t_{SCE}	$\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ LOW to Write End	7		ns
t_{AW}	Address Set-up to Write End	7		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		ns
t_{SD}	Data Set-up to Write End	5.5		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6]		5	ns
t_{BW}	Byte Enable to End of Write	7		ns

Notes:

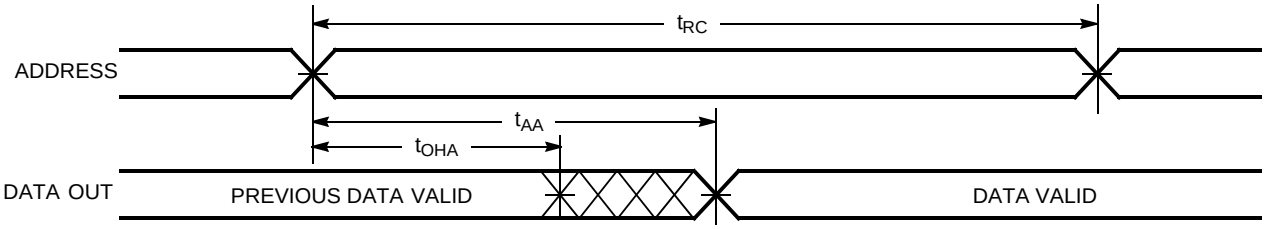
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.1V, input pulse levels of 0 to 2.3V, and output loading of the specified I_{OL}/I_{OH} and transmission line loads. Test conditions for the read cycle use output loading as shown in (a) of AC Test Loads, unless specified otherwise.
5. This part has a voltage regulator that steps down the voltage from 2.3V to 2V internally. t_{power} time has to be provided initially before a read/write operation is started.
6. t_{HZOE}, t_{HZCE}, t_{HZWE}, t_{HZBE}, and t_{LZOE}, t_{LZCE}, t_{LZWE}, and t_{LZBE} are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
7. These parameters are guaranteed by design and are not tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$1 LOW, $\overline{CE}$ 2 HIGH, $\overline{CE}$3 LOW, and $\overline{WE}$ LOW. The chip enables must be active and $\overline{WE}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Data Retention Waveform

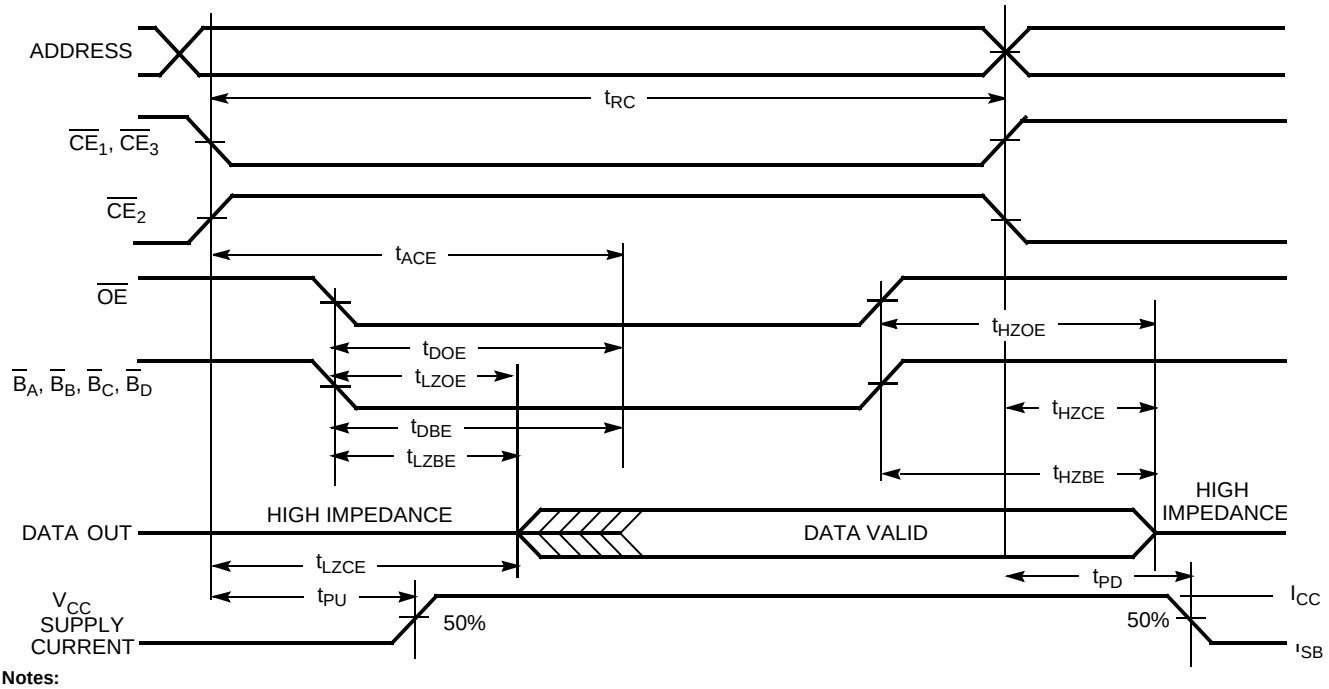


Switching Waveforms

Read Cycle No. 1[11,12]



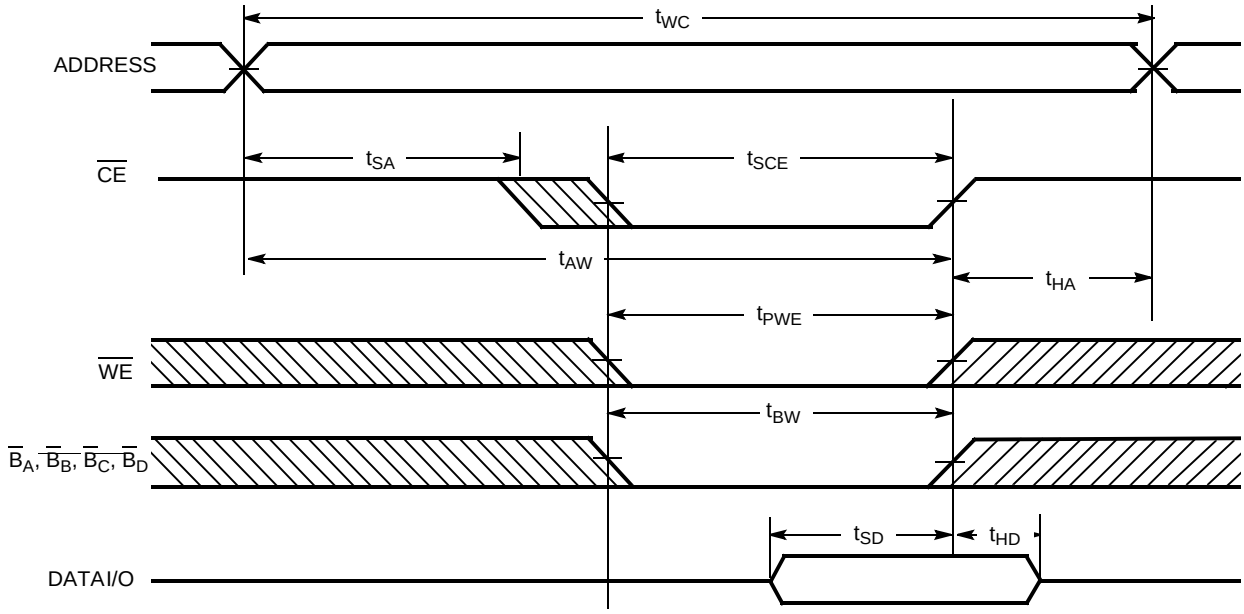
Read Cycle No. 2 ($\overline{OE}$ Controlled)[11,13]



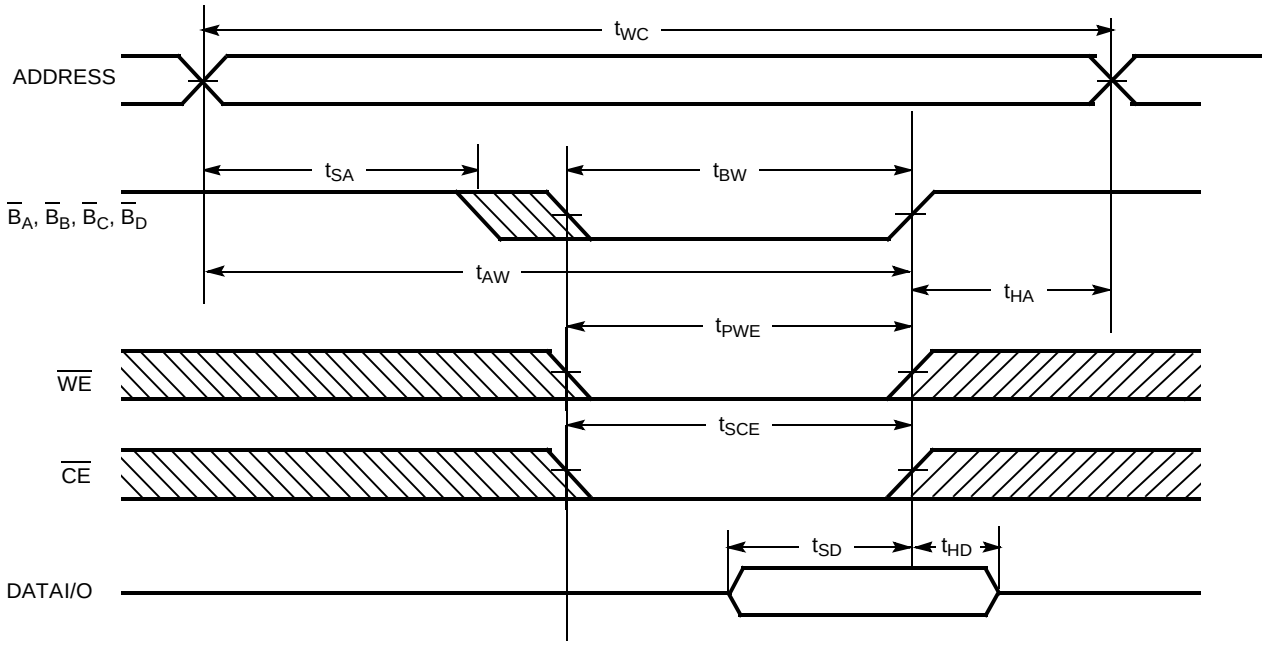
Notes:
10. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs
11. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$, $\overline{B}_D$= V_{IL}.
12. $\overline{WE}$ is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms

Write Cycle No. 1 ($\overline{CE}$ Controlled)[14,15,16]



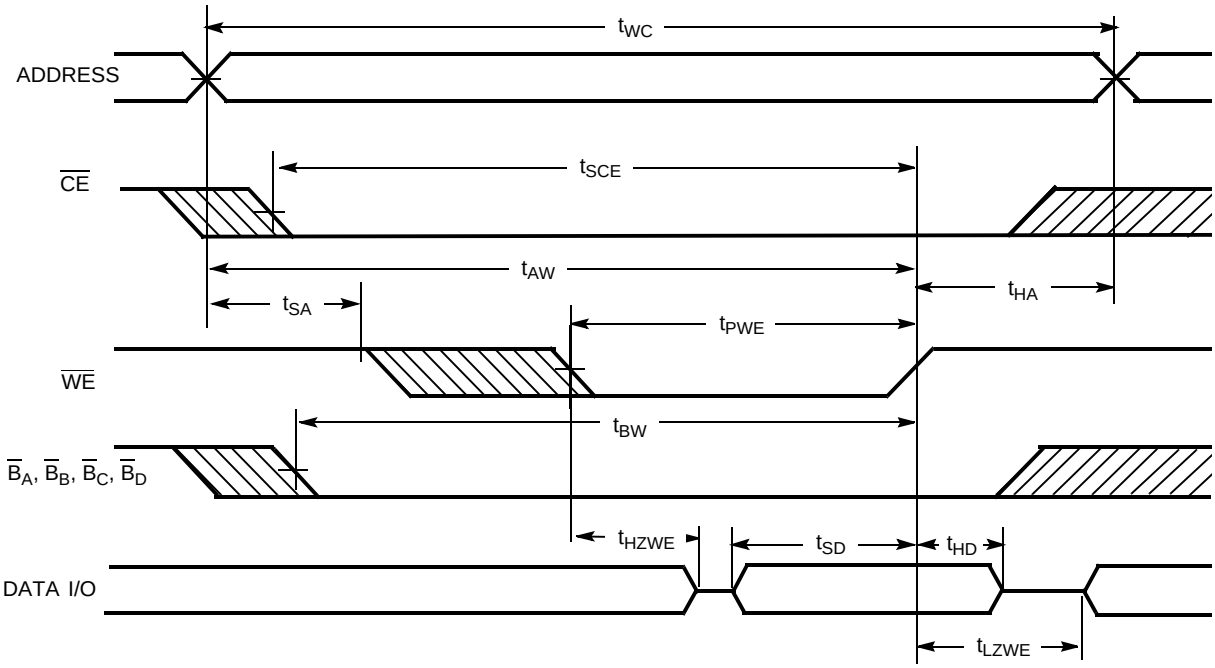
Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)[14,15,16]



Notes:
14. $\overline{CE}$ indicates a combination of all three chip enables. When ACTIVE LOW, $\overline{CE}$ indicates the $\overline{CE_1}$, $\overline{CE_2}$ and $\overline{CE_3}$ are LOW.
15. Data I/O is high-impedance if $\overline{OE}$ or $\overline{B_A}$, $\overline{B_B}$, $\overline{B_C}$, $\overline{B_D}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

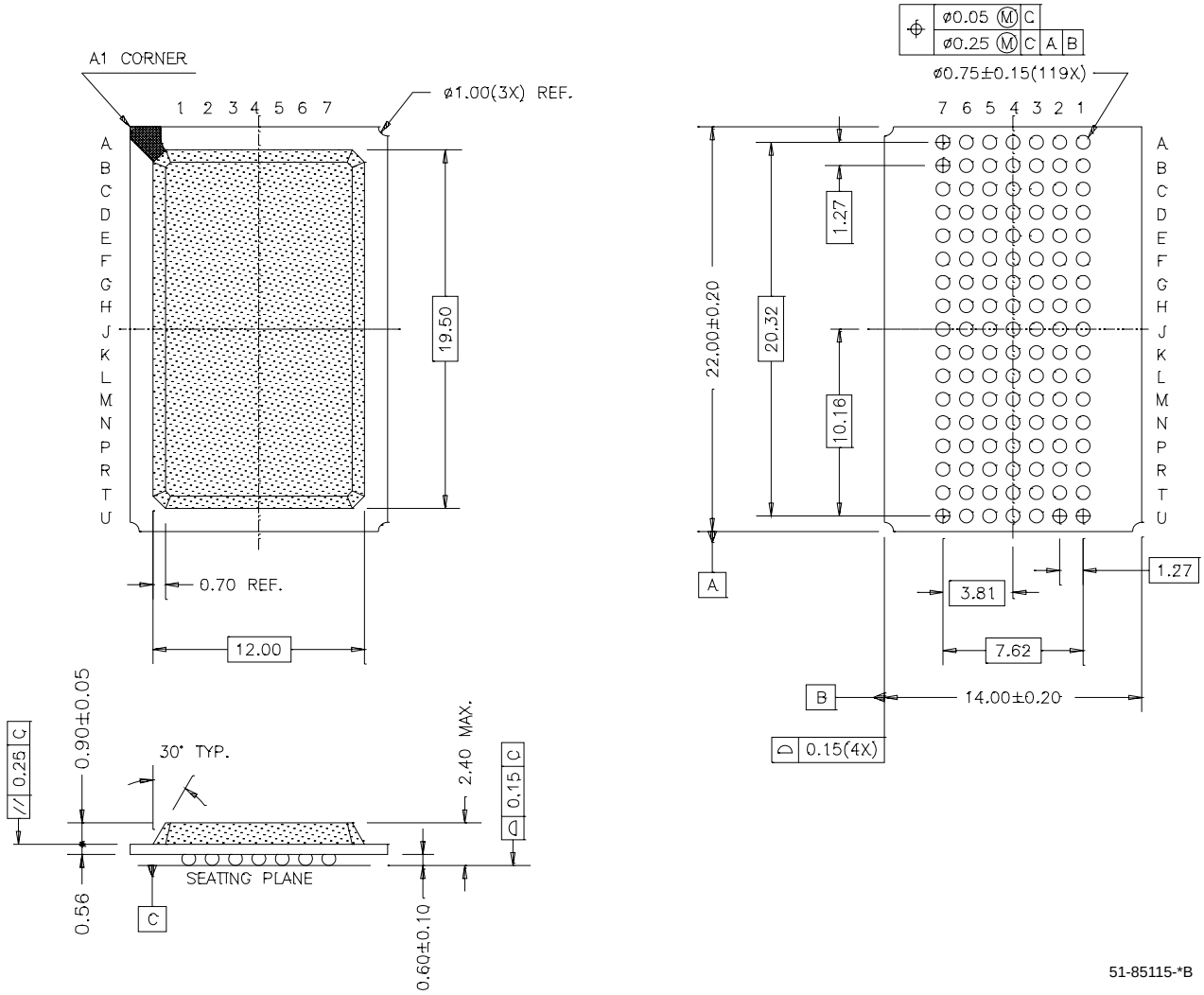
$\overline{CE_1}$	$\overline{CE_2}$	$\overline{CE_3}$	$\overline{OE}$	$\overline{WE}$	$\overline{B_A}$	$\overline{B_B}$	$\overline{B_C}$	$\overline{B_D}$	I/O_0–I/O_7	I/O_8–I/O_{15}	I/O_{16}–I/O_{23}	I/O_{24}–I/O_{31}	Mode	Power
H	H	H	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	H	L	X	X	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Power Down	(I_{SB})
L	L	L	L	H	L	L	L	L	Data Out	Data Out	Data Out	Data Out	Read All Bits	(I_{CC})
L	L	L	L	H	L	H	H	H	Data Out	High-Z	High-Z	High-Z	Read Byte A Bits Only	(I_{CC})
L	L	L	L	H	H	L	H	H	High-Z	Data Out	High-Z	High-Z	Read Byte B Bits Only	(I_{CC})
L	L	L	L	H	H	H	L	H	High-Z	High-Z	Data Out	High-Z	Read Byte C Bits Only	(I_{CC})
L	L	L	L	H	H	H	H	L	High-Z	High-Z	High-Z	Data Out	Read Byte D Bits Only	(I_{CC})
L	L	L	X	L	L	L	L	L	Data In	Data In	Data In	Data In	Write All Bits	(I_{CC})
L	L	L	X	L	L	H	H	H	Data In	High-Z	High-Z	High-Z	Write Byte A Bits Only	(I_{CC})
L	L	L	X	L	H	L	H	H	High-Z	Data In	High-Z	High-Z	Write Byte B Bits Only	(I_{CC})
L	L	L	X	L	H	H	L	H	High-Z	High-Z	Data In	High-Z	Write Byte C Bits Only	(I_{CC})
L	L	L	X	L	H	H	H	L	High-Z	High-Z	High-Z	Data In	Write Byte D Bits Only	(I_{CC})
L	L	L	H	H	X	X	X	X	High-Z	High-Z	High-Z	High-Z	Selected, Outputs Disabled	(I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1062AV25-10BGC	51-85115	119-ball Plastic Ball Grid Array (14 x 22 x 2.4 mm)	Commercial
	CY7C1062AV25-10BGI			Industrial

Package Diagram

119-ball PBGA (14 x 22 x 2.4 mm) (51-85115)



Document History Page

Document Title: CY7C1062AV25 512K x 32 Static RAM Document Number: 38-05333				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	119626	01/29/03	DFP	New Data Sheet
*A	493565	See ECN	NXR	Converted from Preliminary to Final Removed -8 and -10 speed bins Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the ordering information table