Product Brief

C-5e NETWORK PROCESSOR

MOTOROLA
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Freescale Semiconductor, Inc.

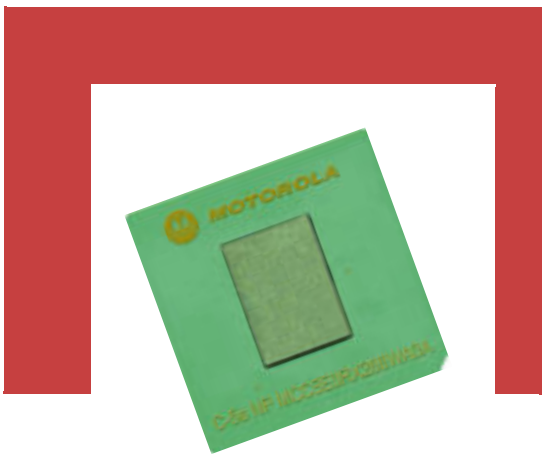
FEATURES

- *Operating frequency of 266MHz with power consumption of 9W at 1.2V typical*
- *5Gbps of bandwidth for nonblocking throughput with over 4,500 MIPs of computing power*
- *17 programmable RISC Cores for cell/packet forwarding and 32 programmable Serial Data Processors for processing bit streams*
- *On-chip classification coprocessor supporting over 46 million IPv4 lookups/second*
- *Flexible interfaces supporting virtually any serial or parallel protocol and individual port data rate from DS1 to OC-48c/STM-16*
- *External C-Port traffic manager for fine-grained QoS*
- *Simple and efficient programming in C-language with robust APIs*
- *Royalty-free reference applications*
- *Key alliances in fabrics, coprocessors, network software, and design services*

The **C-5e™ network processor (NP)**, Motorola's second generation network processor in the C-Port family, is the most integrated, flexible, and functionally-rich processor for developing and deploying advanced services for next-generation networks. With its 5Gbps of bandwidth and more than 4500 MIPs of computing power, the C-5e NP more than satisfies the demanding communications requirements for intelligent network services, such as classification, traffic management, and interworking functions.

The C-5e NP is compatible with Motorola's Traffic Management Coprocessors (TMCs) to provide unprecedented Quality of Service (QoS) capabilities. What's more, Motorola's M-5™ Channel Adapter can extend the C-5e NP's data bandwidth reach to support full-duplex OC-48c/STM-16 and channelized applications, enabling high-speed network services.

The C-5e NP also integrates robust programming interfaces, a comprehensive development environment, and third-party support from Motorola's Smart Networks Alliance to provide a platform approach that can simplify and speed the development of full-featured networking applications today, enable faster development within and across product families, and provide a smooth migration path to future product generations.



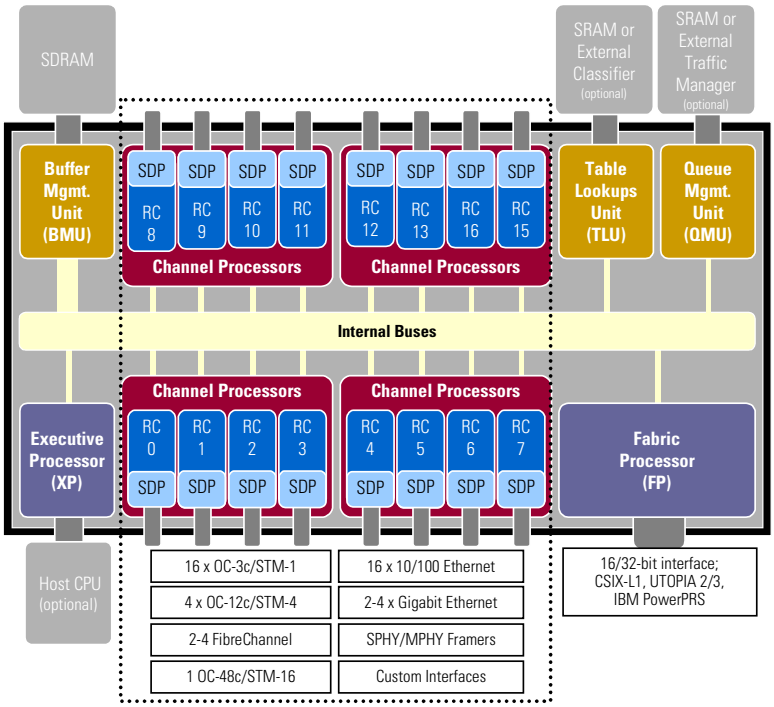
SOFTWARE-OPTIMIZED NPU ARCHITECTURE

The C-5e NP was designed from the ground up to provide a simple and robust programming model. It enables complete programmability of forwarding plane tasks in C-language using Applications Programming Interfaces (APIs). To support this programming model, the interactions among subsystems of the architecture are very efficient with integrated coprocessor acceleration for common tasks such as classification, traffic management, buffer management, fabric interfacing, and supervisory processing.

Traffic typically enters the C-5e NP through its 16 Channel Processors (CPs), each of which can accommodate up to an OC-3's worth of bandwidth. Each CP contains a transmit and receive Serial Data Processor (SDP), which operates like a VLIW engine, and a RISC Core that is used for any application-specific purpose.

The SDPs control programmable external pin logic, allowing them to implement a wide variety of Layer 1 interfaces including connection to T/E-Carrier framers, 10/100 Ethernet PHY (RMII), Gigabit Ethernet PHY (GMII or TBI), OC-3/STM-1 PHY, OC-12/STM-4 PHY, and the M-5 Channel Adapter, a Utopia 3/PoS PHY interface that can support OC-48/OC-48c/STM-16 MPHY capabilities. Ethernet MACs and SONET framers are embedded in the SDP architecture.

At Layer 2, the SDPs can be independently configured to support Ethernet, Packet over SONET (PoS), HDLC streams, ATM, Frame Relay, FibreChannel, or virtually any format, including MPLS and other encapsulations.



C-5e NP high functional integration provides design and programming efficiencies

The programmability of the SDPs supports the diversity of media access control (MAC) interfaces, as well as data parsing requirements, and can support different protocol implementations on a port-by-port basis.

The RISC Cores, programmed in C-language, are dedicated to the advanced services that benefit the most from high-level language implementations. For example, the RISC Cores focus on higher-level forwarding tasks such as final forwarding decision making, scheduling, and statistics gathering. The RISC Cores are also responsible for maintaining the context of the on-chip operations to ensure efficient delivery of traffic to the egress ports with appropriate service levels applied.

The C-5e NP's CPs can each be assigned to a physical interface (up to 16 OC-3's worth), aggregated together in parallel clusters to support higher-bandwidth I/O streams, or assigned internally as dedicated internal coprocessors. When used for additional processing, the CPs are linked for pipelined processing on a single data stream. This allows processing power to be applied independently of data rate.

POWERFUL TRAFFIC CLASSIFICATION

The C-5e NP's fully integrated Table Lookup Unit (TLU) is a high-speed, flexible classification engine that enables a wide range of traffic classification functions and supports multiple, different search algorithms — all while providing the lookup performance that more than supports OC-48c/STM-16 class applications. For example, the TLU can achieve more than 46 million IPv4 lookups per second due to its extensively pipelined architecture. Typical lookups that the TLU supports include IPv4/IPv6 Longest Prefix Match, ATM VCI/VPIs, Ethernet MAC/VLANs, and Multiprotocol Label Switching (MPLS), among others. In addition to the table lookups, the TLU can be configured to do integrated real-time statistics counting.

The TLU is connected to 64bit, 133MHz ZBT SRAM. This same interface can be used for connecting to an external classification coprocessors in the rare case that you need more extensive classification capabilities. In this case, the TLU acts as a proxy to the external coprocessor.

ADVANCED QUALITY OF SERVICE MANAGEMENT

The C-5e NP's Queue Management Unit (QMU), when in internal mode, can support up to 512 queues to satisfy the traffic management requirements of many applications. However, when the C-5e NP, using the QMU's external mode, is gluelessly coupled to a Motorola's Traffic Management Coprocessor (TMC), you can achieve a powerful QoS management solution, including support for both ATM and IP applications.

For more information about Motorola traffic managers, see the *Q-5 Traffic Management Coprocessor Product Brief*.

SCALABLE BANDWIDTH WITH THIRD PARTY FABRICS

By connecting multiple C-5e NPs through their fabric interfaces to a fabric switch, you can achieve Terabits per second of aggregate bandwidth. The C-5e NP's Fabric Processor (FP) is highly configurable, enabling you to implement a wide array of fabric parameters (such as cell size and self-routing headers), per-flow congestion control, segmentation and re-assembly (SARing), and integrated scheduling of up to 128 queues.

The FP can operate at 125MHz, 64bits (32bit Transmit / 32bit Receive) and support a bandwidth of up to 3.2 Gbps full duplex. It supports a wide range of the most standard interfaces, including Utopia 2, Utopia 3, and 32bit, 125MHz CSIX-L1, plus IBM PowerPRS and proprietary fabrics.

C-5e NETWORK PROCESSOR PRODUCT HIGHLIGHTS

Electrical	Power Consumption	9W@266MHz, 1.2V Typical, 13W@266MHz, 1.26V Maximum
	Frequency	266MHz Typical Core Clock
Processing	Throughput	5Gbps aggregate
	Internal Bandwidth	Three internal buses with over 75Gbps aggregate bandwidth
	Processing Power	Over 4,500 MIPS
Physical Interfaces, supported with Serial Data Processors	Ethernet (embedded 10/100 and Gigabit Ethernet MACs)	10Mb Ethernet (RMII); 100Mb Ethernet (RMII); 1Gb Ethernet (GMII and TBI)
	SONET (embedded OC-3 and OC-12 Framers)	OC-3c/STM-1; OC-12/OC-12c/STM-4; OC-48/OC-48c/STM-16 (using C-5e and M-5 system); OC-48 MPHY (using C-5e and M-5 system)
	Other	T1/E1 and T3/E3 (with external framers/multiplexors); 1Gb FibreChannel
Physical Layout	Single Chip System	840 pins (595 active, 245 power) HiTCE Ceramic Ball Grid Array (BGA) package
Environmental	Operating Temperature, Ambient	-40° to +85°C
	Junction Temperature	-40° to +125°C
16 Channel Processors (CPs), for physical interface connection and cell/packet processing	RISC Core	• One RISC Core per each Channel Processor • 32bit C programmable, standard instruction set
	Serial Data Processors (SDPs)	• Two SDPs (one receive and one transmit) per each Channel Processor • Microcode programmable using C function call syntax
	IMEM/DMEM (per cluster)	32kBytes/48kBytes
Executive Processor (XP), for supervisory tasks and management of host processor	RISC Core	C programmable, standard instruction set
	External Interfaces	32bit, 33/66MHz PCI, serial PROM interface. two-wire serial bus interface (400kbps)
	IMEM/DMEM	48kBytes/32kBytes
Fabric Processor (FP), for high-speed fabric interface management	External Interfaces	Utopia-1, -2 and -3, CSIX-L1, IBM PowerPRS
	Interface Bandwidth	Transmit and receive full-duplex at up to 4000 Mbps in each direction
Table Lookup Unit (TLU), for networking lookups/classification	Number of Lookups per Second	Example benchmarks: • 133 million Index lookups/seconds • 46 million IPv4 lookups/seconds
	Table Size/Number	16 Million entries maximum with up to 32 unique tables supported
	Table Types Supported	Hash, Trie, Key, Data, Indexed Pointer, Longest Prefix Match, Chained Index, and Chained Hash
	External Memory Size	Up to 128MB SRAM — with option for external classifier
Queue Management Unit (QMU), for queue control/traffic management	Internal Mode	• Up to 512 queues • Up to 16,384 descriptors • Automated multicast elaboration
	External mode	See the Traffic Management Coprocessor product brief/documentation
Buffer Management Unit (BMU), for payload storage	Buffer Memory Width	139bit (128 bits data, 9 bits ECC, 2 bits control)
	Buffer Memory Size	Up to 128MB SDRAM
Buses, internal	Payload Bus	54.5Gbps bandwidth, 128bits bus width, 64Bytes transfer size
	Ring Bus	17.2Gbps bandwidth, 64bits bus width, 8Byte to 32Bytes transfer size
	Global Bus	3.4Gbps bandwidth, 32bits bus width, 4Bytes transfer size

For more information about Motorola's network processor solutions, please contact your local Motorola sales representative or call (800) 521-6274. You can also visit Motorola's Smart Networks Web site at:

www.motorola.com/networkprocessors

DRAMATICALLY IMPROVING DEVELOPMENT PRODUCTIVITY

The C-5e NP is programmed using standard C-language rather than configurable state-machines or proprietary languages, thus providing a true and simple programming model. In addition, the C-5e NP's standard RISC instruction set enhances code portability and enables use of standard development tools. Although there are 16 CPs per C-5e NP, each CP is independently programmable, avoiding the limitations typical of traditional symmetric multi-processor designs. With the flexibility provided by the CP architectures, it is a straight-forward task to write software for the CP to perform a given function.

The key to a simple programming model and more productivity, however, is a set of robust programming interfaces. C-Ware Applications Programming Interfaces (C-Ware APIs) simplify communications software development and efficiently leverage the power of the C-5e NP and Q-5 TMC. Similar to APIs in the computing world, the C-Ware APIs abstract the underlying hardware architecture of the C-5e NP and Q-5 TMC and support the most common network task building blocks, such as physical interface management, data forwarding, table lookups, buffer management, queuing operations, and so on. Programming to the C-Ware APIs ensures software compatibility and scalability from generation to generation of the C-Port family of network processors.

The programming task is significantly enhanced by the comprehensive C-Port family development environment that consists of the following components:

- **C-Ware Applications Library (CAL)** — Comprehensive set of reference applications for building networking systems based on Motorola's C-Port network processor family. The CAL significantly accelerates customer software development by providing extensive reference source code that is instrumented for and tested with the C-Ware Software Toolset (CST). Wireless Network Interface (WNI) product applications are included in the CAL.
- **C-Ware Software Toolset (CST)** — Functional and performance accurate simulation environment, standard GNU-based compiler and debugger, GUI performance analysis tool, traffic scripting tools, and comprehensive C-Ware APIs.
- **C-Ware Development System (CDS)** — Compact PCI chassis with Motorola MPC750 Host Application Module, which can also include Network Processor Switch Modules, TMC Daughter Cards, and various Physical Interface Modules (PIMS). Complete hardware reference designs are also available.

C5ENP-PB/D
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Freescale Semiconductor, Inc.