LinkSwitch®
Design Guide
Application Note AN-35

Introduction

Integrated switching power supply technology, offering small size, low weight and universal AC input voltage operation, has finally evolved to cost-effectively replace linear transformer-based power supplies for low power applications. *LinkSwitch* reduces the cost of switching battery chargers and AC adapters to the level of linear transformer power supplies. *LinkSwitch* also easily meets standby and no-load energy consumption guidelines specified by worldwide regulatory programs such as the USA's Presidential 1 W Standby Executive Order and the European Commission's 2005 requirement for 300 mW no-load consumption.

The feature set of *LinkSwitch* offers the following advantages over other solutions:

- Lowest cost and component count for a constant voltage, constant current (CV/CC) solution
- Extremely simple circuit – only 14 components required for a production-worthy design
- Primary based CV/CC solution eliminates 10 to 20 components for low system cost
- Up to 75% lighter power supply reduces shipping costs
- Fully integrated auto-restart for short circuit and open loop fault protection
- 42 kHz operation simplifies EMI filter design
- 3 W output with EE13 core for low cost and small size

LinkSwitch is designed to produce an approximate CV/CC output characteristic as shown in Figure 2. In charger applications, a discharged battery operates on the CC portion of the curve until almost fully charged and then naturally transitions to the CV portion of the curve. Below an output voltage of approximately 2 V (consistent with a failed battery pack), the supply enters auto-restart, reducing the average output current to approximately 8% of nominal.

In an AC adapter, normal operation occurs only on the CV portion of the curve, the CC portion providing overload protection and auto-restart short circuit protection.

LinkSwitch is a fixed frequency PWM controlled device, designed to operate with flyback converters in discontinuous mode. In the CV portion of the curve, the device operates using voltage mode control and changes to a current limit mode during the CC portion of the curve. Total system CV accuracy is typically ±10% at the peak power point, including all device tolerances and line input voltage variations. With transformer primary inductance variations within ±10%, the total system CC accuracy is typically ±20% (LNK501) or ±25% (LNK500) compared to nominal values.

During CV operation, the reflected output voltage (V_{OR}) controls the duty cycle. *LinkSwitch* is placed in the high side rail, as shown in Figure 1, such that V_{OR} can be sensed directly, requiring no additional subtraction of the input voltage component.

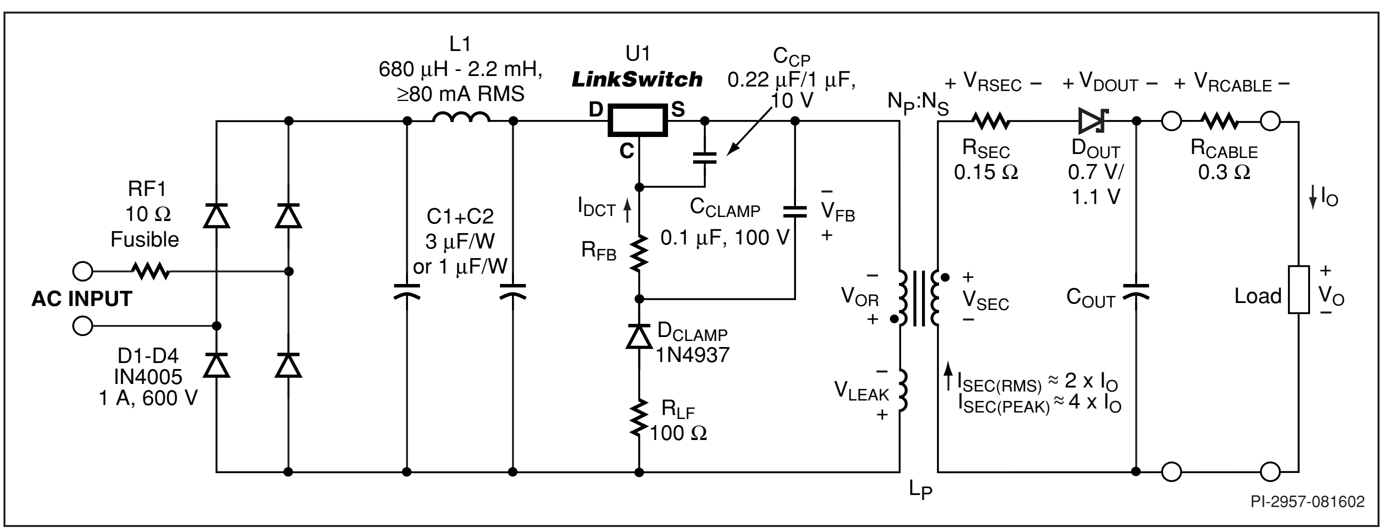

Figure 1. Key Parameters for an Initial LinkSwitch Design.

During CC operation, duty cycle is controlled by the peak drain current limit (I_{LIM}). The device current limit is designed to be a function of reflected voltage such that the load current remains approximately constant as the load impedance is reduced. When the output voltage falls to approximately 30% of nominal value (normally associated with a failed battery), *LinkSwitch* enters the auto-restart mode of operation to safely limit average fault current (typically 8% of I_O).

With discontinuous mode design, maximum output power is independent of input voltage and is a simple function of primary inductance, peak primary current squared and switching frequency (Equation 6). *LinkSwitch* controls and cancels out variations normally associated with frequency and peak current by specifying a device I^2f term. This allows users to easily design for a specific corner point where CV mode transitions to CC mode.

Scope

This application note is for engineers designing an AC-DC power supply using the *LinkSwitch* LNK500 or LNK501 devices in a discontinuous mode flyback converter. Since *LinkSwitch* is designed to replace linear transformer based power supplies, the output characteristic provides an approximate CV characteristic, offering much better line and load regulation than an equivalent linear transformer. The very simple nature of the *LinkSwitch* circuit allows an initial paper design to be completed quickly using simple design equations. It is then recommended that the circuit performance be tuned with a prototype power supply to finalize external component choices. This document therefore highlights the key design parameters and provides expressions to calculate the transformer turns ratio, primary inductance and clamp/feedback component values. This enables designers to build an operating prototype and iterate to reach the final design.

For readers who want to generate a design as quickly as possible, the Quick Start section provides enough information to generate an initial prototype.

This document does not address transformer construction. Please see *LinkSwitch* DAK Engineering Prototype Report for examples showing typical transformer construction techniques. Further details of support tools and updates to this document can be found at *www.powerint.com*.

QUICK START

Figure 1 shows the key parameters and components needed to generate an initial *LinkSwitch* design. Where initial estimates can be used, they are shown below the parameter they refer to.

1) Let V_{OR} equal 50 V.
2) Define the transformer turns ratio according to Equation 5. If no better estimates or measurements are available, then let V_{DOUT} equal 0.7 V for a Schottky or 1.1 V for a PN diode, R_{CABLE} equal 0.3 Ω, R_{SEC} equal 0.15 Ω, $I_{SEC(RMS)}$ equal 2 x I_O, and $I_{SEC(PEAK)}$ equal 4 x I_O, where I_O is the desired CC output current and V_O is the desired output voltage at the CV/CC transition point.
3) Calculate $P_{O(EFF)}$ according to Equation 13. As an initial estimate for P_{CORE} use 0.1 W.
4) Calculate L_P according to Equation 14 and other transformer parameters from Equations 15, 16, 17, 18 and 19.
5) Calculate value for feedback resistor R_{FB} according to Equations 20, 21, 22, 23 and 24. This should be a 1/4 W, 1% part.
6) Set clamp capacitor C_{CLAMP} as a 0.1 µF, 100 V metalized plastic film type.
7) Set clamp resistor R_{LF} as 100 Ω, 1/4 W.
8) Set CONTROL pin capacitor C_{CP} to be 0.22 µF, 10 V for battery loads or 1 µF, 10 V for resistive loads.
9) Select input and output components. See Figure 3 and relevant sections.
10) Construct prototype.
11) Iterate design (see Hints and Tips section).

CV/CC Circuit Design

The *LinkSwitch* circuit shown in Figure 3 serves as a CV/CC charger example to illustrate design techniques. Nominal output voltage is 5.5 V and nominal CC output current is 500 mA.

LinkSwitch design methodology is very simple. Transformer turns ratios and bias component values are selected at the nominal peak power point output voltage V_O, while transformer primary inductance is calculated from the total output power. Few components require computations, while the balance are selected from the included recommendations.

Design and selection criteria for each component are described starting with the transformer. Once set, transformer parameters and behavior are used to design clamp, bias and feedback components for proper supply operation. Output capacitors and the input circuitry can then be determined.

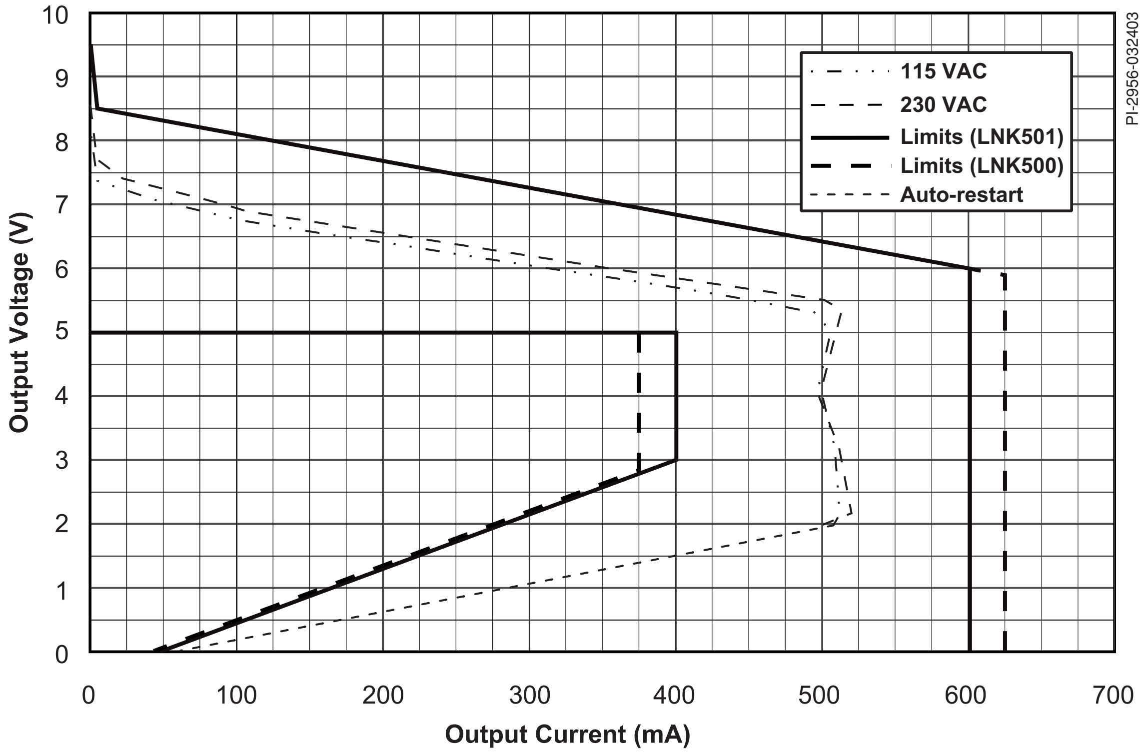

Figure 2. Typical Output Characteristic for LinkSwitch Based 5.5 V, 0.5 A Charger with Specification Limits.

Transformer T1

Transformer design begins by selecting the reflected output voltage (V_{OR}). For most *LinkSwitch* designs, V_{OR} should be between 40 V and 60 V. A good starting point is 50 V allowing for optimization later.

V_{OR} values over 60 V are recommended only for those applications allowed to consume over 300 mW at no-load.

To calculate the transformer turns ratio, the voltage required across the secondary winding V_{SEC} is first calculated. This is a function of output cable voltage drop V_{RCABLE}, nominal output voltage V_O, the secondary winding voltage drop V_{RSEC}, and output diode forward voltage drop V_{DOUT}. Figure 1 shows the sources of secondary side voltage drops. Since C_{CLAMP} charges to the peak value of V_{OR} plus an error due to leakage inductance, the value of V_{RSEC} and V_{DOUT} are defined at the peak secondary current. The output cable drop V_{RCABLE} is defined at the nominal CC output current I_O.

Curves of V_{DOUT} versus instantaneous current can be found in the diode manufacturer's data sheet. Peak secondary current is defined as:

$$I_{SEC(PEAK)} = I_{PRI(PEAK)} \times \frac{N_P}{N_S} \tag{1}$$

The value for $I_{PRI(PEAK)}$ is equal to the typical value of the *LinkSwitch* data sheet parameter I_{LIM}.

As an initial estimate the $I_{SEC(PEAK)}$ can be approximated as $4 \times I_O$. Once the first prototype has been built this can be refined as the final turns ratio is known or alternatively, the peak diode forward voltage can be measured directly using an oscilloscope.

$$V_{RCABLE} = I_O \times R_{CABLE} \tag{2}$$

$$V_{RSEC} = I_{SEC(PEAK)} \times R_{SEC} \tag{3}$$

$$V_{SEC} = V_O + V_{RCABLE} + V_{DOUT} + V_{RSEC} \tag{4}$$

The transformer turns ratio is given by:

$$\frac{N_P}{N_S} = \frac{V_{OR}}{V_{SEC}} \tag{5}$$

If no better estimates or measurements are available, use 0.15 Ω as an initial value for the transformer secondary winding resistance R_{SEC}, 0.7 V for the forward voltage (V_{DOUT}) of a Schottky diode or 1.1 V for a PN diode and 0.3 Ω for the cable resistance R_{CABLE}.

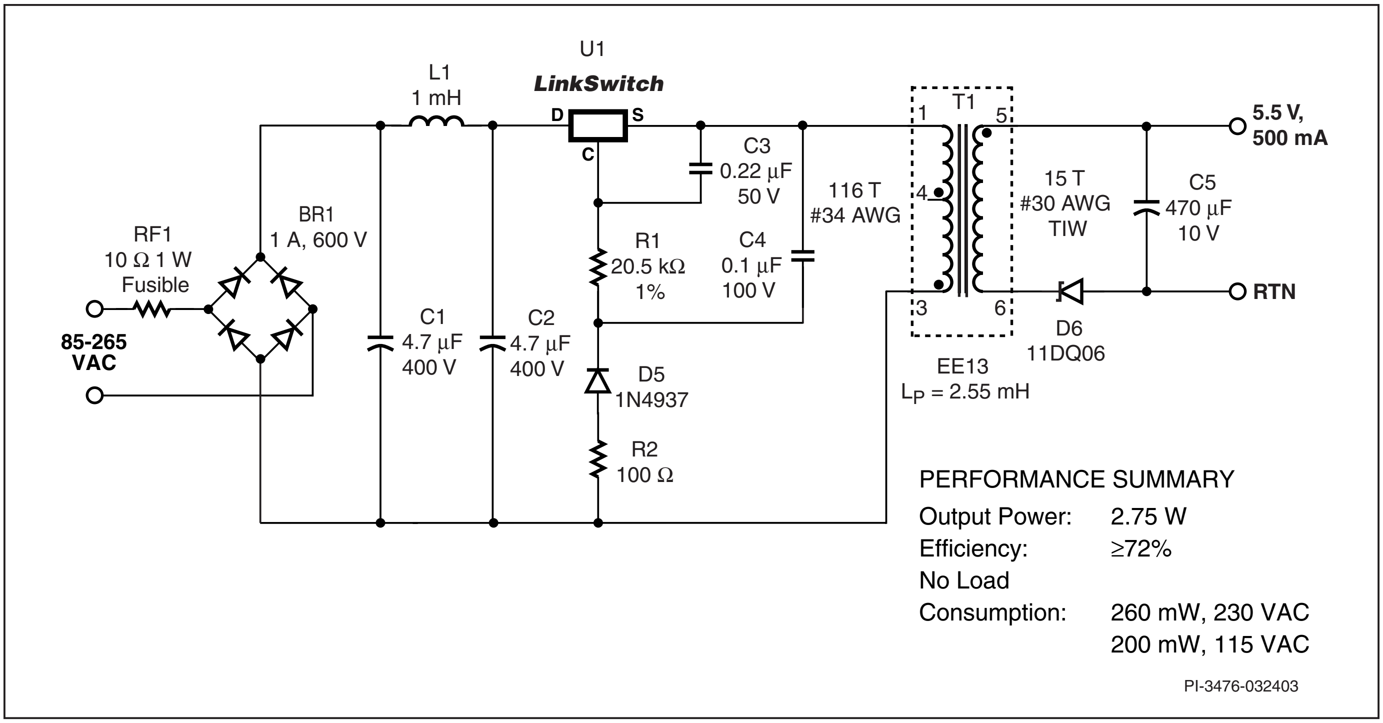

Figure 3. Example Schematic for a Typical LinkSwitch Charger.

The next transformer design step is to calculate the nominal primary inductance L_P. L_P tolerance should be within ±10% (to meet peak power CC tolerance of ±20% for LNK501, ±25% for LNK500). The simple *LinkSwitch* feedback circuit is designed specifically for discontinuous mode operation. Continuous mode designs result in control loop instability and are therefore not recommended. For proper CC operation, the *LinkSwitch* transformer must therefore be designed for discontinuous operation under all line/load conditions.

At the peak power point, the power processed by the core or $P_{O(EFF)}$ is given by:

$$P_{O(EFF)} = \frac{1}{2} \times L_P \times \left[I_P^2 \times f_S \right] \tag{6}$$

L_P is the nominal transformer primary inductance, I_P is equal to the *LinkSwitch* parameter I_{LIM} and f_S is the switching frequency. Note that I_P and f_S are enclosed in brackets as the *LinkSwitch* data sheet specifies an I^2f coefficient equal to the $I_P^2 f_S$ product, normalized to I_{DCT}. By normalizing to I_{DCT} (the CONTROL pin current at 30% duty cycle), the effect of I_{DCT} tolerance is included and does not need to be considered separately. Output power is therefore dependent primarily on transformer primary inductance tolerance (typically ±10% for low cost high volume production methods).

As shown above, effective output power $P_{O(EFF)}$ is calculated from the total energy stored in the transformer and is therefore the sum of actual output power P_O and the following loss terms: cable power P_{CABLE}, diode power P_{DIODE}, bias power P_{BIAS}(the power required to drive the *LinkSwitch* CONTROL pin), transformer secondary copper loss $P_{S(CU)}$, and transformer core loss P_{CORE}.

$$P_{CABLE} = R_{CABLE} \times I_O^2 \tag{7}$$

$$P_{DIODE} = V_{DOUT} \times I_O \tag{8}$$

$$P_{BIAS} = V_{OR} \times 2.3\ mA \tag{9}$$

$$P_{CORE} = \frac{K_{CORE} \times V_E}{2} \tag{10}$$

$$P_{S(CU)} = I_{SEC(RMS)}^2 \times R_{SEC} \tag{11}$$

R_{CABLE} is the total cable DC resistance, I_O is the nominal CC output current, V_{DOUT} is output diode forward voltage drop, V_{OR} is reflected output voltage, $I_{SEC(RMS)}$ is secondary RMS current, R_{SEC} is output winding DC resistance, V_E is core effective volume and K_{CORE} is core loss per unit volume. As before, if no better estimates or measurements are available, use 0.15 Ω for R_{SEC}, 0.7 V for the forward voltage (V_{DOUT}) of a Schottky diode or 1.1 V for a PN diode, 0.3 Ω for R_{CABLE} and $I_{SEC(PEAK)}$ equal to 4 x I_O. Both V_E and K_{CORE} can be read from the ferrite core manufacturer's material curves. To find K_{CORE}, use the core flux swing B_M. In discontinuous mode operation, AC Flux Density B_{AC} is equal to B_M:

$$B_{AC} = B_M \tag{12}$$

The division by two in the expression for P_{CORE} is required since a flyback transformer only excites the core asymmetrically and the core loss curves are typically specified assuming a symmetrical excitation.

K_{CORE} is then read directly from material core loss curves at the *LinkSwitch* switching frequency (typically 42 kHz). A figure for B_M of approximately 3300 gauss (330 mT) is a good initial estimate. A figure for P_{CORE} of 0.1 W is a good initial estimate.

$P_{O(EFF)}$ is calculated from:

$$P_{O(EFF)} = P_O + P_{CABLE} + P_{DIODE} + P_{BIAS} + P_{S(CU)} + \frac{P_{CORE}}{2} \tag{13}$$

P_O here is defined as the output power seen by the load. Note the core loss term is divided in half as only the loss associated with transferring energy to the output during the off time needs to be compensated for in the primary inductance value.

Nominal primary inductance $L_{P(NOM)}$ is calculated from:

$$L_{P(NOM)} = \frac{2 \times P_{O(EFF)}}{\left[I_P^2 \times f_S\right]} \times \Delta_L \tag{14}$$

The typical data sheet value for the I^2f coefficient should be used to replace $I_P^2 f_S$, this defining the nominal primary inductance at the nominal output peak power point.

As the flux density increases, the inductance falls slightly due to the BH characteristic of the core material as shown in Figure 4. This drop in inductance is compensated by increasing the inductance at zero flux density by a factor Δ_L. This is typically in the range of 1 to 1.05 for common low cost ferrite materials. This effect can be minimized by increasing the gap size, reducing the flux density or using ferrite materials with a higher saturation flux density.

Transformer inductance tolerance is most affected by the transformer core gap length. Inductance must also be stable over temperature and as a function of current. Recommended minimum gap length is 0.08 mm (3.2 mils) at a peak flux density of 3300 gauss to 3500 gauss (330 mT to 350 mT).

The number of secondary turns for small E cores is typically 2 to 3 turns per volt across the secondary winding (including cable, secondary and diode voltage drops). The actual number is adjusted to meet gap size and flux density limits.

Once an estimate for the number of secondary turns N_S has been made, the primary turns is found from:

$$N_P = \frac{V_{OR}}{V_{SEC}} \times N_S \tag{15}$$

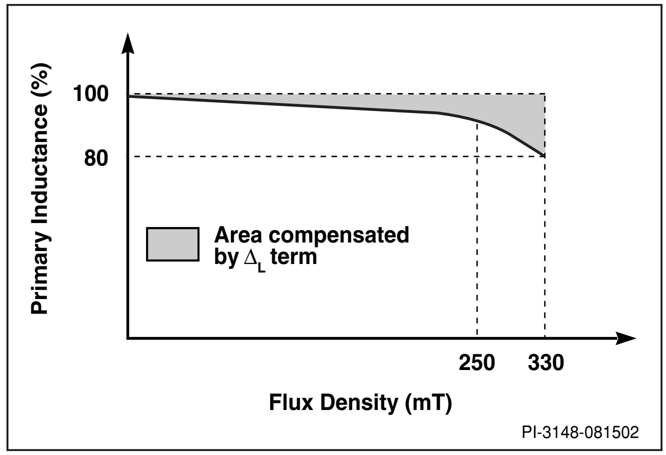

Figure 4. Typical Reduction in Primary Inductance with Flux Density for Small E Cores with Small Gap Sizes.

At this point the core size should be selected. Common core sizes suitable for a *LinkSwitch* design include EE13, EF12.6, EE16 and EF16. With the core selected and the number of transformer turns known, the core peak flux density B_P (gauss) can be found using the effective cross sectional area of the core A_e (cm^2), the primary inductance (µH) and the *LinkSwitch* peak current limit $I_{LIM(MAX)}$ (A):

$$B_P = \frac{100 \times I_{LIM(MAX)} \times L_P}{N_P \times A_e} \tag{16}$$

B_P should be in the range of 3000 gauss to 3500 gauss (300 mT to 350 mT).

The relative permeability μ_r of the ungapped core must be calculated to estimate the gap length L_g. The relative permeability, μ_r is found from core parameters A_e (cm^2), the effective core path length L_e (cm), and ungapped effective inductance A_L(nH/t^2):

$$\mu_r = \frac{A_L \times L_e}{0.4 \times \pi \times A_e \times 10} \tag{17}$$

Gap length L_g is the air gap ground into the center leg of the transformer core. Grinding tolerances and A_L accuracy place a minimum limit of approximately 0.08 mm on L_g. If L_g is smaller than this then either the core size (A_e) or N_P must be increased. L_g (mm) is calculated from primary turns N_P, core effective cross sectional area A_e (cm^2), primary inductance L_P (µH), core effective path length L_e (cm) and relative permeability μ_r:

$$L_g = \left[\frac{0.4 \times \pi \times N_P^2 \times A_e}{L_P \times 100} - \frac{L_e}{\mu_r} \right] \times 10 \qquad (18)$$

The gapped effective inductance A_{LG} (nH/t^2), required by the transformer manufacturer, is calculated from the primary inductance L_P (µH) and the number of primary turns N_P:

$$A_{LG} = 1000 \times \frac{L_P}{N_P^2} \qquad (19)$$

Clamp, Bias, Bypass and Feedback

An RCD clamp, formed by R_{FB}, C_{CLAMP}, and D_{CLAMP} (Figure 1), safely limits transformer primary voltage, due to transformer leakage inductance, to below the *LinkSwitch* internal MOSFET breakdown voltage BV_{DSS} each time *LinkSwitch* turns off. Leading-edge voltage spikes (caused by transformer leakage inductance) are filtered by R_{LF} and C_{CLAMP}, such that C_{CLAMP} effectively charges to the transformer reflected voltage.

Feedback is derived from the reflected voltage, that approximates closely the transformer secondary winding output voltage (V_{SEC} in Figure 1) multiplied by the transformer turns ratio. Due to effects of leakage inductance (causing peak charging), calculated V_{OR} may be slightly different from actual voltage measured across C_{CLAMP}. Since *LinkSwitch* is in the upper rail, reflected voltage information is now relative to the *LinkSwitch* SOURCE pin and independent of the input voltage.

Reflected voltage is directly converted by R_{FB} to *LinkSwitch* CONTROL pin current for duty cycle control and bias. The CONTROL pin capacitor C_{CP} provides bypass filtering, control loop compensation, and the energy storage required during start-up and auto-restart.

Feedback Resistor (R_{FB})

Clamp and feedback circuit design begins by first considering reflected voltage. Using the schematic in Figure 3 as an example. With primary turns N_P = 116 and secondary turns N_S = 15 the peak secondary current can be calculated from Equation 20, where $I_{PRI(PEAK)}$ is equal to the *LinkSwitch* typical current limit $I_{LIM(TYP)}$.

$$\begin{aligned} I_{SEC(PEAK)} &= \frac{N_P}{N_S} \times I_{PRI(PEAK)} \\ &= \frac{116}{15} \times 0.254 \\ &= 1.96\ A \end{aligned} \qquad (20)$$

The secondary diode peak voltage was measured as 0.7 V, the secondary winding resistance as 0.15 Ω and the cable resistance as 0.23 Ω. Therefore V_{SEC} is defined as:

$$\begin{aligned} V_{SEC} &= V_O + V_{RCABLE} + V_{DOUT} + V_{RSEC} \\ &= V_O + (I_O \times R_{CABLE}) + V_{DOUT} \\ &\quad + (I_{SEC(PEAK)} \times R_{SEC}) \\ &= 5.5\ V + (0.5\ A \times 0.23\ \Omega) + 0.7\ V \\ &\quad + (1.96\ A \times 0.15\ \Omega) \\ &= 6.61\ V \end{aligned} \qquad (21)$$

Voltage V_{SEC} allows the exact V_{OR} to be calculated:

$$\begin{aligned} V_{OR} &= \frac{N_P}{N_S} \times V_{SEC} \\ &= \frac{116}{15} \times 6.61\ V \\ &= 51.1\ V \end{aligned} \qquad (22)$$

Resistor R_{FB}, a 1%, 0.25 W resistor, converts clamp voltage to *LinkSwitch* bias and control current.

Feedback voltage V_{FB} is calculated from V_{OR} and the error due to leakage inductance, V_{LEAK}.

The value for V_{LEAK} varies depending on the value of leakage inductance, the size of the clamp capacitor and the type of clamp diode selected. For a leakage inductance of 50 µH, a value of 5 V is a good initial estimate.

$$V_{FB} = V_{OR} + V_{LEAK} \qquad (23)$$

Once a prototype has been constructed, the value of V_{FB} can be found directly, by measuring the voltage across C_{CLAMP} at the power supply peak output power point, using a battery powered digital voltmeter. These have sufficient common mode rejection to be unaffected by the switching waveform and provide accurate results. The voltage measured is V_{FB}. By subtracting V_{OR} the value for V_{LEAK} can be determined, useful as an estimate in future designs. For the design in Figure 3, V_{FB} was measured as 56.7 V, giving V_{LEAK} as 5.6 V.

An initial value for R_{FB} is calculated from the feedback voltage V_{FB}, the CONTROL pin voltage $V_{C(IDCT)}$ and current I_{DCT} at the CC/CV transition point, specified in the *LinkSwitch* data sheet.

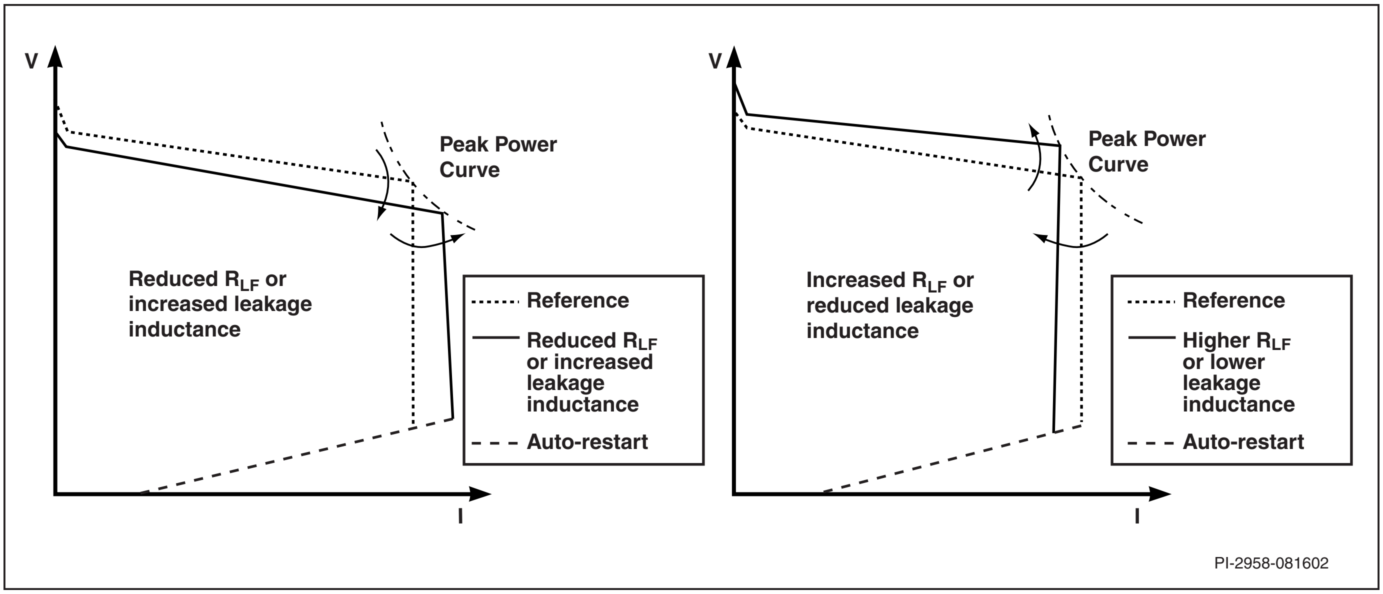

Figure 5. Effect on Output Characteristic when R_{LF} or Leakage Inductance Changes.

$$R_{FB} = \frac{V_{FB} - V_{C(IDCT)}}{I_{DCT}} = \frac{56.7\ V - 5.75\ V}{2.3\ mA} = 22\ k\Omega \tag{24}$$

Select the nearest standard value. Resistor R_{FB} can then be adjusted to center the output voltage. The example in Figure 3 uses a 20.5 kΩ value for R_{FB} (R1), centering the output voltage V_O near 5.5 V at nominal output current I_O.

Note that R_{FB} power dissipation, a significant component of *LinkSwitch* standby power, should always be calculated:

$$P_{RFB} = (2.3\ mA)^2 \times R_{FB} = 111\ mW \tag{25}$$

For applications that do not need to comply with strict standby power requirements, higher values of V_{OR} can be used, also increasing the power capability of *LinkSwitch*.

Clamp Diode (D_{CLAMP})

Diode D_{CLAMP} should be an ultra-fast or fast recovery diode with at least 600 V breakdown voltage. Fast types typically offer a slight cost advantage and also reduce EMI, so they are preferred.

Note that normal recovery diodes (1N400X or similar types), which may allow excessive drain voltage ringing, should not be used.

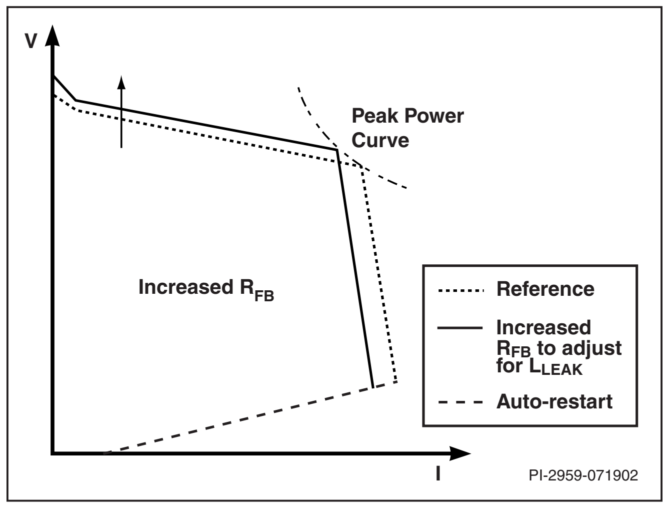

Figure 6. Increasing R_{FB} to Adjust for High Leakage Increases No load Voltage and Consumption.

Clamp Resistor (R_{LF})

The value for R_{LF}, which effectively filters the leakage inductance spike from the reflected voltage waveform, is verified empirically through iteration. R_{LF} has a direct effect on both the average value and slope of both the CV and CC curves as shown in Figure 5 and can therefore be used to tune the output characteristic to some extent.

In the CV region, increasing R_{LF} increases the average output voltage, while reducing the slope of the CV region (the change in output voltage with the change in output current). In the CC region, increasing R_{LF} makes the average output current lower, while tending to "bend" the curve inward slightly (fold back).

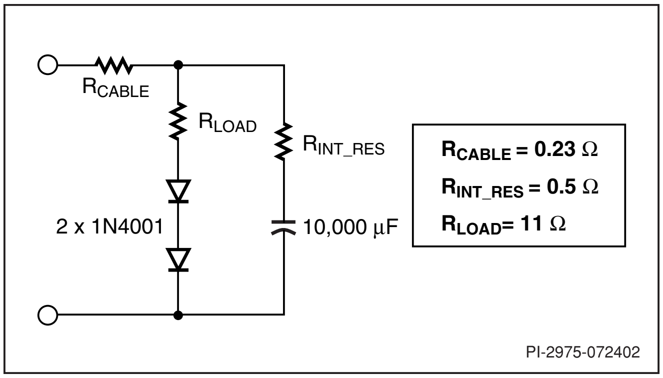

Figure 7. Example of Battery Model Load (Values for a Typical 3 W, 5.5 V Battery Charger).

At no-load, increasing R_{LF} slightly increases the no-load voltage since the primary leakage inductance is filtered more effectively, but the same peak charging due to secondary leakage inductance occurs. Although the no-load voltage is slightly higher, there is only a minor effect on no-load consumption.

In a design that has high leakage, the value of R_{FB} can be increased to raise the overall output voltage (Figure 6). However, this will also increase no-load voltage and therefore no-load input power consumption.

To iterate R_{LF}:

- Start with typical value of 100 Ω and a transformer with nominal inductance.
- Verify CC portion of the curve and increase or decrease R_{LF} until CC curve is approximately vertical (current at start of CC and end are approximately the same)
- Verify CV portion of the curve.
  - For minor adjustment, change value of R_{FB}.

Clamp Capacitor (C_{CLAMP})

With small values of clamp capacitor C_{CLAMP}, the output voltage tends to be slightly higher. With larger values for C_{CLAMP}, output voltage will be slightly lower. Further increases in C_{CLAMP} will not change the output voltage.

C_{CLAMP} is therefore chosen empirically as the smallest value that does not significantly change the output voltage when compared to the next larger value. For most designs, 100 nF is typical and standard device tolerances will have a negligible effect on the output voltage. This capacitor should be rated above the V_{OR}, typically 100 V.

C_{CLAMP} must have a stable value over temperature and also over the operating voltage range. Metalized plastic film capacitors are the best choice, since the higher voltage ceramic capacitors with stable dielectrics (NPO or COG, for example) are higher cost. The value of low cost ceramic capacitors varies significantly with voltage and temperature (Z5U dielectric, for example) and should not be used since they may cause output oscillation.

CONTROL Pin Capacitor (C_{CP})

C_{CP} sets the auto-restart period and also the time the output has to reach regulation before entering auto-restart at power supply start-up. If the load is a battery, then a value of 0.22 µF is typical. However, if the supply is required to start into a resistive load or constant current load (such as a bench electronic load) at the peak output power point, then this should be increased to 1 µF. This ensures enough time during start-up to bring the output into regulation. The type of capacitor is not critical. Either a small ceramic or electrolytic may be used with a voltage rating of 10 V or more.

Output Rectifier and Filter (D_{OUT}, C_{OUT})

The output diode should be selected with an adequate peak inverse voltage (PIV) rating. Either PN or Schottky diodes can be used. Schottky diodes offer higher efficiency at higher cost but provide the most linear CC output characteristic. Both fast or ultra fast PN diodes may be used, but ultra fast (t_{rr}~50 ns) are preferred giving CC linearity close to the performance of a Schottky.

$$PIV\ D_{OUT} \geq \left(V_{DC(MAX)} \times \frac{N_S}{N_P} \right) + \left(V_O \times 1.5 \right) \quad (26)$$

The output diode voltage rating should be calculated from Equation 26. $V_{DC(MAX)}$ is the maximum primary DC rail voltage (375 V for universal or 230 VAC and 187 V for 115 VAC only designs). The output voltage V_O is multiplied by 1.5 to allow for increased output voltage at no-load. An output diode current rating of 2 x I_O is a good initial estimate.

The output diode may be placed in either the upper or lower leg of the secondary winding. However, placement in the lower leg may provide lower conducted EMI with a suitably constructed transformer.

For battery charger applications, the size and cost of the output capacitor C_{OUT} can be significantly reduced. High ripple current flows through C_{OUT} for only the short time a fully depleted battery charges. The designer should take into account that C_{OUT} ripple current rating can be exceeded for short periods of time without reducing lifetime significantly. When the battery is close to fully charged, the *LinkSwitch* circuit transitions to CV mode, where capacitor ripple current is much smaller.

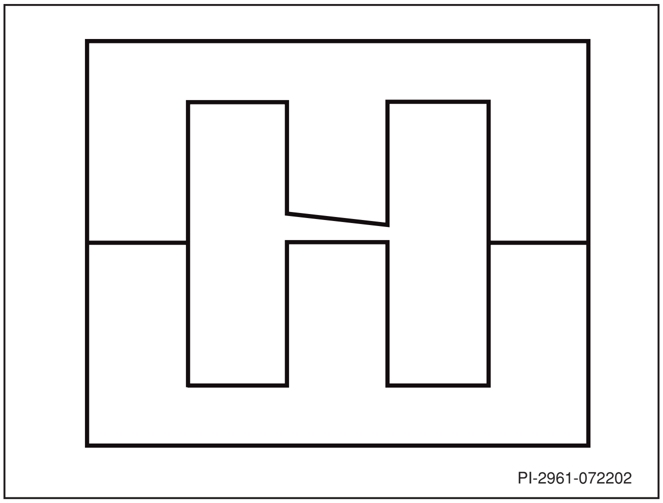

Figure 8. Uneven Core Gapping Makes CC Portion Nonlinear and Should be Avoided.

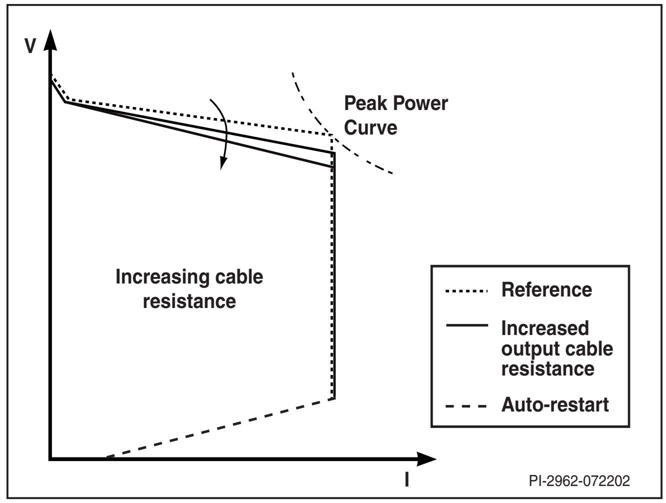

Figure 9. Effect on Output Characteristic Due to Increased Output Cable Resistance.

For adapter applications drawing rated load current in steady state, C_{OUT} should be a low ESR type, properly rated for ripple current.

Designs for battery charging usually do not require an additional output L-C stage (π filter) to reduce switching noise. The battery itself will filter this noise and output ripple. However, if the load is resistive, then this stage may be required to meet ripple and noise specifications. For evaluation of a battery charger during design, a battery load can be simulated using a circuit similar to that shown in Figure 7, which models both the battery and output cable.

Bridge Rectifier, Energy Storage, and EMI Filter

Figure 1 shows a typical input stage for a low cost design. D1-D4 rectifies universal AC input voltage. C1 and C2 provide energy storage, smoothing, and EMI filtering. RF1 reduces surge current, EMI and will also safely open, like a fuse, if another primary component fails in a short circuit.

The conducted emissions EMI filter has effectively two differential mode stages. RF1 and C1 form the first differential mode stage. The second differential mode filter stage is formed by L1 and C2.

RF1 should be a 10 Ω low cost wire-wound fusible resistor or be replaced by a fuse. A resistor is preferable to a fuse as it also limits inrush current and protects against input voltage transients and surges (differential or normal mode). Lower values increase dissipation (V^2/R power term) during transients and inrush, while higher values increase steady state dissipation (I^2R) and lower overall efficiency. Metal film types should not be used since they do not have a high enough transient power capability to survive line transient and inrush current and may fail prematurely in service.

To meet certain safety agency requirements RF1 should fail open without emitting smoke, fire or incandescent material, that might damage the primary-to-secondary insulation barrier. Consult with a safety engineer or local safety agency for specific guidance.

Diodes D1-D4 should be rated at 400 V or above and be standard recovery types to minimize EMI.

The combined value of C1 and C2 should be selected to give 3 μF per watt (of output power), giving acceptable voltage ripple for universal designs. For high single input voltage ranges (185 VAC to 265 VAC), this recommendation can be reduced to 1 μF/W, however ripple current ratings and differential mode line transient performance should be verified.

L1, which is effective for low frequencies, is typically in the range of 680 μH to 2.2 mH and should have a current rating of ≥80 mA RMS.

Hints and Tips

Transformer Construction

Since the primary inductance is crucial in setting the peak output power, the tolerance of this parameter should be well controlled. For a CC tolerance at the peak power point of ±20%/±25% (LNK501/LNK500, respectively) the primary inductance tolerance should be ±10% or better.

Tolerance of ungapped core permeability limits minimum gap size for center leg gapping. For an EE13 core size, the practical minimum center leg gap size, for an overall primary inductance tolerance of ±10%, is ~0.08 mm. This varies with core supplier, so this should be verified before committing to a design.

Other gapping techniques allow tighter tolerances, but may not be universally supported, so again, this should be verified with the preferred magnetics vendor. Film gapping, where thin material spaces all three legs of the core, allows better mechanical tolerance and improves overall primary inductance tolerance to ±7% with a 0.05 mm gap. Since a gap now appears on the outer legs of the core, flux spraying may result, causing pick up in the input filter components and resulting in poorer than expected conducted EMI. This can be prevented, if necessary, by adding a single shorted turn of copper foil around the outside of the transformer core also known as a "belly band."

Core gaps should be uniform. Uneven core gapping (see Figure 8), especially with small gap sizes, may cause variation in the primary inductance with flux density (partial saturation) and make the constant current region nonlinear. To verify uniform gapping, it is recommended that the primary switching current waveshape be examined while feeding the supply from a DC source. The slope is defined as di/dt = V/L and should remain constant throughout the MOSFET on time. Any change in slope of the current ramp is an indication of uneven gapping.

Verifying Discontinuous Mode Operation

To verify a design will remain discontinuous conduction mode under worst case condition use Equation 27:

$$\frac{2 \times I_{O(MAX)} \times f_{S(MAX)} \times L_{P(MAX)}}{D \times (1-D) \times V_{DC(MIN)}} < \frac{N_P}{N_S} \qquad (27)$$

where $I_{O(MAX)}$ is the output current (A) at maximum CC tolerance (typically $I_{O(NOM)}$ + 20%), $f_{S(MAX)}$ is the maximum *LinkSwitch* switching frequency (Hz), $L_{P(MAX)}$ is the primary inductance (H) at maximum tolerance, D is duty cycle at minimum input voltage (typically 0.3 at 85 VAC or 0.13 at 195 VAC) and $V_{DC(MIN)}$ the minimum DC voltage at lowest input line voltage (typically 100 VDC for 85 VAC and 230 VDC for 195 VAC).

Effect of Output Cable

Factors such as leakage inductance, the value for R_{LF}, R_{FB} and C_{CLAMP} have been covered. However, there are other parameters that should be considered when designing with *LinkSwitch*.

If the gauge of wire selected for the output cable is reduced, then the voltage drop across the cable resistance will increase. As seen at the load, this appears as poorer CV operation and lower efficiency, but with the CV/CC transition at the same output current (see Figure 9). Ensure that the voltage drop or resistance of the output cable is acceptable.

Reducing No-load Voltage with a Pre-load

At very light loads (< ~5 mA), the output voltage rises due to secondary peak charging. This can be significantly reduced by the addition of a small pre-load resistor. Figure 10 shows the effect of a 1 mA and 2 mA pre-load on a 9 V output design, reducing the no-load voltage by 1.3 V. This level of pre-load has minimal effect on no-load consumption (~10 mW to 20 mW).

Minimizing No-Load Consumption

The major factors for no-load or standby consumption are P_{BIAS} and the capacitive switching loss $P_{C(LOSS)}$ (Equations 9 and 28). If no-load consumption is too high, then the transformer may be redesigned with a lower V_{OR}.

Total parasitic capacitance of device and transformer, typically 25 pF to 30 pF, causes a switching loss that increases with input voltage and has a significant effect on standby or no-load output power consumption.

$$P_{C(LOSS)} = \frac{C_{TOT} \times V_{MAX}^2 \times f_S}{2} \qquad (28)$$

V_{MAX} is typically 340 V for universal or 230 VAC applications and f_S is 30 kHz at light or no load. Parasitic capacitance loss $P_{C(LOSS)}$ is typically 40 mW to 100 mW. This loss is not included in the L_P calculation as this power is not processed through the core.

To minimize transformer capacitance, double coated magnet wire should be used for the primary winding. The technique of vacuum impregnation should not be used since the varnish acts as a dielectric, increasing winding capacitance. Dip varnishing does not cause this problem.

An RC snubber placed across the output diode also increases no-load consumption. If necessary, minimize the value of the

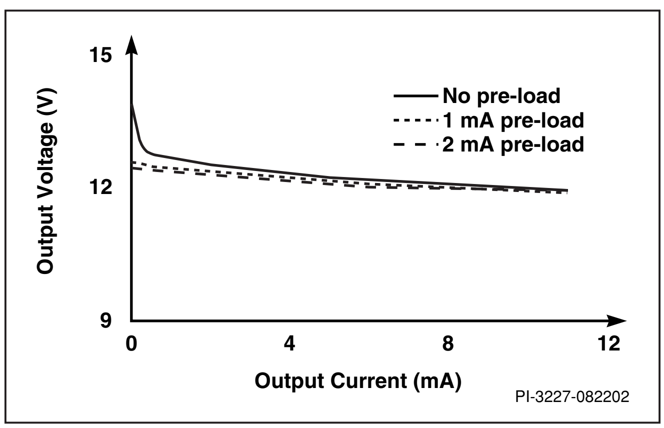

Figure 10. A Small Pre-load can Significantly Reduce No-load Voltage.

capacitor used. If an ultra-fast diode has been selected, try a fast diode as this may allow the snubber to be removed.

Correct Oscilloscope Connection

To prevent the additional capacitance of an oscilloscope probe from triggering the *LinkSwitch* current limit, do not connect the scope ground to the SOURCE pin. The scope should be connected as shown in Figure 11 to measure source to drain voltage. Since the scope is referenced to the DC rail, an isolation transformer must be used.

Improving CV Tolerance with Optocoupler

The schematic in Figure 12 shows an example of adding a secondary reference and optocoupler to improve CV tolerance across the entire load range. The voltage drop (sense voltage) across VR1, U1 and R3 sets the nominal output voltage. The feedback resistor R_{FB} is split into two to form a divider which limits the voltage across the optocoupler phototransistor. The optocoupler therefore effectively adjusts the resistor divider ratio to control the DC voltage across R2 and the current into the CONTROL pin. For an output tolerance $\leq \pm 5\%$, VR1 should be replaced by a reference IC (TL431).

A full description of the operation with an optocoupler can be found in the *LinkSwitch* data sheet.

Single Point Failure Testing

The *LinkSwitch* circuit requires few considerations for single point failure testing. Breaking the feedback loop by opening either R_{LF}, D_{CLAMP} or R_{FB} results in *LinkSwitch* entering auto-restart. Under this condition, the secondary output voltage will rise but the output power is limited to ~8% of normal. This prevents the output capacitor from failing catastrophically. If

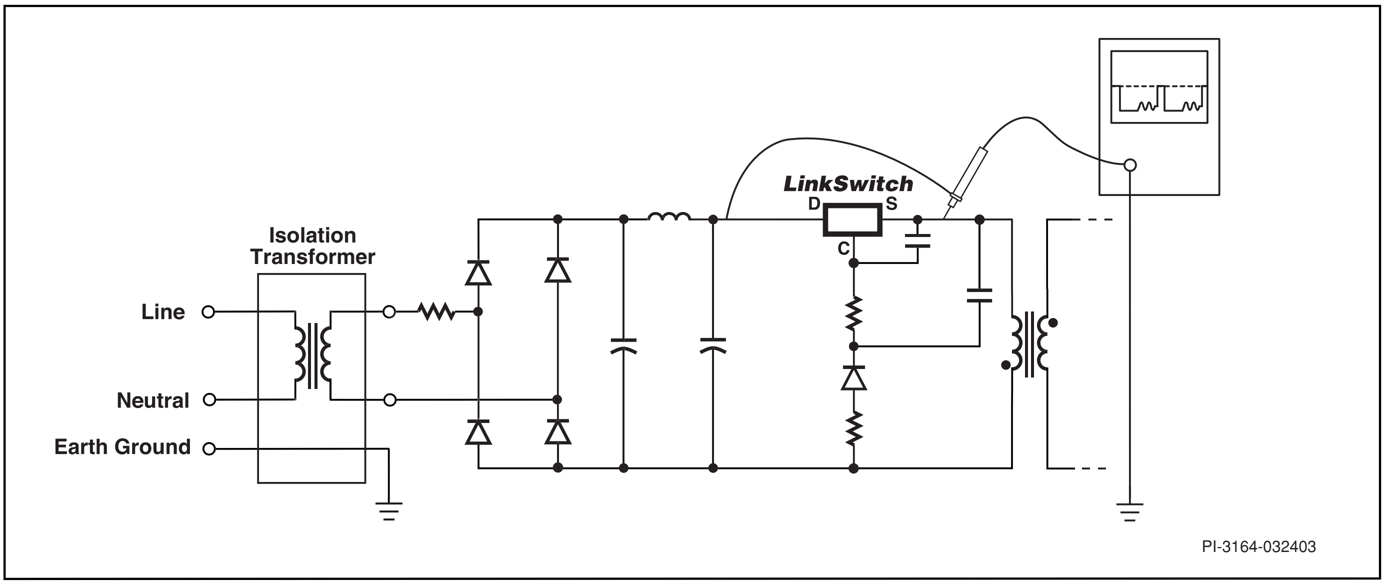

Figure 11. Correct Method of Connecting an Oscilloscope to Measure Switching Waveform.

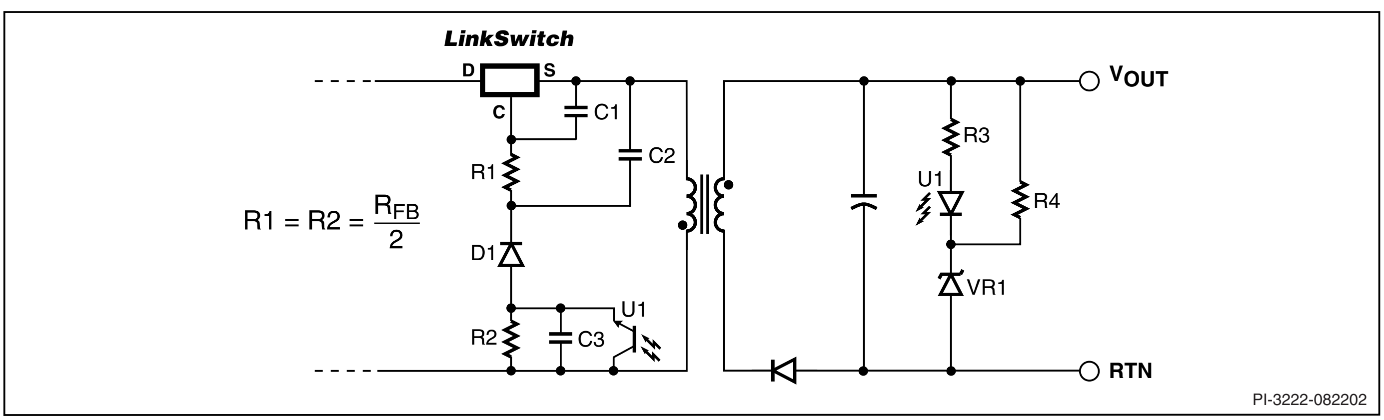

Figure 12. Power Supply Outline Schematic with Optocoupler Feedback.

desired, a 0.5 W Zener can be added across the output to clamp this voltage rise. The Zener voltage should be set above the normal maximum output voltage at no-load. Short circuiting or opening C_{CP} safely prevents *LinkSwitch* operation.

However, on opening of C_{CLAMP}, *LinkSwitch* does not enter auto-restart. The output voltage may rise unacceptably high under this condition and cause the failure of the output capacitor. As the supply delivers full power, output clamping requires a Zener power rating equal to or above the nominal output power.

Adding a second capacitor in parallel to C_{CLAMP} prevents this problem. When C_{CLAMP} is open circuited the second capacitor acts as C_{CLAMP}. This second capacitor can be a small value ceramic (0.01 μF) capacitor since during normal operation C_{CLAMP} dominates the parallel combination.

Appendix A–*LinkSwitch* Tolerance Analysis

Output Characteristic Tolerances

Both the device tolerance and external circuit govern the overall tolerance of the *LinkSwitch* power supply output characteristic. For a typical design, the peak power point tolerances are ±10% for voltage and ±20% (LNK501) / ±25% (LNK500) for current limit. This is the estimated overall variation due to *LinkSwitch*, transformer tolerance and line variation in high volume manufacturing.

This appendix provides expressions to allow the calculation of expected circuit variation when in high volume manufacturing for a design employing a LNK501 as shown in Figure 3.

The same analysis can be extended to the LNK500. The only significant difference is a wider I^2f tolerance (±12% compared to ±6% for LNK501) and associated increase in $\Delta I/\Delta V$ to ±3%.

Constant Current Limit

The peak power point prior to entering constant current operation is defined by the maximum power transferred by the transformer. Since *LinkSwitch* is designed to operate in discontinuous mode, the power transferred is given by the expression $P = 1/2\,L\,I^2f$, where L is the primary inductance, I is the primary peak current and f is the switching frequency.

To simplify analysis, the data sheet parameter table specifies an I^2f coefficient. This is the product of current limit squared and switching frequency, normalized to the feedback parameter I_{DCT}. This provides a single term that specifies the variation of the peak power point in the power supply due to *LinkSwitch*.

Additional variations are summarized in Table 1, as both random (unit-to-unit) or statistically independent variations

Variable	Biases	Random	$\Delta I/\Delta V$	Random + $\Delta I/\Delta V$	Biases + Random
Primary Inductance	–	±10%	±2.5%	±12.5%	
I^2f	–	±6%	±1.5%	±7.5%	
Input Line	±3.2%	±3%	–	±3%	
CC Linearity	–	±2%	–	±2%	
T_j (25-65 °C)	±1.5%	–	–	–	
Totals	±4.7%			±15%	±19.7%

Table 1. Sources of CC Tolerance.

and biases or deterministic variations (apparent in a single unit when tested). This distinction is made since random variations are added using the root-sum-squares method, whereas biases add directly. A further column ($\Delta I/\Delta V$), applicable to the I^2f and L_P terms, contains the value including the effect of the change in output current with output voltage. This is necessary because the CV slope is nonzero. Therefore, for example, if the peak power increases, the voltage at the new peak power point tends to be lower, further increasing the output current.

The figure of ±19.7% in Table 1 is the overall variation of the CC region.

It is important to note that the figure of ±2% for constant current linearity (the straightness of the constant current characteristic) is only valid for designs close to 3 W output power, with a primary inductance of ~3 mH. This is due to the internal compensation for drain current di/dt variations over line voltage. This compensation was arranged to correctly compensate, over a line voltage range of 85 VAC to 265 VAC, with a primary inductance of 3 mH. In lower power designs, where the primary inductance is lower, an error results which increases the non-linearity in the CC curve.

Output diode of choice also effects CC linearity. The value in Table 1 is based on a Schottky diode. The slower forward recovery time of a PN diode can cause the CC characteristic to bend outwards with falling output voltage.

Constant Voltage Operation at Peak Power Point

During CV operation, the output characteristic is controlled by adjusting the duty cycle, based on the voltage V_{FB} across capacitor C_{CLAMP} (Figure 1). A number of parameters define the actual output voltage, and therefore, the tolerance of the output voltage at the peak power point. The key parameters to consider are:

- Current variation through R_{FB} due to line voltage variation
- CONTROL pin voltage - $V_{C(IDCT)}$

- Output diode forward voltage - V_{DOUT}
- Current variation through R_{FB} due to CONTROL pin voltage tolerance at 30% Duty Cycle (I_{DCT})
- Feedback resistor tolerance - $\Delta\%_{RFB}$

Each of the key parameters above is examined in turn.

The most significant variation in the output voltage is the change with input line.

The voltage across R_{FB} is defined at I_{DCT}, corresponding to a 30% duty cycle at low line voltage. At higher line voltage, the CONTROL pin current increases and the voltage across R_{FB} increases. The change in voltage across R_{FB}, $\Delta V_{FB(LINE)}$, depends on the change in duty cycle ΔDC, the corresponding change in CONTROL pin current ΔI_C (mA) and the value R_{FB} (kΩ). The change in CONTROL pin current for a given change in duty cycle can be found from a curve in the *LinkSwitch* data sheet.

$$\Delta V_{RFB(LINE)} = \Delta I_C \times R_{FB} \quad \text{(A1)}$$

For a universal input voltage design, ΔDC from low line to high line is typically 0.2 (0.09 for a single input design) giving a change in CONTROL pin current of typically 0.15 mA.

The value of $\Delta V_{RFB(LINE)}$ should be expressed as a percentage of V_{FB} to give the variation at the power supply output. The expression for line variation (at the peak power point) is therefore:

$$\Delta\%_{LINE} = \pm\frac{\Delta V_{RFB(LINE)}}{2 \times V_{FB}} \times 100\% \quad \text{(A2)}$$

The CONTROL pin voltage $V_{C(IDCT)}$ is specified at a current equal to I_{DCT}, giving a duty cycle of 30% for a typical design at the peak power point, at 85 VAC input. The tolerance of this parameter includes temperature variation and can be read from the data sheet directly. Since the output voltage is actually controlled using V_{FB}, the variation of $V_{C(IDCT)}$ must be expressed as a percentage of V_{FB}. The expression for this is given by:

$$\Delta\%_{VC(IDCT)} = \pm\frac{V_{C(IDCT)(MAX)} - V_{C(IDCT)(TYP)}}{V_{FB}} \times 100\% \quad \text{(A3)}$$

Any variation in the output diode forward drop with temperature will cause a change in the output voltage. Expressing as a percentage of V_O gives the expression:

$$\Delta\%_{VDOUT} = \pm\frac{\Delta V_{DOUT}}{2 \times V_O} \times 100\% \quad \text{(A4)}$$

Typical values for the change in forward voltage for a temperature change of +50 °C are +0.1 V for a silicon PN diode and +0.025 V for Schottky diode. For device-to-device variations, please consult diode manufacturer.

Any change in the current through R_{FB}, due to the tolerance of the CONTROL pin current at 30% duty cycle, I_{DCT}, will also cause a change in the output voltage. The change in the voltage across R_{FB} (kΩ) due to the tolerance of I_{DCT} (mA) is given by:

$$\Delta V_{RFB(IDCT)} = \pm\frac{I_{DCT(MAX)} - I_{DCT(MIN)}}{2} \times R_{FB} \quad \text{(A5)}$$

Expressed as a percentage of the voltage across V_{FB}, the variation is:

$$\Delta\%_{IDCT} = \pm\frac{\Delta V_{RFB(IDCT)}}{V_{FB}} \times 100\% \quad \text{(A6)}$$

The overall variation can then be estimated using the expression:

$$\Delta\%_{CV} = \pm\Delta\%_{LINE} \pm \Delta\%_{VDOUT} \pm \sqrt{\Delta\%^2_{VC(IDCT)} + \Delta\%^2_{IDCT} + \Delta\%^2_{RFB}} \quad \text{(A7)}$$

Using the design shown in Figure 3 as an example:

$$\Delta\%_{VC(IDCT)} = \pm\frac{6\ V - 5.75\ V}{54.2\ V} \times 100\% = \pm 0.46\% \quad \text{(A8)}$$

$$\Delta\%_{VDOUT} = \pm\frac{0.025\ V}{2 \times 5.5\ V} \times 100\% = \pm 0.23\% \quad \text{(A9)}$$

$$\Delta V_{RFB(LINE)} = 0.15\ mA \times 20.5\ k\Omega = 3.1\ V \quad \text{(A10)}$$

$$\Delta\%_{LINE} = \pm\frac{3.1\ V}{2 \times 54.2\ V} \times 100\% = \pm 2.9\% \quad \text{(A11)}$$

$$\begin{aligned}\Delta V_{RFB(IDCT)} &= \pm\frac{2.36\ mA - 2.24\ mA}{2} \times 20.5\ k\Omega \\ &= \pm 1.23\ V\end{aligned} \quad \text{(A12)}$$

$$\Delta\%_{IDCT} = \pm\frac{1.23\ V}{54.2\ V} \times 100\% = \pm 2.27\% \quad \text{(A13)}$$

The tolerance of R1 (R_{FB}) is 1%.

$$\begin{aligned}\Delta\%_{CV} &= \pm 2.9\% \pm 0.23\% \pm \sqrt{(0.46^2 + 2.27^2 + 1^2)} \\ &= \pm 2.9\% \pm 0.23\% \pm 2.52\% \\ &= \pm 5.65\%\end{aligned} \quad \text{(A14)}$$

The overall tolerance is the sum of the deterministic variation due to the change in line voltage and the change in the output diode forward voltage with temperature, together with the root-sum-square addition of the statistically independent circuit and device variables.

In Equation A14 the $\Delta\%_{LINE}$ term (±2.9%) is the expected change in output voltage for a change of ±90 VAC at 175 VAC, the mid point of the specified input voltage range of 85 VAC to 265 VAC.

Equivalently, stating with the reference as 85 VAC, the output voltage would increase +5.8% (twice 2.9%) when the input increases to 265 VAC.

The analysis above is for a specific example, factors such as diode choice, temperature range and output voltage can result in a larger tolerance. However, for most cases the designer can be confident the overall tolerance will be <±10%.

Note that all of the above tolerances other than R_{FB} and $V_{C(IDCT)}$ are compensated or accounted for in the previous analysis of CC tolerance. The contributions of R_{FB} and $V_{C(IDCT)}$, since they are unit-to-unit tolerances, have a very small influence (<0.1% on the total sum of unit-to-unit tolerances).

Constant Voltage Operation Below Peak Power Point

As the output load reduces from the peak power point, the output voltage will tend to rise due to tracking errors compared to the load terminals. Sources of these include the output cable drop, output diode forward voltage and leakage inductance, which is the dominant cause.

As the load reduces, the primary operating peak current reduces, together with the leakage inductance energy, which reduces the peak charging of C_{CLAMP}. With a primary leakage inductance figure of 50 µH, the output voltage typically rises 40% from full to no-load.

Revision	Notes	Date
A	–	8/02
B	1) Added support for LNK500	4/03

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