

### FEATURES

- Internal MOSFET driver with Integrated High Side
- Uses External Low Side MOSFET
- Adjustable output voltage down to 0.600V
- External Clock Synchronization
- Built in Start/Stop UVLO
- Over Current and Thermal Protection
- Shutdown supply current < 1uA
- Frequency range 100KHz to 750KHz

### APPLICATIONS

- LCD TVs and LCD monitors
- Computer Peripherals
- Portable (Notebook) Computers
- Industrial power supply
- Point of regulation for high performance electronics
- Consumer Electronics
- Audio Power Amplifiers

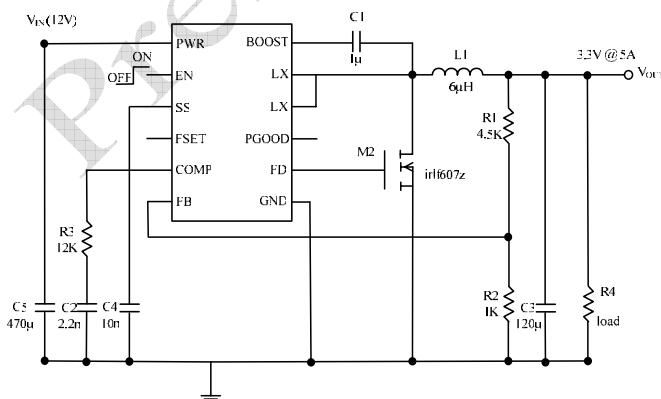
### GENERAL DESCRIPTION

The AMS4106 is a medium output current synchronous buck converter. The high side device is integrated into the device. The AMS4106 provides an adaptive gate drive for the external FET. For low current operation this can be replaced with a Schottky diode allowing asynchronous operation. The part has either a fixed internal present PWM frequency of 250 kHz, or externally adjustable up to 600 kHz, allowing smaller inductors where efficiency is less critical and faster transient response is needed. The part uses current mode control for simple compensation and ease of use with low ESR capacitors. It uses a programmable soft start to reduce inrush current and allow large output capacitors to be used where very low ripple is required. The part has enable pin with virtual zero power in shutdown mode. A power good is provided with open collector to facilitate power ready functions. The part is available in SOIC 16 thermally enhanced packages.

### ORDERING INFORMATION

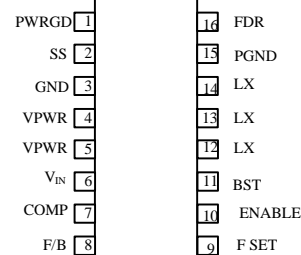
| OUTPUT     | PACKAGE TYPE | TEMP.          |
|------------|--------------|----------------|
| VOLTAGE    | 16 Lead SOIC | RANGE          |
| Adjustable | AMS4106S     | -25°C to 125°C |

### TYPICAL APPLICATION



### PIN CONNECTIONS

#### 16 Lead SOIC (S)



#### Top View

## PIN DESCRIPTION

| AMS4106     |                 |                                                                                                                                                                                                         |
|-------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIN NUMBERS | NAME            | DESCRIPTION                                                                                                                                                                                             |
| 1           | PWRGD           | Power good output. Open collector output. A low on the pin indicates that the output is less than the desired output voltage. There is an internal rising filter on the output of the PWRGD comparator. |
| 2           | SS              | Soft start pin connect a capacitor to GND, to slow the start up.                                                                                                                                        |
| 3           | GND             | Analog ground-internally connected to the sensitive analog ground circuitry.                                                                                                                            |
| 4, 5        | VPWR            | Input supply voltage, 4.5 V to 20 V. Must bypass with a low ESR 10- $\mu$ F ceramic capacitor.                                                                                                          |
| 6           | V <sub>IN</sub> | Input supply voltage, 4.5 V to 20 V powers up the internal circuitry. Must bypass with a low ESR 10- $\mu$ F ceramic capacitor.                                                                         |
| 7           | COMP            | Error amplifier output. Connect frequency compensation network from COMP to GND.                                                                                                                        |
| 8           | F/B             | Input pin of the error comparator.                                                                                                                                                                      |
| 9           | F SET           | External frequency set 100 Khz-750Khz.                                                                                                                                                                  |
| 10          | ENABLE          | Logic enable/disable device function.                                                                                                                                                                   |
| 11          | BST             | Boost voltage for the output stage drive. Connect a capacitor between LX pin and Boost.                                                                                                                 |
| 12, 13, 14  | LX              | Phase node- Connect to external FET and external L-C filter.                                                                                                                                            |
| 15          | PGND            | Power Ground-Noisy internal ground-Return currents from the FDR driver output return through the PGND                                                                                                   |
| 16          | FDR             | Gate drive for low side MOSFET. Connect gate of n-channel MOSFET.                                                                                                                                       |

## ABSOLUTE MAXIMUM RATINGS

|                                     |                |                            |                    |
|-------------------------------------|----------------|----------------------------|--------------------|
| V <sub>IN</sub>                     | -0.3V to 30V   | LX                         | Internally Limited |
| F/B                                 | -0.3 to 8.0V   | FDR (steady state current) | 500 mA             |
| EN                                  | -0.3V to 8.0V  | COMP                       | 3 mA               |
| FSET                                | -0.3V to 4.0V  | FDR (steady state current) | 100 mA             |
| SS                                  | -0.3V to 4.0V  | LX (steady state current)  | 500 mA             |
| BST                                 | VI (PH) + 8.0V | COMP                       | 3 mA               |
| FDR                                 | -0.3V to 8.5V  | SS PWRGD                   | 10 mA              |
| PWRGD                               | 0.3V to 30V    | AGND to PGND               | ±0.3V              |
| COMP                                | 0.3V to 30V    | ESD                        | 2kV                |
| LX                                  | -1.5V to 30V   | Junction Temperature       | +150°C             |
| Lead Temperature 1,6 mm for 10 sec. | 260°C          | Storage Temperature        | -65°C to +150°C    |

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

Electrical Characteristics at T<sub>J</sub> = 25 °C and Vin=12V (unless otherwise noted)

| PARAMETER                                | TEST CONDITIONS                                                 | AMS4106 |       |       | Units |
|------------------------------------------|-----------------------------------------------------------------|---------|-------|-------|-------|
|                                          |                                                                 | Min.    | Typ.  | Max.  |       |
| <b>SUPPLY CURRENT</b>                    |                                                                 |         |       |       |       |
| I <sub>0</sub> Quiescent current         | Operating Current, LX pin open,<br>No external low side MOSFET, |         | 3     | 12    | mA    |
|                                          | Shutdown, EN= 0V                                                |         | 0.5   |       | µA    |
| VIN                                      | Start threshold voltage                                         |         | 4.32  | 4.49  | V     |
|                                          | Stop threshold voltage                                          | 3.69    | 3.97  |       | V     |
|                                          | Hysteresis                                                      |         | 350   |       | mV    |
| <b>REFERENCE SYSTEM ACCURACY</b>         |                                                                 |         |       |       |       |
| Reference voltage                        | T <sub>J</sub> = 25 °C                                          | 0.588   | 0.600 | 0.612 | V     |
|                                          | T <sub>J</sub> = 125 °C                                         |         | 0.600 |       | V     |
| <b>OSCILLATOR (RT PIN)</b>               |                                                                 |         |       |       |       |
| Internally set PWM switching frequency   | F set open                                                      | 200     | 250   | 300   | kHz   |
|                                          | F set to GND                                                    |         |       |       |       |
|                                          | F set to VCC                                                    |         |       |       | kHz   |
| <b>ERROR AMPLIFIER F/B and COMP PINS</b> |                                                                 |         |       |       |       |
| Error amplifier Sink current Running     |                                                                 | 60      | 85    |       | µA    |
| Error amplifier Source current Running   |                                                                 | 1.0     | 98    |       | µA    |
| Error amplifier Source current Start-up  |                                                                 |         | 20    |       | µA    |

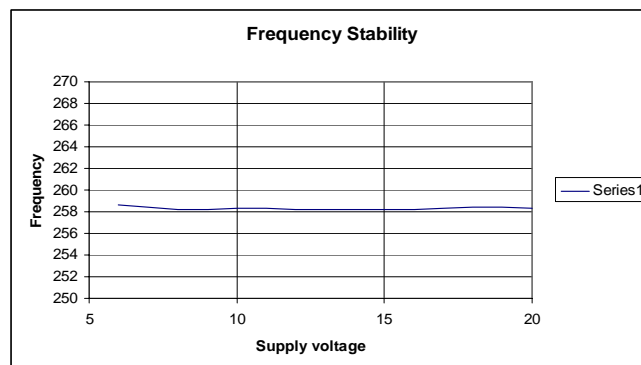
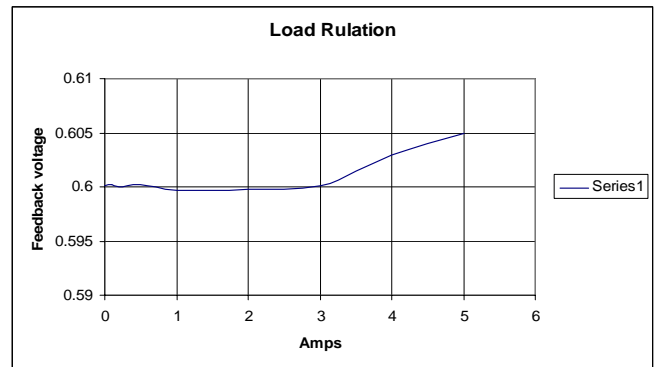
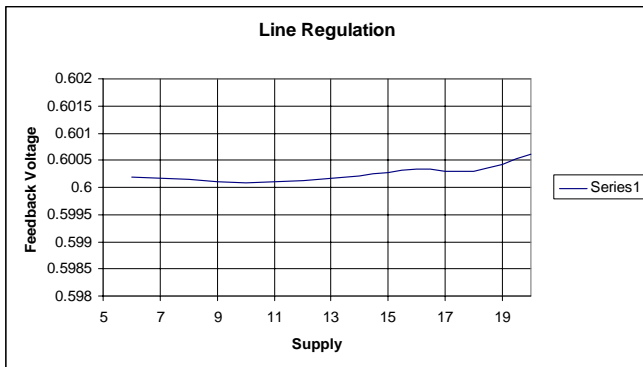
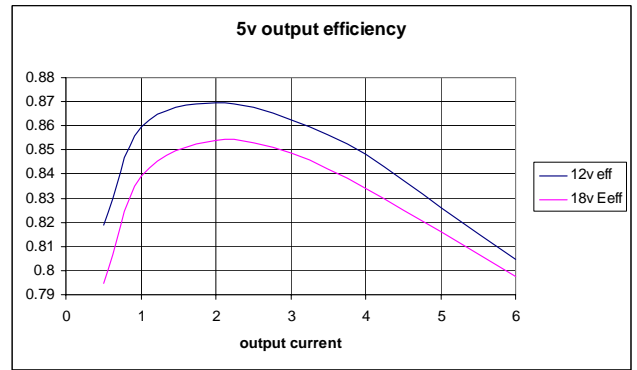
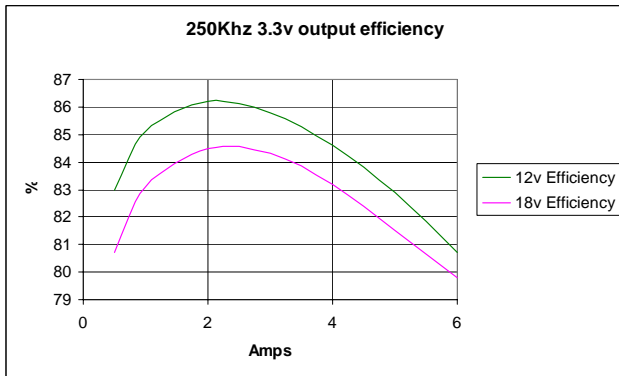
## ELECTRICAL CHARACTERISTICS (continued)

Electrical Characteristics at  $T_J = -40\text{ }^\circ\text{C}$  to  $125\text{ }^\circ\text{C}$  and  $V_{in} = 4.5\text{V}$  (unless otherwise noted)

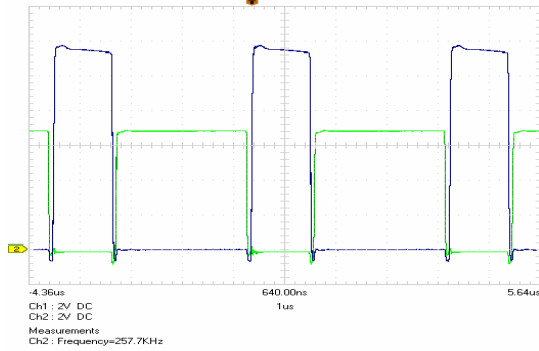
| PARAMETER                                   | TEST CONDITIONS                                                | AMS4106                                                          |       |      | Units            |
|---------------------------------------------|----------------------------------------------------------------|------------------------------------------------------------------|-------|------|------------------|
|                                             |                                                                | Min.                                                             | Typ.  | Max. |                  |
| Soft Start (SS)                             |                                                                |                                                                  | 2.22  |      | $\mu\text{A}$    |
| Internal soft start (10% to 90%)            | f = 250 kHz                                                    |                                                                  | 4.6   |      | ms               |
|                                             | f = 500 kHz                                                    |                                                                  | 2.3   |      |                  |
| <b>POWER GOOD (PWRGD PIN)</b>               |                                                                |                                                                  |       |      |                  |
| Power good threshold                        | Rising voltage                                                 |                                                                  | 95%   |      |                  |
| Rising edge delay                           | f = 250 kHz                                                    |                                                                  | 4     |      | ms               |
|                                             | f = 500 kHz                                                    |                                                                  | 2     |      |                  |
| PWR<br>GD                                   | Output saturation voltage                                      | $I_{\text{sink}} = 1\text{ mA}$ , $V_{in} > 4.5\text{ V}$        | 0.05  |      | V                |
|                                             | Output saturation voltage                                      | $I_{\text{sink}} = 1\text{ }\mu\text{A}$ , $V_{in} = 0\text{ V}$ | 0.075 |      | V                |
|                                             | Open collector leakage                                         | Voltage on PWRGD = 6 V                                           |       | 2    | $\mu\text{A}$    |
| <b>CURRENT LIMIT</b>                        |                                                                |                                                                  |       |      |                  |
| Current limit                               | $V_{in} = 12$                                                  | 6.1                                                              | 6.5   | 7.5  | A                |
| Current limit Hiccup Time                   | f = 500 kHz                                                    |                                                                  | 4.5   |      | ms               |
| <b>THERMAL SHUTDOWN</b>                     |                                                                |                                                                  |       |      |                  |
| Thermal shutdown trip point                 |                                                                |                                                                  | 145   |      | $^\circ\text{C}$ |
| Thermal shutdown hysteresis <sup>(1)</sup>  |                                                                |                                                                  | 10    |      | $^\circ\text{C}$ |
| <b>LOW SIDE EXTERNAL FET DRIVE</b>          |                                                                |                                                                  |       |      |                  |
| Turn on rise time, (10%/90%) <sup>(1)</sup> | $V_{in} = 4.5\text{V}$ , Capacitive load = 1000 pF             |                                                                  | 15    |      | ns               |
|                                             | $V_{in} = 8\text{ V}$ , Capacitive load = 1000 pF              |                                                                  | 12    |      |                  |
| Deadtime <sup>(1)</sup>                     | $V_{in} = 12\text{ V}$                                         |                                                                  | 60    |      | ns               |
| Driver ON resistance                        | $V_{in} = 4.5\text{ V}$ sink/ source                           |                                                                  | 7.5   |      | $\Omega$         |
|                                             | $V_{in} = 12\text{ V}$ sink/ source                            |                                                                  | 5     |      |                  |
| <b>OUTPUT POWER MOSFETS (LX PIN)</b>        |                                                                |                                                                  |       |      |                  |
| Lx node voltage when disabled               | DC conditions and no load, EN = 0 V                            |                                                                  | 0.5   |      | V                |
| Voltage drop, low side FET and diode        | $V_{in} = 4.5\text{ V}$ , $I_{dc} = 100\text{ mA}$             |                                                                  | 1.13  | 1.42 | V                |
|                                             | $V_{in} = 12\text{ V}$ , $I_{dc} = 100\text{ mA}$              |                                                                  | 1.08  | 1.38 |                  |
| $r_{DS(ON)}$ High side power switch         | $V_{in} = 4.5\text{ V}$ , BST-LX = 4.5 V, $I_o = 0.5\text{ A}$ |                                                                  | 60    |      | m $\Omega$       |
|                                             | $V_{in} = 12\text{ V}$ , BST-LX = 8 V, $I_o = 0.5\text{ A}$    |                                                                  | 40    |      |                  |

(1) Specified by design, not production tested.

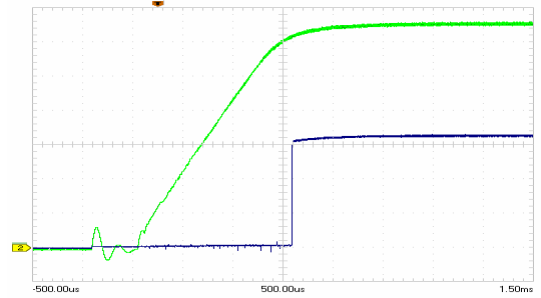
## TYPICAL PERFORMANCE CHARACTERISTICS



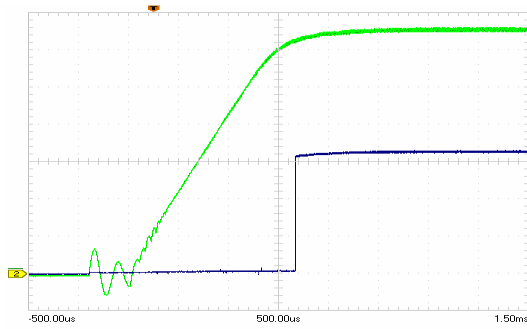
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



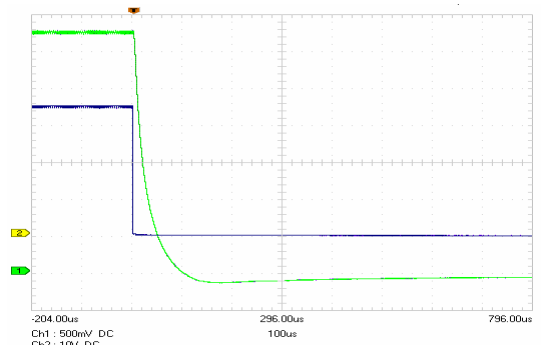
**FIG.1**  
Normal operating waveform, with internal frequency, 12V input and 2A load.



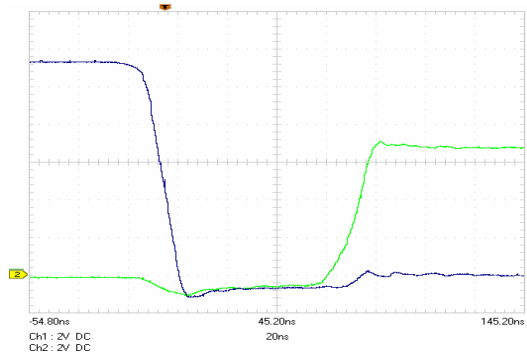
**FIG.2**  
Power good threshold ~95%, 2.5A load start up.



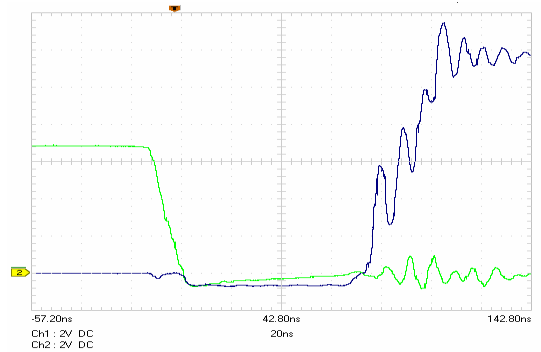
**FIG.3**  
Power good at Light load Start up <10mA



**FIG.4**  
Shutdown

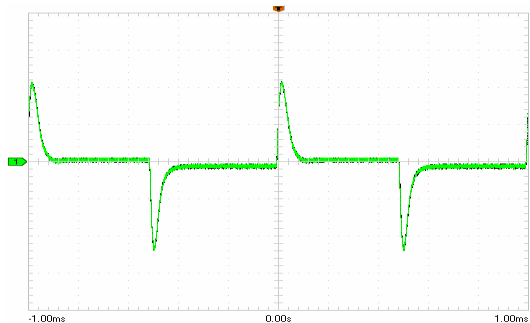


**FIG.5**  
Trailing Edge Non Overlap

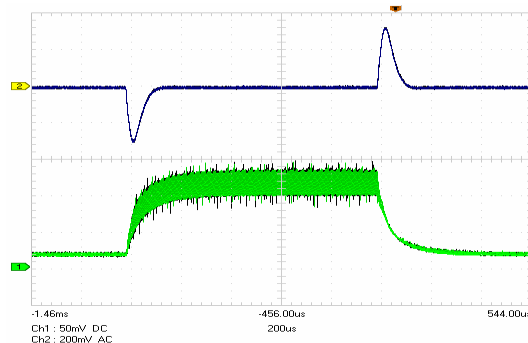


**FIG.6**  
Leading Edge Non Overlap

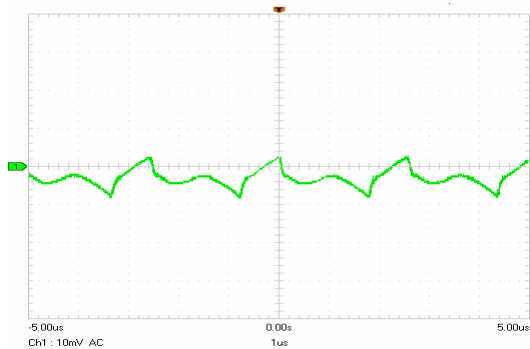
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



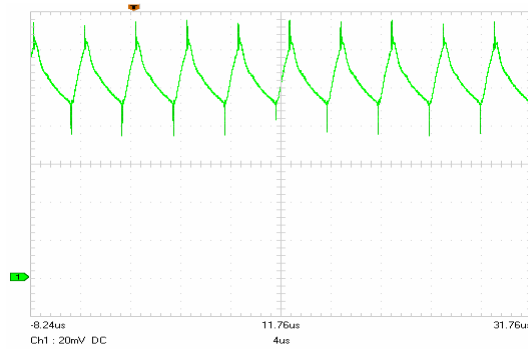
**FIG. 7**  
Load Transient test performance 0.5A to 4A/10  $\mu$ s  
Scale 100mV division, Current/ fall time 10  $\mu$ s



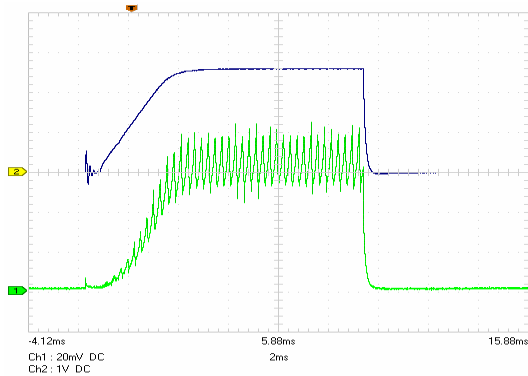
**FIG. 8**  
Supply current through transient event (0.5-4A)  
Current scale is 0.5A per division



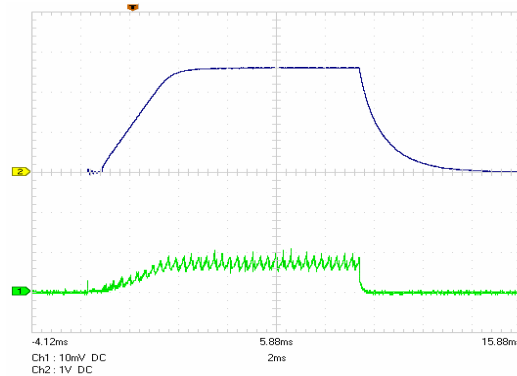
**FIG. 9**  
Output Ripple at 3A Load



**FIG. 10**  
Supply ripple current at 4A (200mA per division)



**FIG. 11**  
Start up current with 2A load  
Current is 200mA per division.



**FIG. 12**  
Input Current during start up and shutdown.

## DETAIL DESCRIPTION and GUIDELINES

### Start up from enable

When the enable is low the part is completely shut down with the nano-amps only of leakage current. When the enable is taken above the turn on threshold it powers up part. There are 2 soft start mechanisms in operation during start up, error amplifier and external. For small output capacitance (ceramic only solutions), the compensation can be used for soft start, and the soft start pin is left open. For situation requiring slower soft start or where large output capacitors are used a separate soft start pin is used. This charges the external capacitor with around 2.2  $\mu\text{A}$  current allowing small ceramic capacitors to be used. When Power good senses the output is almost at its final value the error amplifier current is turned on to its normal running current overriding the startup current.

### Enable connected to Vin

The part initiates its soft start described above at UVLO threshold of around 4.75V.

### PWM frequency

The default is internally set to 250 kHz with the FSET pin left open. Adding a resistor to ground switches it into the external set mode. A 68K resistor to ground gives approximately 250 kHz PWM frequency. Care should be taken to keep the resistor close to the part as pick-up on this pin can cause jitter.

### Over-current shutdown

If over-current is sensed the part shuts down and initiates the soft start sequence providing a hiccup function. This means that shorting the output is non destructive and will run a low supply current. When the output shuts down the low-side FET is turned off giving a tri-state output. This helps prevent negative output voltages being generated in an overload condition where the load significantly reduces (due to system reset etc) as a result of the output voltage failing. Power good is held low during over current.

### Synchronous operation

With an external FET fitted between Phase and ground the parts enters synchronous operation. Gate time is adaptively controlled allowing large freedom in the choice of output FET. For highest performance the lowest gate charge FET typically will give the best overall efficiency. The gate drive features a medium drive capability of around 0.5-1A removing the need series gate resistors for most applications. Due to the fast switching on the phase node it is important that the FET is placed very close to the part with very short paths for both ground and the phase node. Large parasitic inductance can cause large negative spikes on the switch output causing jitter and in severe circumstances potential circuit malfunction.

### Asynchronous operation

A Schottky diode can be used in place of the FET for certain applications, no other changes are required to accommodate this mode. The gate drive pin should be left open. This is at the expense of full load efficiency especially at low output voltage. Transient performance is also reduced.

For applications when light load higher efficiency is required Asynchronous operation is preferred.

For Applications requiring HOT switching Asynchronous operation is preferred preventing unwanted dips on the output supply.

### Duty cycle considerations

For low input output ratios greater than 50% duty cycle the maximum output should be de-rated to reduce package heating and thermal shutdown.

For high input output ratios the maximum frequency is determined by the minimum useable duty cycle, for this part it is around 120ns, shorter duty cycles could cause jitter or pulse skipping. For a 0.8v output and a switching frequency of 500kHz a maximum input voltage of around 14v can be accommodated at light load rising to about 20v at 4A.

### Bootstrap Circuit

To allow operation over a very large range the devices uses an internal boost regulator and internal boost diode. The boost capacitor supplies the output bias current requirements. The regulator is set to the minimum voltage required to give operation at full output current. It is important that the capacitor is large enough to supply the current for the full on time for large duty 1 $\mu\text{F}$  is recommended for short duty cycle < 10% 100nf is suitable. Using a 1 $\mu\text{F}$  boost capacitor for all applications has no detrimental effect. The voltage across the capacitor is small (around 3v) so small ceramic case sizes can be used.



## DETAIL DESCRIPTION and GUIDELINES (continued)

### Reference Circuit

A high precision bandgap is used giving a low TC and good supply rejection. The output is attenuated to give a reference voltage of 0.600V making it suitable for very low output voltage applications.

### COMPENSATION

The converter is of the current mode topology considered simplifying the selection of compensation components. For most voltages this simple formula is a good starting point

$C_{comp} = 15e-9/V_{out}$  for  $L = 10e-6$  and  $C_{out} = 44e-6$

$C_{comp}$  is proportional to the output inductors and output capacitor

$R_{comp} = 18e3/V_{out}$

Output capacitor  $C_{out}$ , is a function of the maximum current and ripple required.

Multiple capacitors may be required to give the optimum ripple and transient response.

The stability is not that critical for varying  $C_{out}$ , however to prevent OCP during fast load transients  $C_{comp}$ , has to be increased in proportion to  $C_{out}$ .

The current gain of the output stage is approximately 6A/volt

The running transconductance output current is

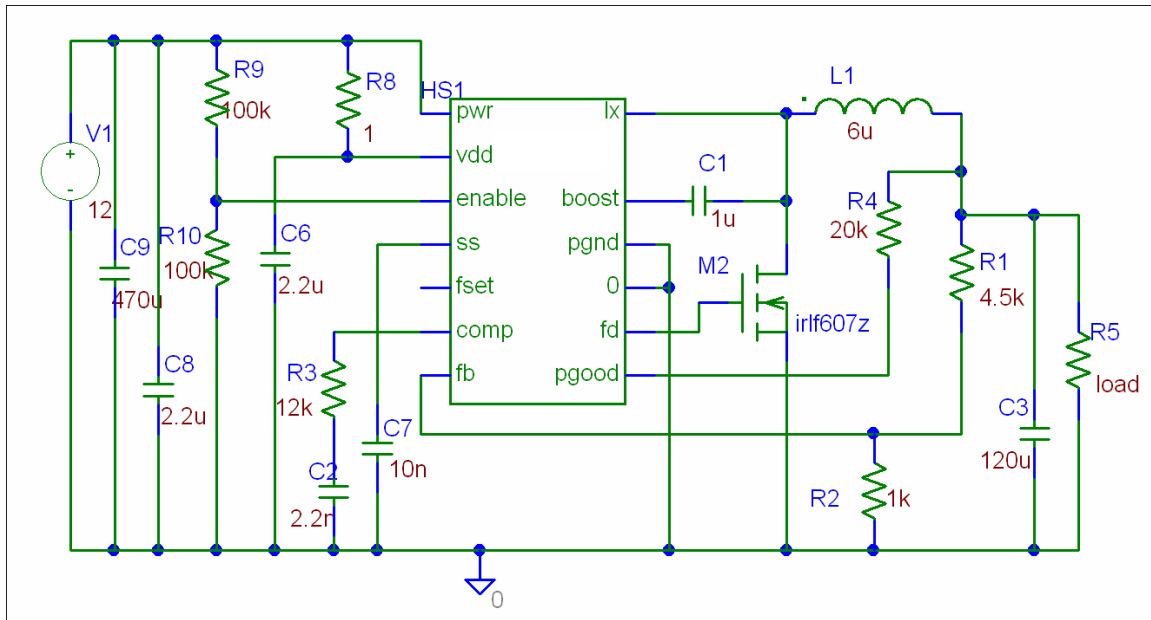
Sourcing current 95  $\mu$ A

Sinking current 85  $\mu$ A

This equates to about 600e-6 mohs

For best transient response each application is unique and these components should only be used as a starting point.

## APPLICATION EXAMPLE



### TESTING CONDITION FOR ABOVE CIRCUIT

Supply Working range

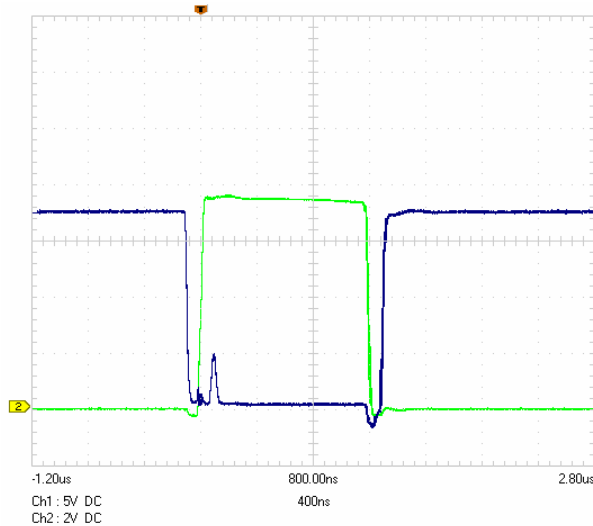
6-20V

Maximum 5A input voltage @23V

Gate drive voltage max 8V

Nominal frequency

258 kHz

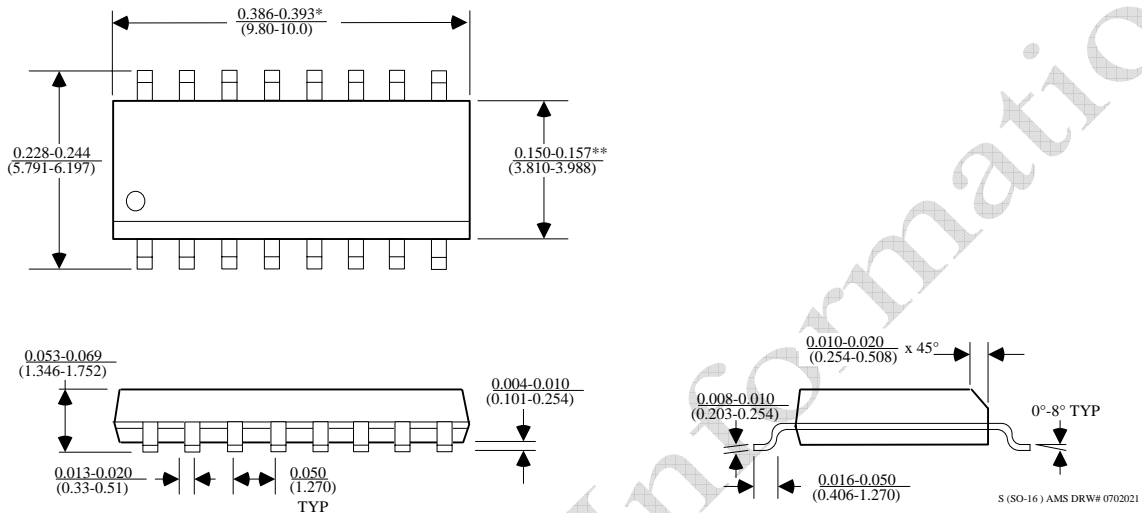


**Gate and output wave form.**

**Small kick on gate drive present at 20V in 5V/4A output**

PACKAGE DIMENSIONS inches (millimeters) unless otherwise noted.

## 16 LEAD SOIC PACKAGE (S)



\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Preliminary Information