HITACHI

2SK1911

Silicon N Channel MOS FET

Application

High speed power switching

Features

- Low on–resistance
- High speed switching
- Low drive current
- 4 V gate drive device can be driven from 5 V source
- Suitable for Switching regulator, DC – DC converter
- Avalanche ratings

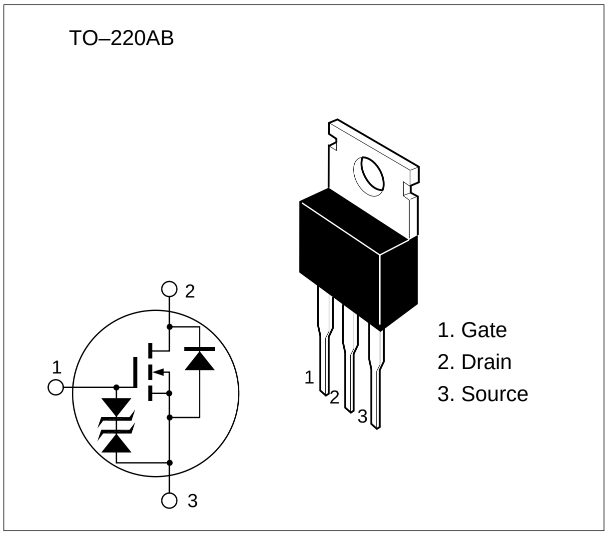


Table 1 Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}^{*}$	160	A
Body–drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP}^{***}	40	A
Avalanche energy	E_{AR}^{***}	137	mJ
Channel dissipation	Pch**	75	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

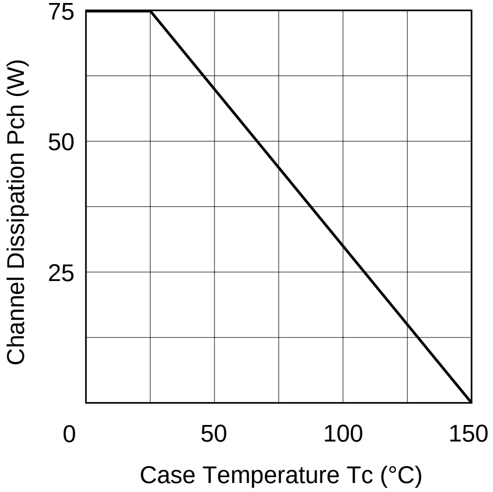
* PW ≤ 10 μs, duty cycle ≤ 1 %
** Value at Tc = 25 °C
*** Value at Tch = 25 °C, Rg ≥ 50 Ω

Table 2 Electrical Characteristics (Ta = 25°C)

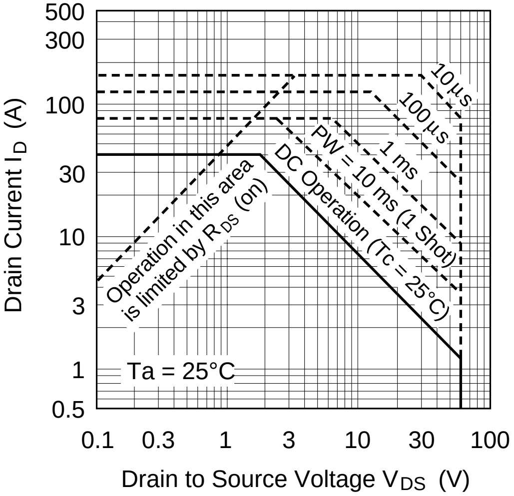
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	I_G = ±200 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	±10	µA	V_{GS} = ±16 V, V_{DS} = 0
Zero gate voltage drain current	I_{DSS}	—	—	250	µA	V_{DS} = 50 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1 mA, V_{DS} = 10 V
Static drain to source on state resistance	$R_{DS(on)}$	—	0.018	0.022	Ω	I_D = 20 A V_{GS} = 10 V *
		—	0.023	0.028	Ω	I_D = 20 A V_{GS} = 4 V *
Forward transfer admittance	$\lvert y_{fs} \rvert$	22	35	—	S	I_D = 20 A V_{DS} = 10 V *
Input capacitance	Ciss	—	3530	—	pF	V_{DS} = 10 V
Output capacitance	Coss	—	1480	—	pF	V_{GS} = 0
Reverse transfer capacitance	Crss	—	300	—	pF	f = 1 MHz
Turn–on delay time	$t_{d(on)}$	—	33	—	ns	I_D = 20 A
Rise time	t_r	—	155	—	ns	V_{GS} = 10 V
Turn–off delay time	$t_{d(off)}$	—	450	—	ns	R_L = 1.5 Ω
Fall time	t_f	—	220	—	ns	
Body–drain diode forward voltage	V_{DF}	—	1.2	—	V	I_F = 40 A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	120	—	ns	I_F = 40 A, V_{GS} = 0, diF / dt = 50 A / µs

* Pulse Test

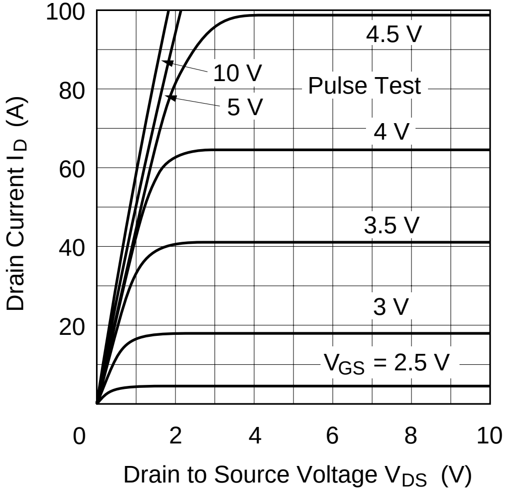
Power vs. Temperature Derating



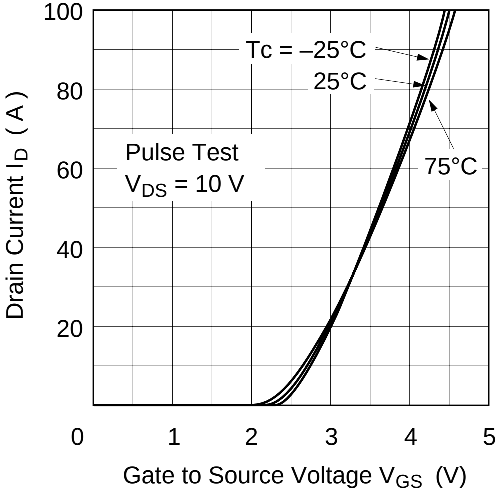
Maximum Safe Operation Area



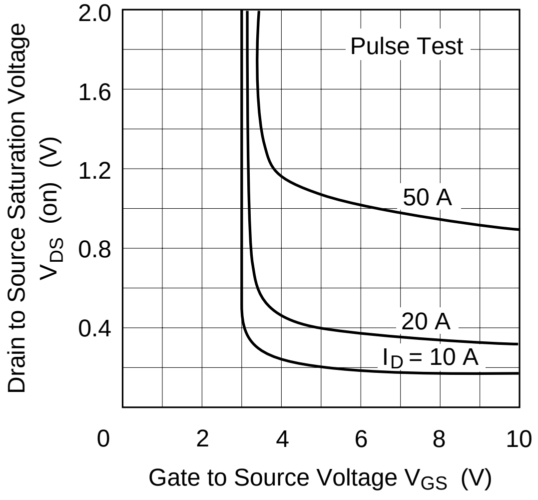
Typical Output Characteristics



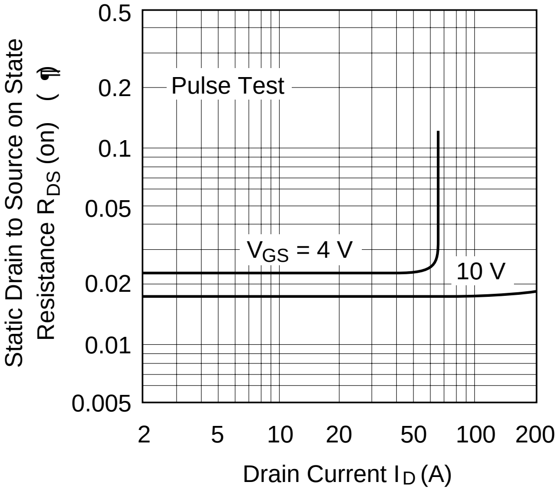
Typical Transfer Characteristics



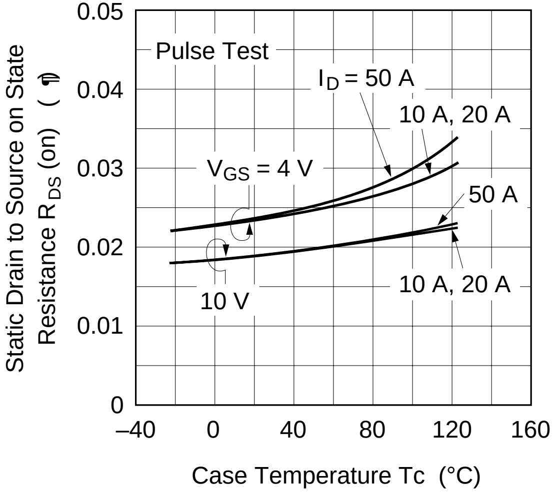
Drain to Source Saturation Voltage vs. Gate to Source Voltage



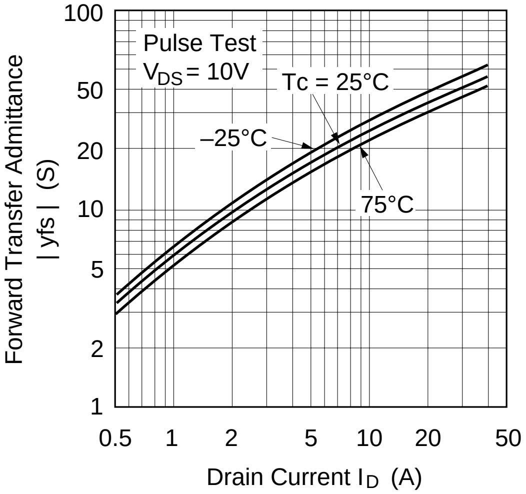
Static Drain to Source on State Resistance vs. Drain Current



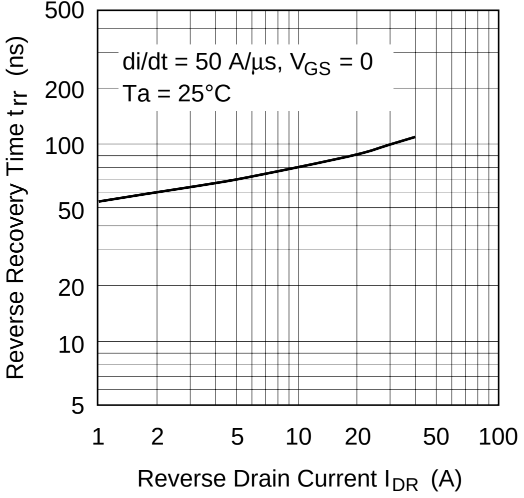
Static Drain to Source on State Resistance vs. Temperature



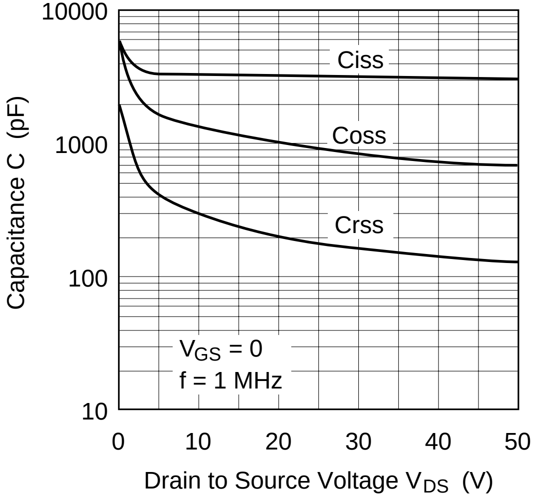
Forward Transfer Admittance vs. Drain Current



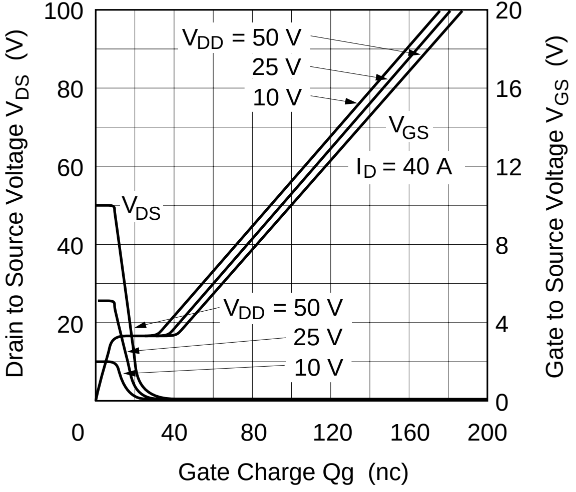
Body to Drain Diode Reverse Recovery Time



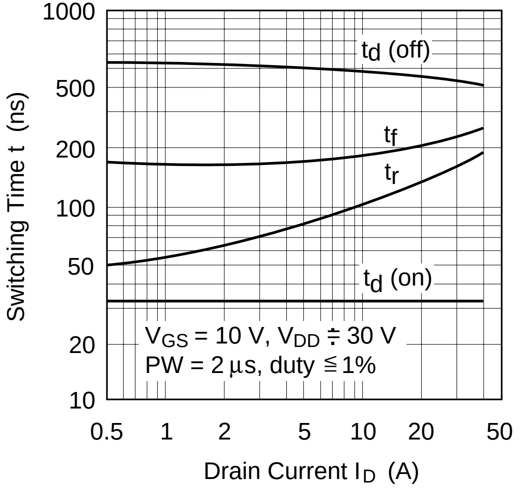
Typical Capacitance vs. Drain to Source Voltage



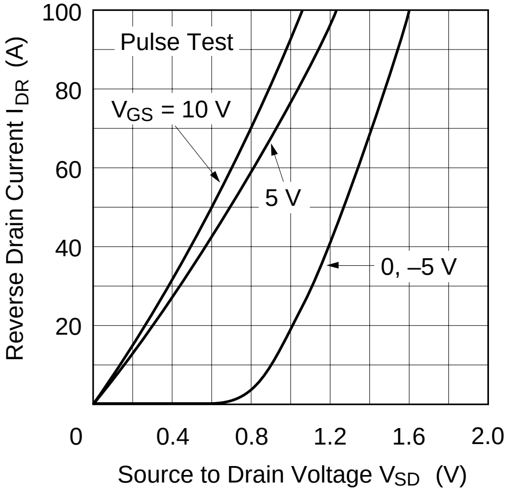
Dynamic Input Characteristics



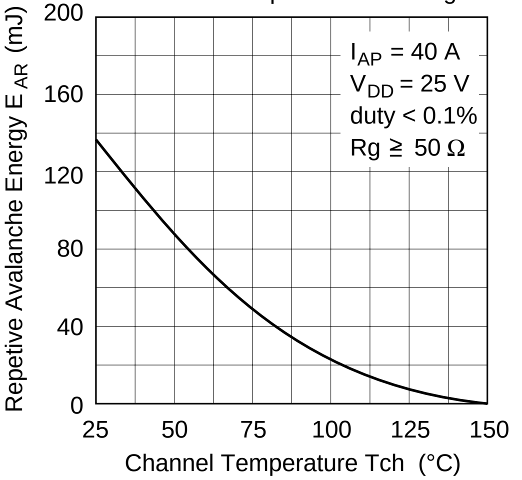
Switching Characteristics



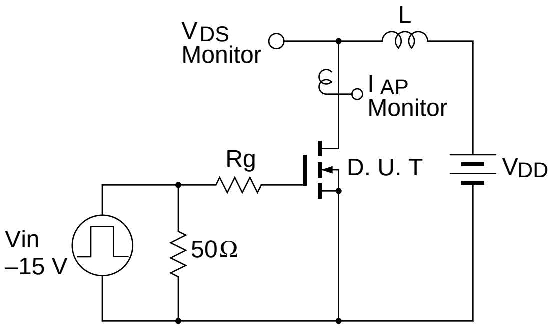
Reverse Drain Current vs. Source to Drain Voltage



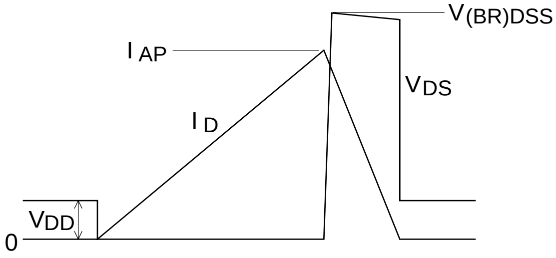
Maximum Avalanche Energy vs. Channel Temperature Derating



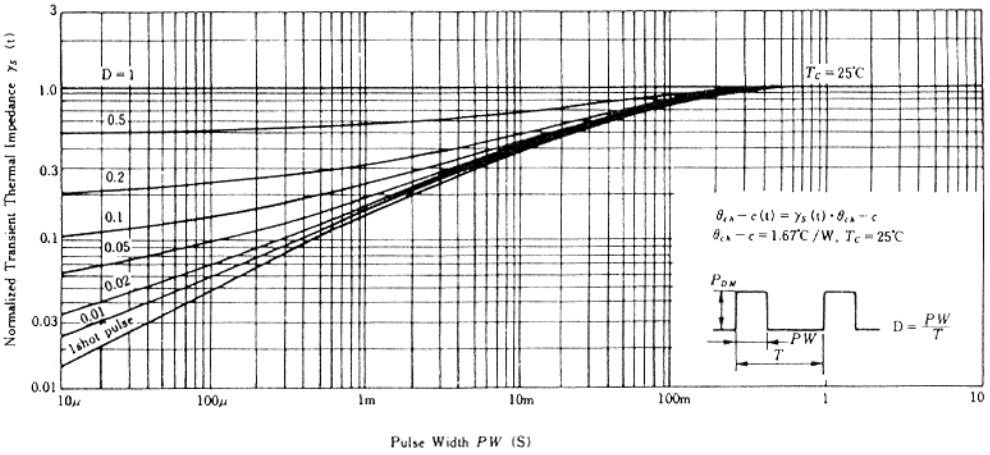
Avalanche Test Circuit and Waveform



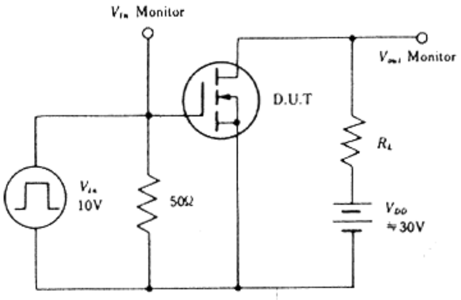
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^{2} \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



NORMALIZED TRANSIENT THERMAL IMPEDANCE VS. PULSE WIDTH



SWITCHING TIME TEST CIRCUIT



WAVEFORMS