

4M-BIT CMOS STATIC RAM 256K-WORD BY 16-BIT EXTENDED TEMPERATURE OPERATION

Description

The μ PD444012A-X is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

The μ PD444012A-X has two chip enable pins (/CE1, CE2) to extend the capacity.

The μ PD444012A-X is packed in 48-pin plastic TSOP (I) (Normal bent).

Features

- 262,144 words by 16 bits organization
- Fast access time: 55, 70, 85, 100, 120, 150 ns (MAX.)
- Byte data control: /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
(B version: $V_{CC} = 2.7$ to 3.6 V, C version: $V_{CC} = 2.2$ to 3.6 V, D version: $V_{CC} = 1.8$ to 3.6 V)
- Low V_{CC} data retention: 1.0 V (MIN.)
- Operating ambient temperature: $T_A = -25$ to $+85^\circ\text{C}$
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply Voltage V	Operating ambient temperature $^\circ\text{C}$	Supply current		
				At operating mA (MAX.)	At standby μA (MAX.)	At data retention μA (MAX.)
μ PD444012A-BxxX	55, 70, 85, 100	2.7 to 3.6	-25 to +85	40 ^{Note 1}	7	3
μ PD444012A-CxxX	70, 85, 100, 120	2.2 to 3.6		40		
μ PD444012A-DxxX ^{Note 2}	100, 120, 150	1.8 to 3.6				

Note 1. Cycle time ≥ 70 ns. μ PD444012A-B55X : 50 mA

2. Under development

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Ordering Information

Part number	Package	Access time ns (MAX.)	Operating supply voltage V	Operating temperature °C	Remark
μPD444012AGY-B55X-MJH	48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)	55	2.7 to 3.6	−25 to +85	B version
μPD444012AGY-B70X-MJH		70			
μPD444012AGY-B85X-MJH		85			
μPD444012AGY-B10X-MJH		100			
μPD444012AGY-C70X-MJH		70	2.2 to 3.6		C version
μPD444012AGY-C85X-MJH		85			
μPD444012AGY-C10X-MJH		100			
μPD444012AGY-C12X-MJH		120			
μPD444012AGY-D10X-MJH ^{Note}		100	1.8 to 3.6		D version
μPD444012AGY-D12X-MJH ^{Note}		120			
μPD444012AGY-D15X-MJH ^{Note}		150			

Note Under development

Pin Configuration (Marking Side)

/xxx indicates active low signal.

48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

[μPD444012AGY-BxxX-MJH]

[μPD444012AGY-CxxX-MJH]

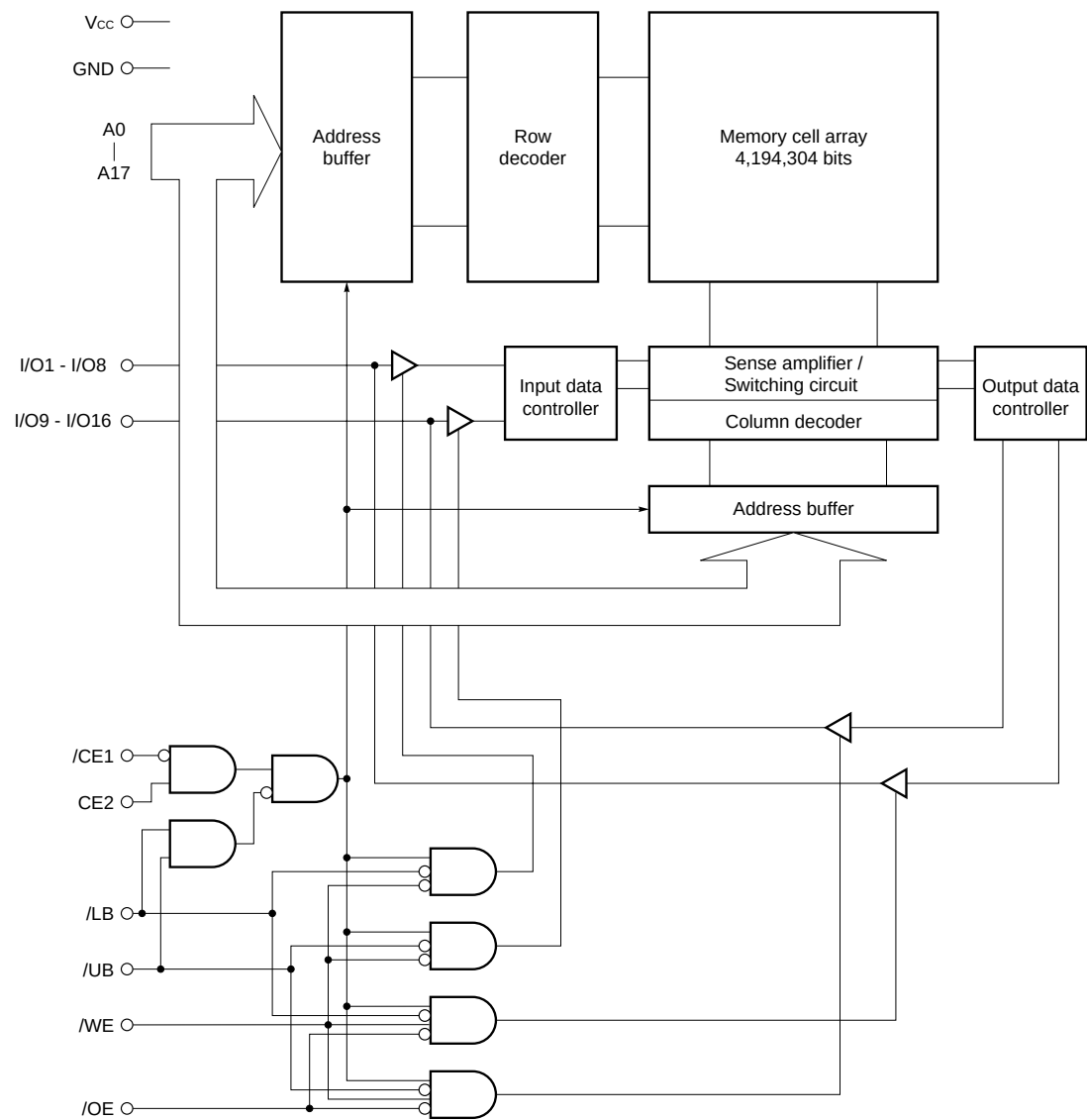
[μPD444012AGY-DxxX-MJH]



- A0 - A17 : Address inputs
- I/O1 - I/O16 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- Vcc : Power supply
- GND : Ground
- NC : No Connection

Remark Refer to **Package Drawing** for the 1-pin index mark.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O1 - I/O8	I/O9 - I/O16	
H	x	x	x	x	x	Not selected	High impedance	High impedance	I _{SB}
x	L	x	x	x	x		High impedance	High impedance	
L	H	H	H	x	x	Output disable	High impedance	High impedance	I _{CCA}
		L	H	L	L	Word read	D _{OUT}	D _{OUT}	
				L	H	Lower byte read	D _{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D _{OUT}	
		x	L	L	L	Word write	D _{IN}	D _{IN}	
				L	H	Lower byte write	D _{IN}	High impedance	
				H	L	Upper byte write	High impedance	D _{IN}	
x	x	x	x	H	H	Not selected	High impedance	High impedance	I _{SB}

Remark x : V_{IH} or V_{IL}

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		-0.5^{Note} to +4.0	V
Input / Output voltage	V_T		-0.5^{Note} to $V_{CC} + 0.4$ (4.0 V MAX.)	V
Operating ambient temperature	T_A		-25 to +85	°C
Storage temperature	T_{stg}		-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μ PD444012A-BxxX		μ PD444012A-CxxX		μ PD444012A-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V_{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V_{IH}	$2.7 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$	2.4	$V_{CC}+0.4$	2.4	$V_{CC}+0.4$	2.4	$V_{CC}+0.4$	V
		$2.2 \text{ V} \leq V_{CC} < 2.7 \text{ V}$	—	—	2.0	$V_{CC}+0.3$	2.0	$V_{CC}+0.3$	
		$1.8 \text{ V} \leq V_{CC} < 2.2 \text{ V}$	—	—	—	—	1.6	$V_{CC}+0.2$	
Low level input voltage	V_{IL}		-0.3^{Note}	+0.5	-0.3^{Note}	+0.3	-0.3^{Note}	+0.2	V
Operating ambient temperature	T_A		-25	+85	-25	+85	-25	+85	°C

Note -1.5 V (MIN.) (Pulse width: 30 ns)

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	$V_{IN} = 0 \text{ V}$			8	pF
Input / Output capacitance	$C_{I/O}$	$V_{I/O} = 0 \text{ V}$			10	pF

Remarks 1. V_{IN} : Input voltage

$V_{I/O}$: Input / Output voltage

2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)(1/2)

Parameter	Symbol	Test condition		V _{CC} ≥ 2.7 V			Unit
				μPD444012A-BxxX			
				MIN.	TYP.	MAX.	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}		−1.0		+1.0	μA
I/O leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , /CE1 = V _{IH} or CE2 = V _{IL} or /WE = V _{IL} or /OE = V _{IH}		−1.0		+1.0	μA
Operating supply current	I _{CCA1}	/CE1 = V _{IL} , CE2 = V _{IH} ,	Cycle time = 55 ns		−	50	mA
		Minimum cycle time, I _{I/O} = 0 mA	Cycle time ≥ 70 ns		−	40	
	I _{CCA2}	/CE1 = V _{IL} , CE2 = V _{IH} , I _{I/O} = 0 mA Cycle time = ∞			−	10	
	I _{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V _{CC} − 0.2 V, Cycle time = 1 μs, I _{I/O} = 0 mA, V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} − 0.2 V			−	8	
Standby supply current	I _{SB}	/CE1 = V _{IH} or CE2 = V _{IL} or /LB = /UB = V _{IH}			−	0.6	mA
	I _{SB1} I _{SB2} I _{SB3}	/CE1 ≥ V _{CC} − 0.2 V, CE2 ≥ V _{CC} − 0.2 V			0.5	7	μA
		CE2 ≤ 0.2 V			0.5	7	
		/LB = /UB ≥ V _{CC} − 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} − 0.2 V			0.5	7	
High level output voltage	V _{OH}	I _{OH} = −0.5 mA		2.4			V
Low level output voltage	V _{OL}	I _{OL} = 1.0 mA				0.4	V

Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

2. These DC characteristics are in common regardless of access time.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)(2/2)

Parameter	Symbol	Test condition	V _{CC} ≥ 2.2 V			V _{CC} ≥ 1.8 V			Unit
			μPD444012A-CxxX			μPD444012A-DxxX			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	−1.0		+1.0	−1.0		+1.0	μA
I/O leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , /CE1 = V _{IH} or CE2 = V _{IL} or /WE = V _{IL} or /OE = V _{IH}	−1.0		+1.0	−1.0		+1.0	μA
Operating supply current	I _{CCA1}	/CE1 = V _{IL} , CE2 = V _{IH} ,		−	40		−	40	mA
		Minimum cycle time, V _{CC} ≤ 2.7 V		−	38		−	38	
		I _{I/O} = 0 mA, V _{CC} ≤ 2.2 V		−	−		−	35	
	I _{CCA2}	/CE1 = V _{IL} , CE2 = V _{IH} ,		−	10		−	10	
		I _{I/O} = 0 mA, V _{CC} ≤ 2.7 V		−	8		−	8	
		Cycle time = ∞, V _{CC} ≤ 2.2 V		−	−		−	6	
	I _{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V _{CC} − 0.2 V, Cycle time = 1 μs, I _{I/O} = 0 mA,		−	8		−	8	
		V _{IL} ≤ 0.2 V, V _{CC} ≤ 2.7 V		−	6		−	6	
		V _{IH} ≥ V _{CC} − 0.2 V, V _{CC} ≤ 2.2 V		−	−		−	6	
	Standby supply current	I _{SB}	/CE1 = V _{IH} or CE2 = V _{IL} or /LB = /UB = V _{IH}		−	0.6		−	
V _{CC} ≤ 2.7 V				−	0.6		−	0.6	
V _{CC} ≤ 2.2 V				−	−		−	0.6	
I _{SB1}		/CE1 ≥ V _{CC} − 0.2 V, CE2 ≥ V _{CC} − 0.2 V		0.5	7		0.5	7	μA
		V _{CC} ≤ 2.7 V		0.4	6		0.4	6	
		V _{CC} ≤ 2.2 V		−	−		0.3	5	
I _{SB2}		CE2 ≤ 0.2 V		0.5	7		0.5	7	
		V _{CC} ≤ 2.7 V		0.4	6		0.4	6	
		V _{CC} ≤ 2.2 V		−	−		0.3	5	
I _{SB3}		/LB = /UB ≥ V _{CC} − 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} − 0.2 V		0.5	7		0.5	7	
		V _{CC} ≤ 2.7 V		0.4	6		0.4	6	
		V _{CC} ≤ 2.2 V		−	−		0.3	5	
High level output voltage	V _{OH}	I _{OH} = −0.5 mA	2.4			2.4			V
		V _{CC} ≤ 2.7 V	1.8			1.8			
		V _{CC} ≤ 2.2 V	−			1.5			
Low level output voltage	V _{OL}	I _{OL} = 1.0 mA			0.4			0.4	V

Remarks 1. V_{IN} : Input voltage

V_{I/O} : Input / Output voltage

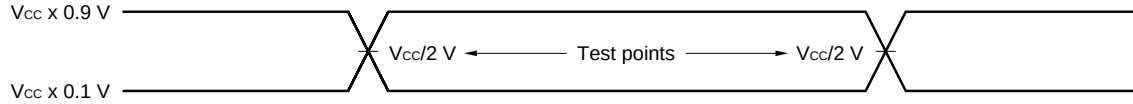
2. These DC characteristics are in common regardless of access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

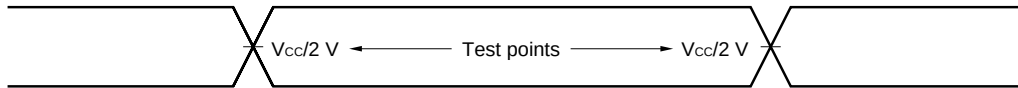
AC Test Conditions

[μPD444012A-B55X, μPD444012A-B70X, μPD444012A-B85X, μPD444012A-B10X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

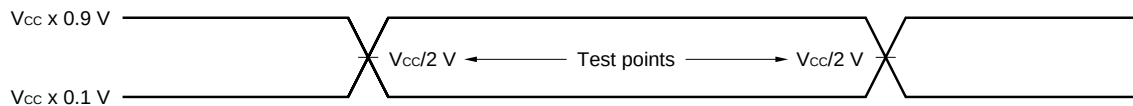


Output Load

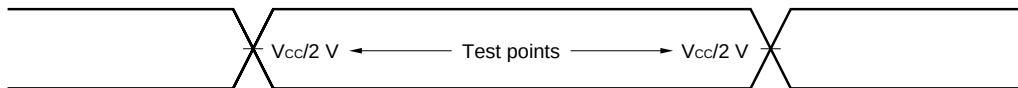
1TTL + 50 pF

[μPD444012A-C70X, μPD444012A-C85X, μPD444012A-C10X, μPD444012A-C12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

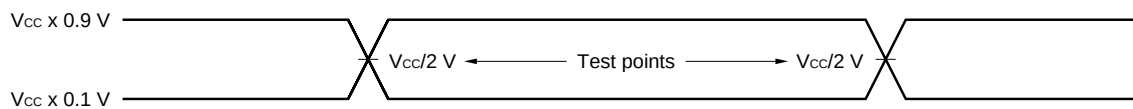


Output Load

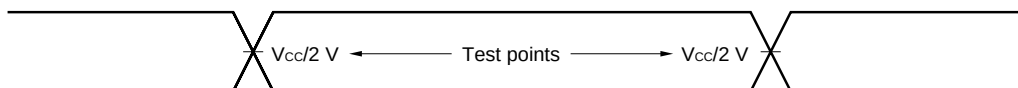
1TTL + 30 pF

[μPD444012A-D10X, μPD444012A-D12X, μPD444012A-D15X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

Read Cycle (1/3) (B version)

Parameter	Symbol	V _{CC} ≥ 2.7 V								Unit	Condition
		μPD444012A -B55X		μPD444012A -B70X		μPD444012A -B85X		μPD444012A -B10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	55		70		85		100		ns	Note 1
Address access time	t _{AA}		55		70		85		100	ns	
/CE1 access time	t _{CO1}		55		70		85		100	ns	
CE2 access time	t _{CO2}		55		70		85		100	ns	
/OE to output valid	t _{OE}		30		35		40		50	ns	
/LB, /UB to output valid	t _{BA}		55		70		85		100	ns	
Output hold from address change	t _{OH}	10		10		10		10		ns	Note 2
/CE1 to output in low impedance	t _{LZ1}	10		10		10		10		ns	
CE2 to output in low impedance	t _{LZ2}	10		10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	0		0		0		0		ns	
/LB, /UB to output in low impedance	t _{BLZ}	10		10		10		10		ns	
/CE1 to output in high impedance	t _{HZ1}		20		25		30		35	ns	
CE2 to output in high impedance	t _{HZ2}		20		25		30		35	ns	
/OE to output in high impedance	t _{OHZ}		20		25		30		35	ns	
/LB, /UB to output in high impedance	t _{BHZ}		20		25		30		35	ns	

Notes 1. The output load is 1TTL + 50 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle (2/3) (C version)

Parameter	Symbol	V _{CC} ≥ 2.2 V								Unit	Condition
		μPD444012A -C70X		μPD444012A -C85X		μPD444012A -C10X		μPD444012A -C12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	70		85		100		120		ns	Note 1
Address access time	t _{AA}		70		85		100		120	ns	
/CE1 access time	t _{CO1}		70		85		100		120	ns	
CE2 access time	t _{CO2}		70		85		100		120	ns	
/OE to output valid	t _{OE}		35		40		50		60	ns	
/LB, /UB to output valid	t _{BA}		70		85		100		120	ns	
Output hold from address change	t _{OH}	10		10		10		10		ns	Note 2
/CE1 to output in low impedance	t _{LZ1}	10		10		10		10		ns	
CE2 to output in low impedance	t _{LZ2}	10		10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	0		0		0		0		ns	
/LB, /UB to output in low impedance	t _{BLZ}	10		10		10		10		ns	
/CE1 to output in high impedance	t _{HZ1}		25		30		35		40	ns	
CE2 to output in high impedance	t _{HZ2}		25		30		35		40	ns	
/OE to output in high impedance	t _{OHZ}		25		30		35		40	ns	
/LB, /UB to output in high impedance	t _{BHZ}		25		30		35		40	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

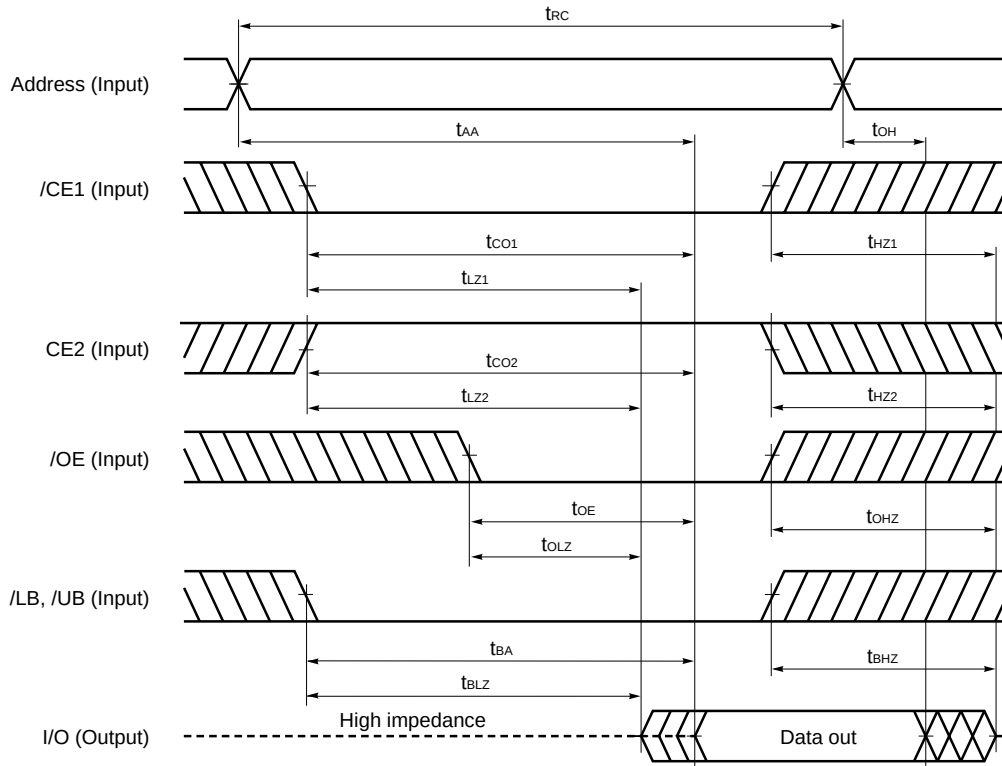
Read Cycle (3/3) (D version)

Parameter	Symbol	V _{CC} ≥ 1.8 V						Unit	Condition
		μPD444012A -D10X		μPD444012A -D12X		μPD444012A -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	100		120		150		ns	
Address access time	t _{AA}		100		120		150	ns	Note 1
/CE1 access time	t _{CO1}		100		120		150	ns	
CE2 access time	t _{CO2}		100		120		150	ns	
/OE to output valid	t _{OE}		50		60		70	ns	
/LB, /UB to output valid	t _{BA}		100		120		150	ns	
Output hold from address change	t _{OH}	10		10		10		ns	
/CE1 to output in low impedance	t _{LZ1}	10		10		10		ns	Note 2
CE2 to output in low impedance	t _{LZ2}	10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	0		0		0		ns	
/LB, /UB to output in low impedance	t _{BLZ}	10		10		10		ns	
/CE1 to output in high impedance	t _{HZ1}		35		40		50	ns	
CE2 to output in high impedance	t _{HZ2}		35		40		50	ns	
/OE to output in high impedance	t _{OHZ}		35		40		50	ns	
/LB, /UB to output in high impedance	t _{BHZ}		35		40		50	ns	

Notes 1. The output load is 1TTL + 30 pF.

2. The output load is 1TTL + 5 pF.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

Write Cycle (1/3) (B version)

Parameter	Symbol	V _{CC} ≥ 2.7 V								Unit	Condition
		μPD444012A -B55X		μPD444012A -B70X		μPD444012A -B85X		μPD444012A -B10X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	55		70		85		100		ns	
/CE1 to end of write	t _{CW1}	50		55		70		80		ns	
CE2 to end of write	t _{CW2}	50		55		70		80		ns	
/LB, /UB to end of write	t _{BW}	50		55		70		80		ns	
Address valid to end of write	t _{AW}	50		55		70		80		ns	
Address setup time	t _{AS}	0		0		0		0		ns	
Write pulse width	t _{WP}	45		50		55		60		ns	
Write recovery time	t _{WR}	0		0		0		0		ns	
Data valid to end of write	t _{DW}	25		30		35		40		ns	
Data hold time	t _{DH}	0		0		0		0		ns	
/WE to output in high impedance	t _{WHZ}		20		25		30		35	ns	Note
Output active from end of write	t _{OW}	5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Write Cycle (2/3) (C version)

Parameter	Symbol	V _{CC} ≥ 2.2 V								Unit	Condition
		μPD444012A -C70X		μPD444012A -C85X		μPD444012A -C10X		μPD444012A -C12X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	70		85		100		120		ns	
/CE1 to end of write	t _{CW1}	55		70		80		100		ns	
CE2 to end of write	t _{CW2}	55		70		80		100		ns	
/LB, /UB to end of write	t _{BW}	55		70		80		100		ns	
Address valid to end of write	t _{AW}	55		70		80		100		ns	
Address setup time	t _{AS}	0		0		0		0		ns	
Write pulse width	t _{WP}	50		55		60		85		ns	
Write recovery time	t _{WR}	0		0		0		0		ns	
Data valid to end of write	t _{DW}	30		35		40		60		ns	
Data hold time	t _{DH}	0		0		0		0		ns	
/WE to output in high impedance	t _{WHZ}		25		30		35		40	ns	Note
Output active from end of write	t _{OW}	5		5		5		5		ns	

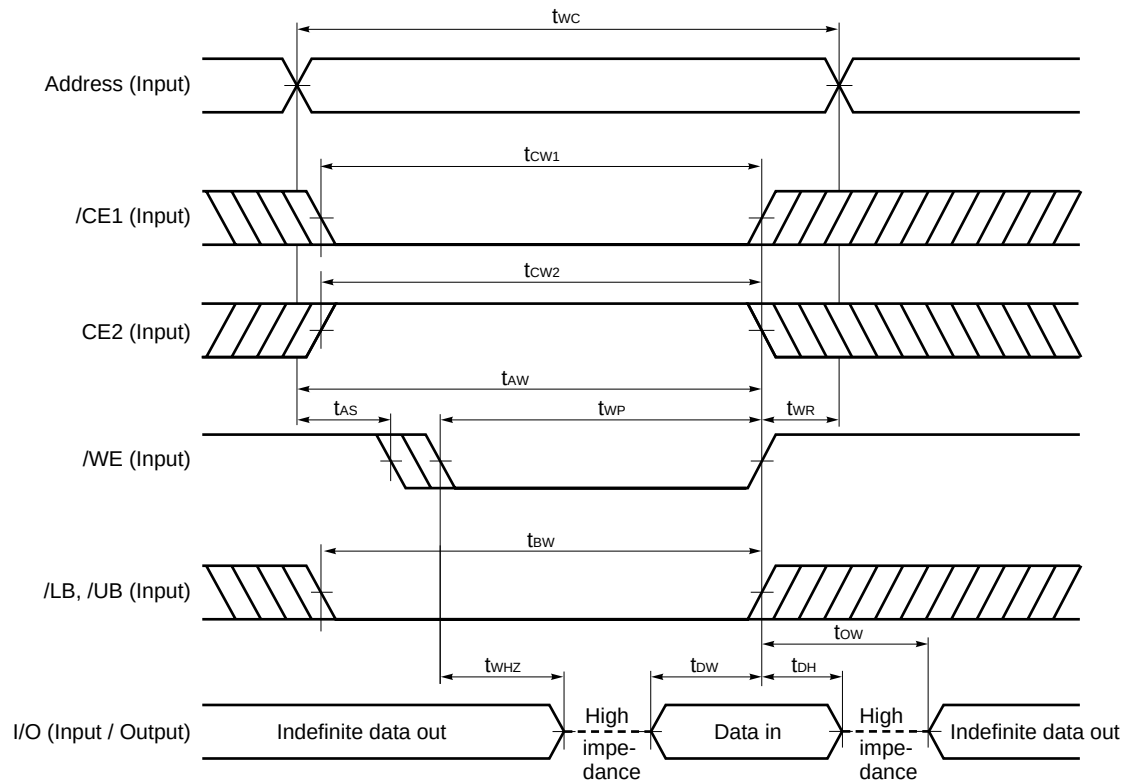
Note The output load is 1TTL + 5 pF.

Write Cycle (3/3) (D version)

Parameter	Symbol	V _{CC} ≥ 1.8 V						Unit	Condition
		μPD444012A -D10X		μPD444012A -D12X		μPD444012A -D15X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{WC}	100		120		150		ns	
/CE1 to end of write	t _{CW1}	80		100		120		ns	
CE2 to end of write	t _{CW2}	80		100		120		ns	
/LB, /UB to end of write	t _{BW}	80		100		120		ns	
Address valid to end of write	t _{AW}	80		100		120		ns	
Address setup time	t _{AS}	0		0		0		ns	
Write pulse width	t _{WP}	60		85		100		ns	
Write recovery time	t _{WR}	0		0		0		ns	
Data valid to end of write	t _{DW}	40		60		80		ns	
Data hold time	t _{DH}	0		0		0		ns	
/WE to output in high impedance	t _{WHZ}		35		40		50	ns	Note
Output active from end of write	t _{OW}	5		5		5		ns	

Note The output load is 1TTL + 5 pF.

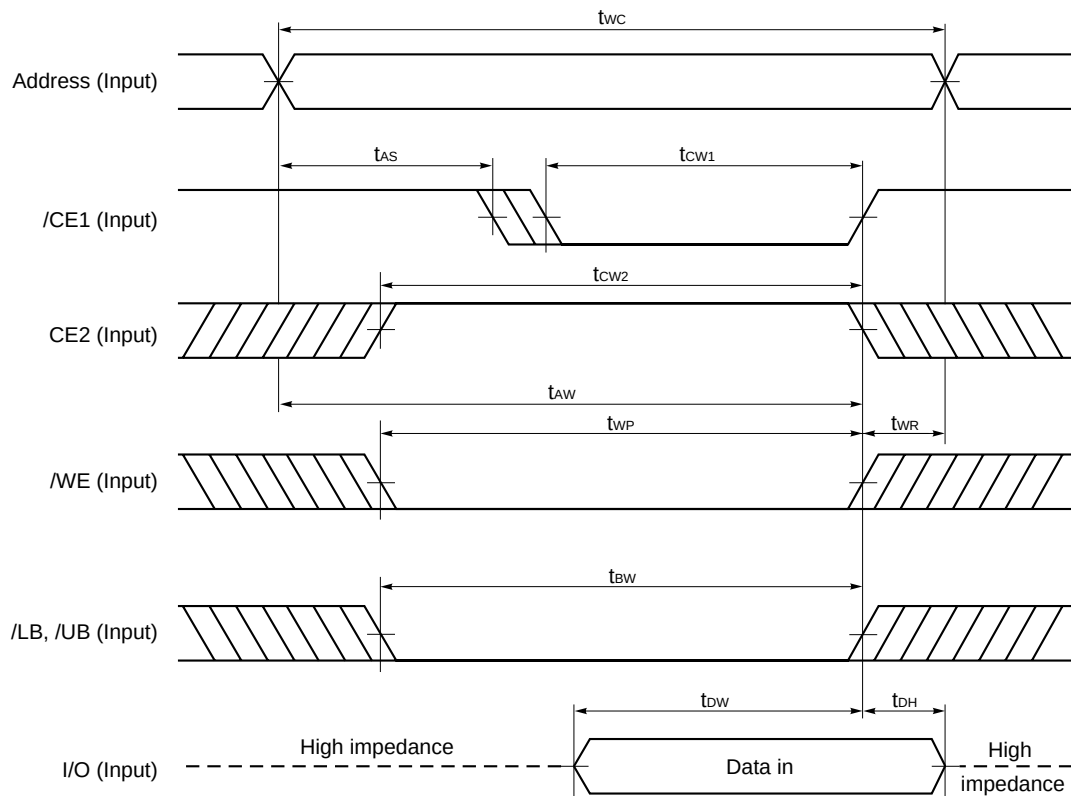
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.
 2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
 3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

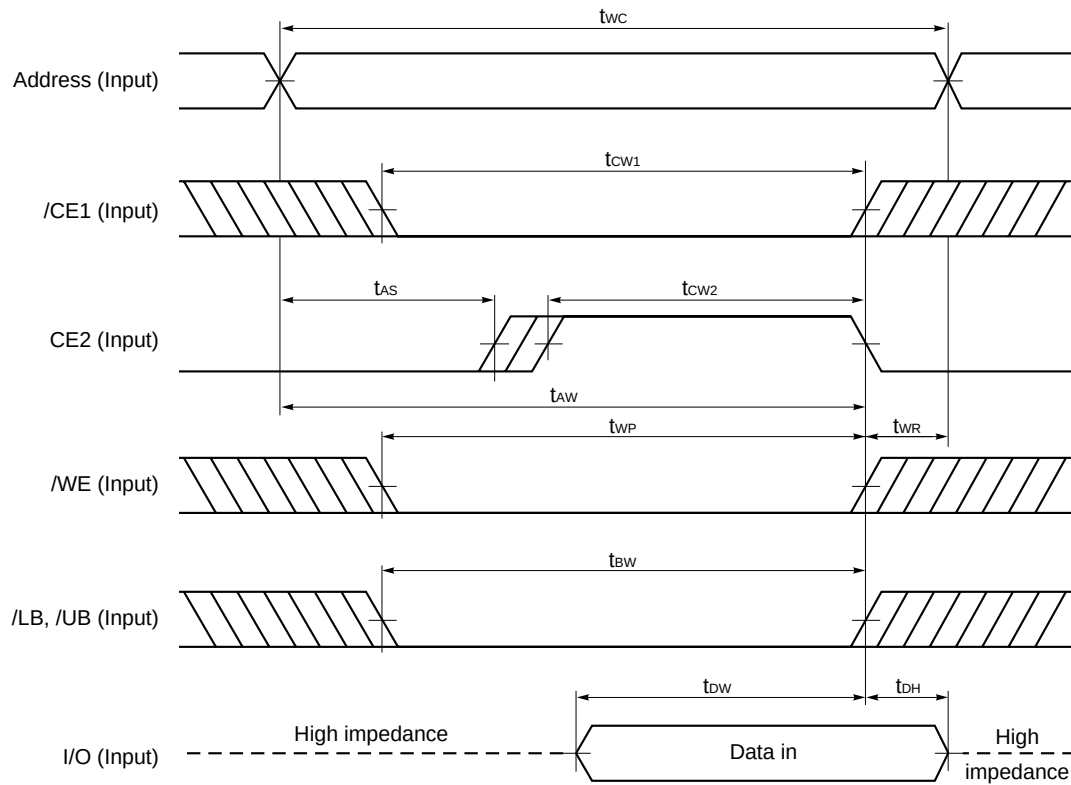
Write Cycle Timing Chart 2 (/CE1 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

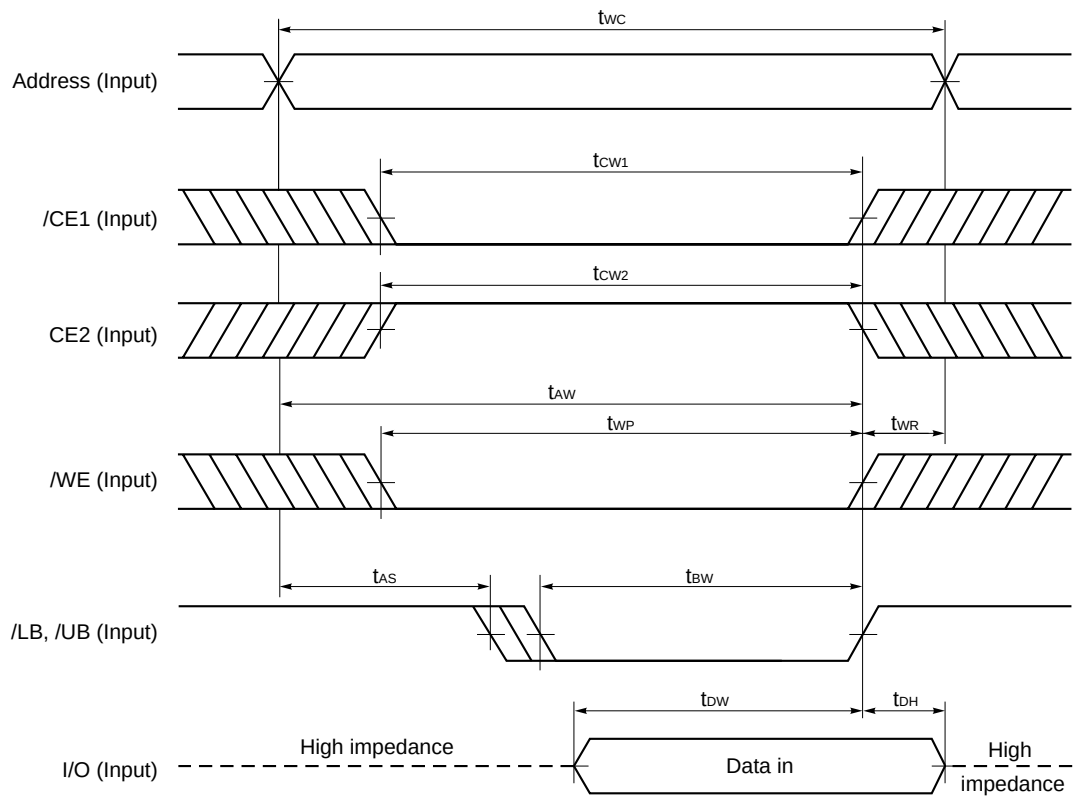
Write Cycle Timing Chart 3 (CE2 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. Do not input data to the I/O pins while they are in the output state.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

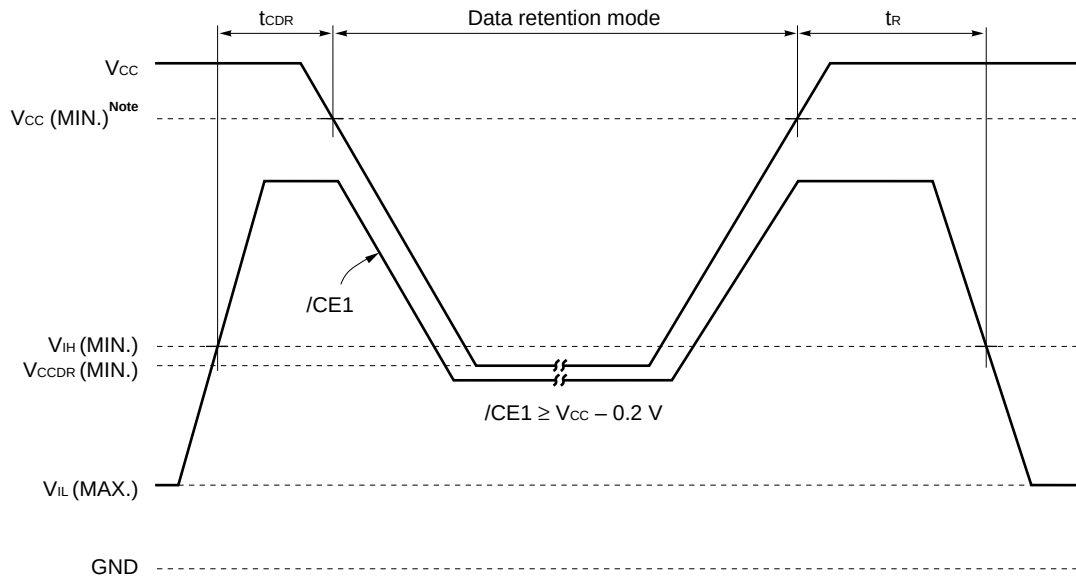
Low V_{CC} Data Retention Characteristics (T_A = -25 to +85°C)

Parameter	Symbol	Test Condition	V _{CC} ≥ 2.7 V			V _{CC} ≥ 2.2 V			V _{CC} ≥ 1.8 V			Unit
			μPD444012A -BxxX			μPD444012A -CxxX			μPD444012A -DxxX			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V _{CCDR1}	/CE1 ≥ V _{CC} – 0.2 V, CE2 ≥ V _{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	V
	V _{CCDR2}	CE2 ≤ 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	
	V _{CCDR3}	/LB = /UB ≥ V _{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} – 0.2 V	1.0		3.6	1.0		3.6	1.0		3.6	
Data retention supply current	I _{CCDR1}	V _{CC} = 1.5 V, /CE1 ≥ V _{CC} – 0.2 V, CE2 ≥ V _{CC} – 0.2 V or CE2 ≤ 0.2 V		0.3	3.0		0.3	3.0		0.3	3.0	μA
	I _{CCDR2}	V _{CC} = 1.5 V, CE2 ≤ 0.2 V		0.3	3.0		0.3	3.0		0.3	3.0	
	I _{CCDR3}	V _{CC} = 1.5 V, /LB = /UB ≥ V _{CC} – 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} – 0.2 V		0.3	3.0		0.3	3.0		0.3	3.0	
Chip deselection to data retention mode	t _{CDR}		0			0			0			ns
Operation recovery time	t _R		t _{RC} ^{Note}			t _{RC} ^{Note}			t _{RC} ^{Note}			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

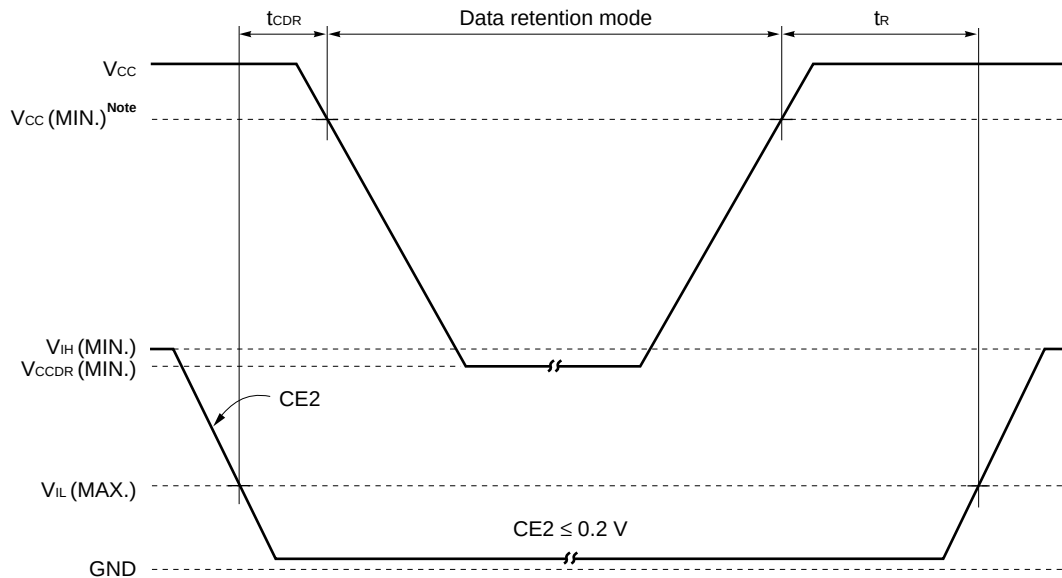
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling $\overline{\text{CE1}}$, the input level of CE2 must be $\geq V_{\text{CC}} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$. The other pins (Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$) can be in high impedance state.

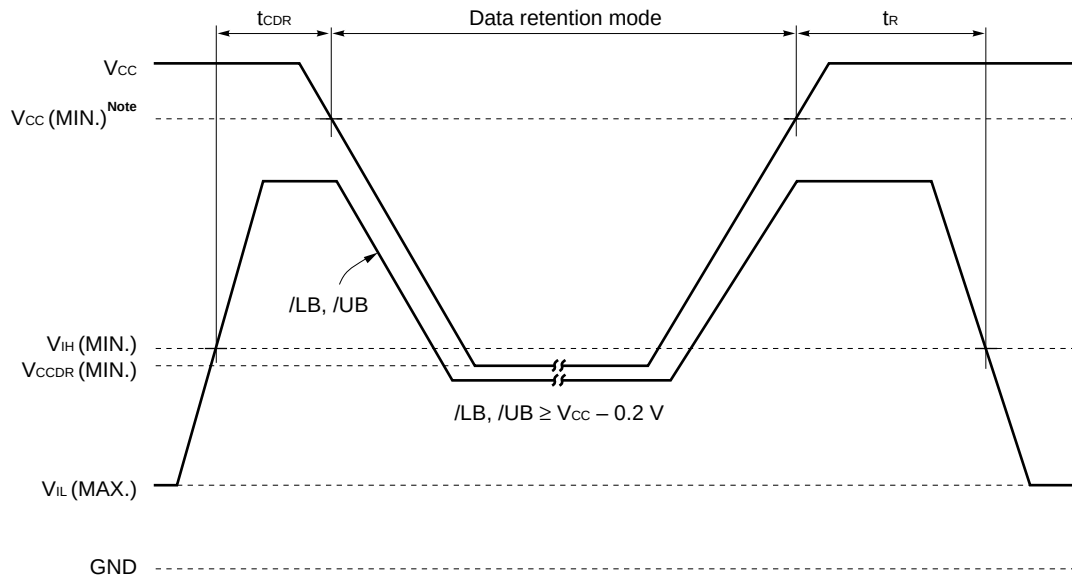
(2) CE2 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling CE2, The other pins ($\overline{\text{CE1}}$, Address, I/O, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{LB}}$, $\overline{\text{UB}}$) can be in high impedance state.

(3) /LB, /UB Controlled

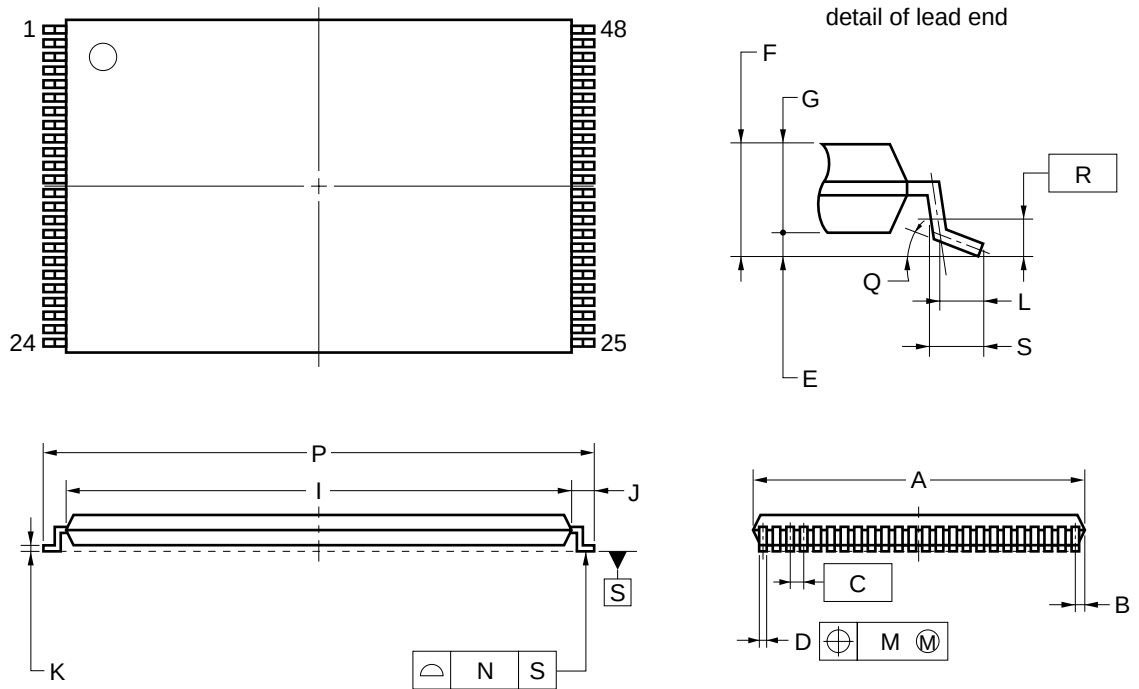


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be $\geq V_{CC} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawing

48-PIN PLASTIC TSOP(I) (12x18)



NOTES

1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
2. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	18.0±0.2
Q	3°+5° -3°
R	0.25
S	0.60±0.15

S48GY-50-MJH1-1

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μ PD444012A-X.

Types of Surface Mount Device

μ PD444012AGY-BxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

μ PD444012AGY-CxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

μ PD444012AGY-DxxX-MJH: 48-PIN PLASTIC TSOP (I) (12×18) (Normal bent)

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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