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128K x 32 EEPROM Module

PUMA 2E4001-15/17/20

Issue 4.1 : September 1996

Description

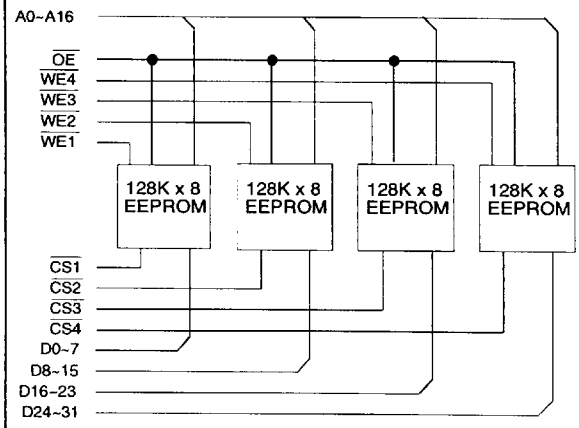
The PUMA 2E4001 is a 4Mbit CMOS EEPROM organised as 128k x 32 in a 66 pin PGA ceramic package. Access times of 150, 170 and 200ns are available. The device has a user configurable output width as by 8,16 or 32 bits with four separate Write Enables and Chip Selects. The PUMA 2E4001 has a single 5.0V supply and has $\overline{DATA}$ polling for end of write detection. Both hardware and software data protection are incorporated into this package. Page write (128 bytes) is performed in less than 10ms, there is an endurance of 10,000 Erase/Write cycles and a data retention time of 10 years.
May be processed in accordance with MIL-STD-883.

4,194,304 bit CMOS EEPROM Module

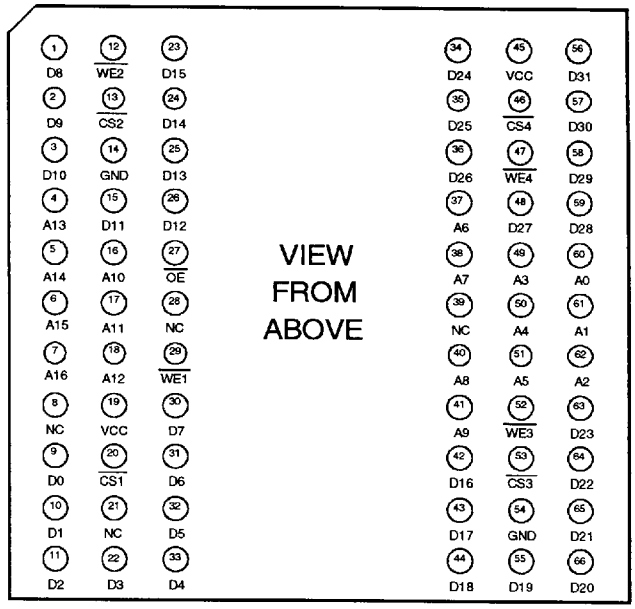
Features

- Access Times of 150/170/200 ns.
- User Configurable as 8 / 16 / 32 bit wide output.
- Operating Power 490/ 913 / 1760 mW (max).
  Low Power Standby 7mW (max).
- Page Write (128 Bytes) in 10ms max.
- $\overline{DATA}$ Polling and Toggle bit indication of end of Write.
- Hardware and Software Data Protection.
- Endurance of 10^4 Erase/Write Cycles and Data Retention Time of 10 years.
- Available in accordance with MIL-STD-883.

Block Diagram



Pin Definition



Pin Functions

A0~16	Address Inputs	**D0~31**	Data Inputs/Outputs
$\overline{CS1}$~4	Chip Select	**$\overline{OE}$**	Output Enable
$\overline{WE1}$~4	Write Enables	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	°C
Storage Temperature	T_{STG}	-65 to +150	°C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.6 to +6.25	V
Output voltages with respect to GND	V_{OUT}	-0.6 to +6.25	V
Voltage on OE & A9 with respect to GND	V_{ID}	-0.6 to +13.5	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	-	V
Operating Temp Range	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (**I** Suffix)
	T_{AM}	-55	-	125	°C (**M**, **MB** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current A0-A16, $\overline{OE}$		I_{LI1}	V_{IN} = GND to V_{CC}	-	±40	µA
Input Leakage Current $\overline{WE1\text{-}4}$, $\overline{CS1\text{-}4}$		I_{LI2}	V_{IN} = GND to V_{CC}	-	±10	µA
Operating Supply Current	32 bit	I_{CC32}	I_{OUT}=0mA, f=5MHz(2)	-	320	mA
	16 bit	I_{CC16}	As above	-	166	mA
	8 bit	I_{CC8}	As above	-	89	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}$(1) = 2.0V to V_{CC}+1V	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}$(1) = V_{CC}-0.3V to V_{CC}+1	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA.	-	0.45	V
Output High Voltage		V_{OH}	I_{OH} = -400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

Operating Modes

The table below shows the logic inputs required to control the operating modes of each device on the PUMA 2E4001.

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	I	0	Data in
Standby	1	X	X	High Z
Write Inhibit	X	X	1	
Write Inhibit	X	0	X	
Output Disable	X	1	X	High Z
Chip Erase	0	I	0	

1 = V_{IH} 0 = V_{IL} X = Don't care

Note : (1) Refer to AC Programming Waveforms

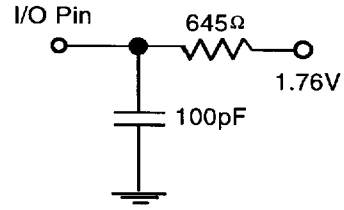
Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	A0-A16, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	16	pF
	$\overline{CS1\sim4}$, $\overline{WE1\sim4}$	C_{IN2}	V_{IN}=0V	-	34	pF
Output Capacitance		C_{OUT}	V_{OUT}=0V	-	22	pF

AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Output Test Load



AC OPERATING CONDITIONS

Read Cycle

Parameter	Symnbol	-15 min	-15 max	-17 min	-17 max	-20 min	-20 max	Unit	Notes
Read Cycle Time	t_{RC}	150	-	170	-	200	-	ns	
Address Access Time	t_{AA}	-	150	-	170	-	200	ns	
Chip Select Access Time	t_{CS}	-	150	-	170	-	200	ns	
Output Enable Access Time	t_{OE}	0	55	0	55	0	55	ns	
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns	

Notes: (1) $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.

(2) $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{CE}$ after an address transition without impact on t_{ACC}.

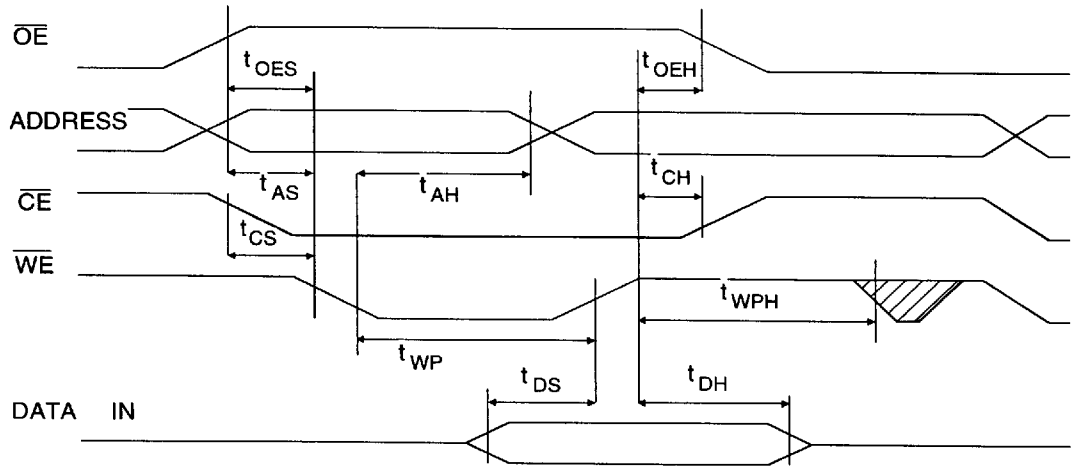
(3) t_{DF} is specified from $\overline{OE}$ or $\overline{CS\ 1\text{-}4}$ whichever occurs first (Cl=5 pf).

(4) This parameter is characterised and not 100% tested.

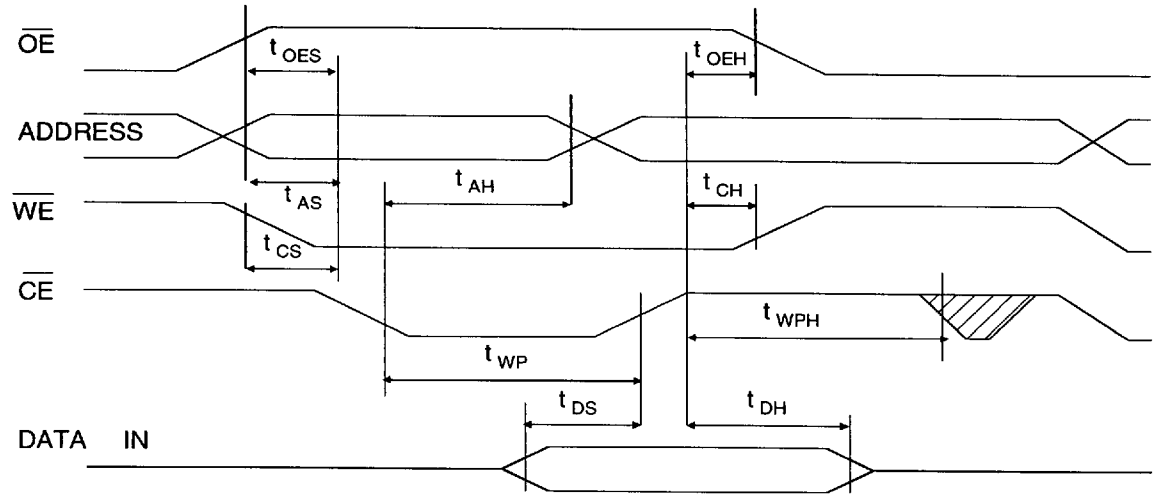
Write Cycle

Parameter	Symbol	min	typ	max	Unit
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DS}	0	-	-	ns
Byte Load Cycle	t_{BLC}	-	-	150	us

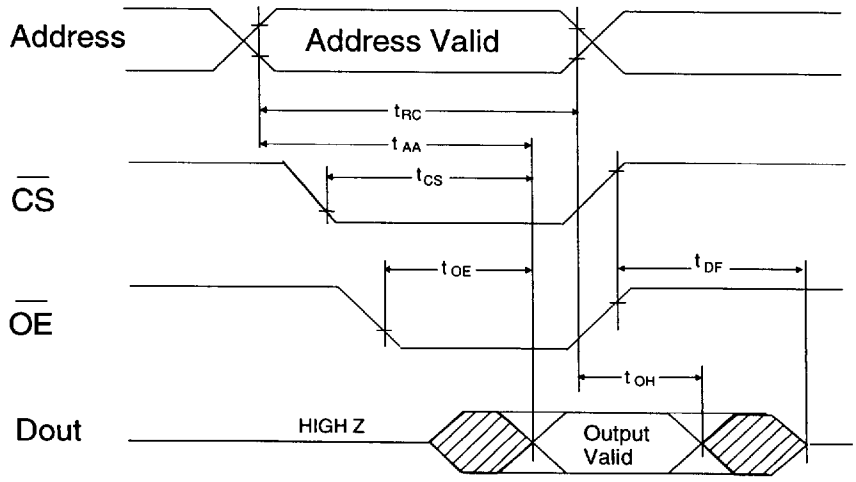
AC Write Waveform - $\overline{WE}$ Controlled



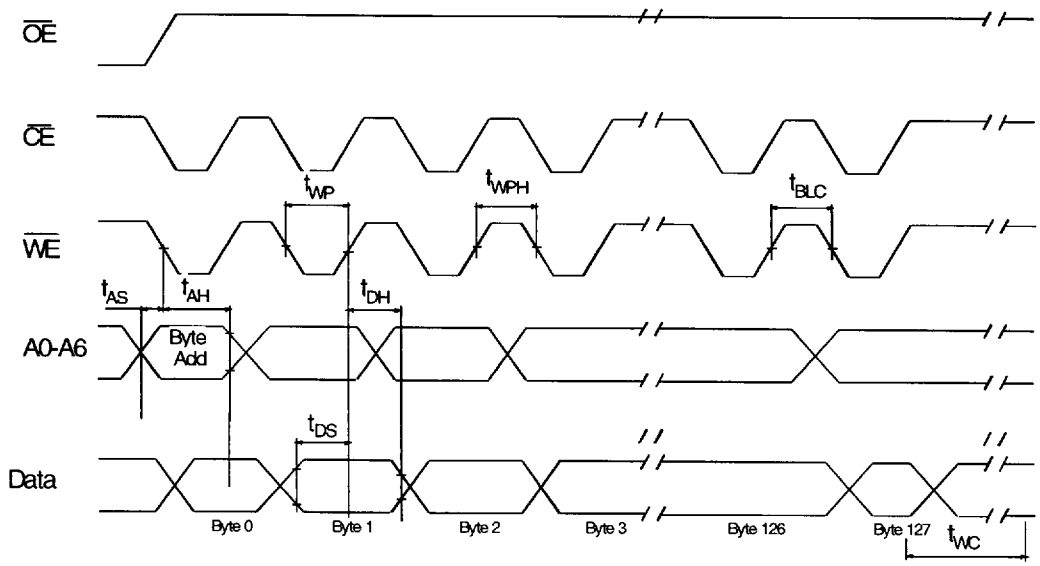
AC Write Waveform - $\overline{CS}$ Controlled



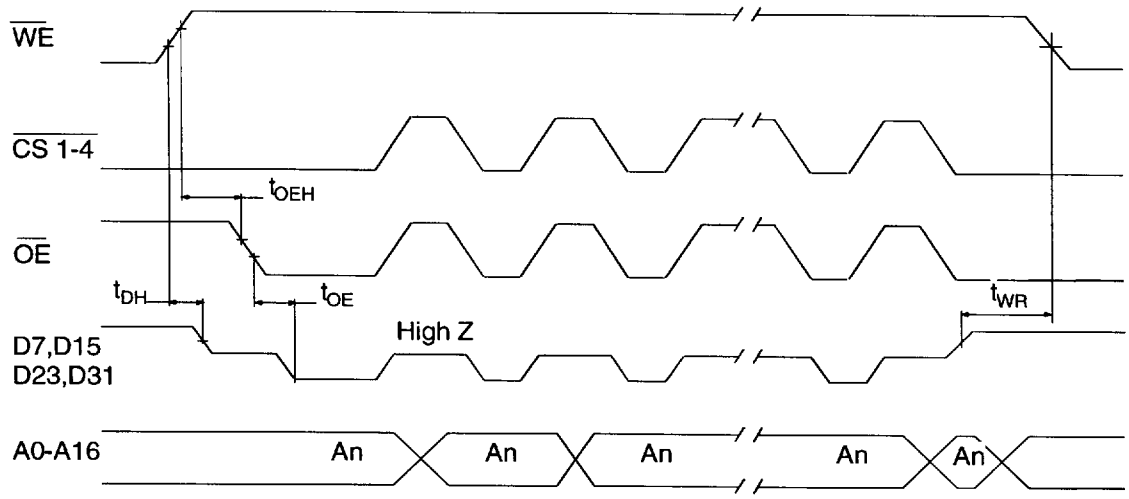
Read Cycle Timing Waveform



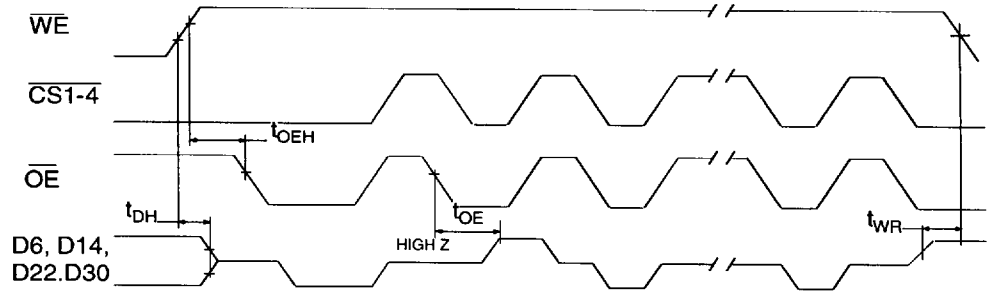
Page Mode Write Waveform



DATA Polling Waveform



Toggle Bit Waveform

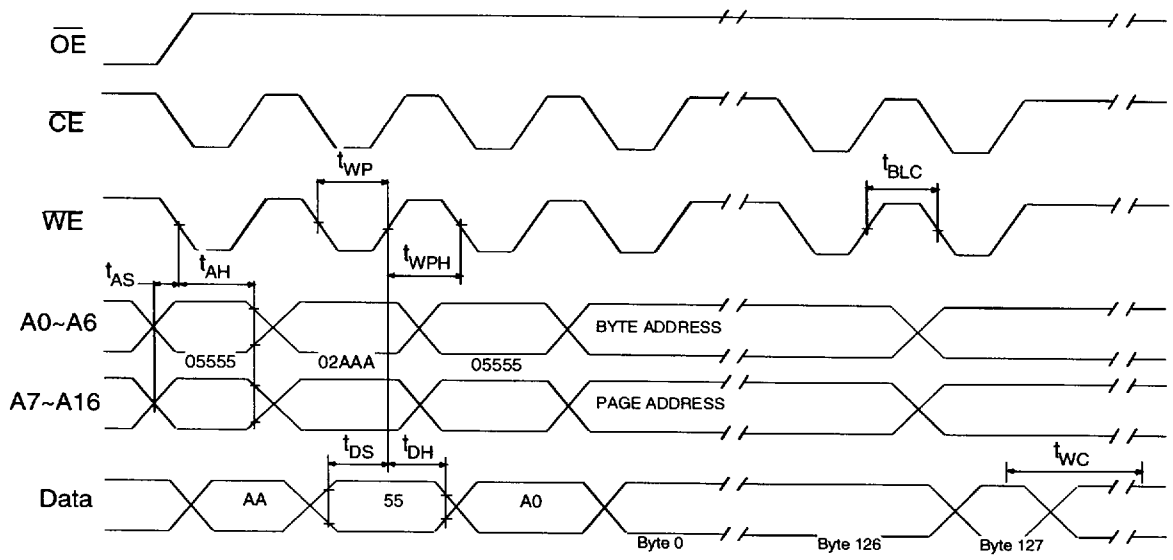


(1) Polling operations are by definition read cycles and therefore are subject to read cycle timings.

(2) Beginning and adding state of D6 may vary.

(3) Any address location may be used but the address should not vary.

Software Protected Write Waveform



Note: (1) A0-A14 must conform to the address sequence for the first three bytes.
(2) After the command sequence has been issued A7 through A16 must specify the page address during each high to low transition of WE (or CS). OE must be high only when WE and CS are both low
(3) The example above is for PUMA 2E4001 module operating in 8 bit mode.

Device Operation

Read

The PUMA 2E4001 is accessed in the same way as a static RAM. With the data stored at the memory location determined by the address pins being placed on the output pins when $\overline{CS}$ and $\overline{OE}$ are low and $\overline{WE}$ are high. Whenever $\overline{CS}$ or $\overline{OE}$ are high, the outputs are in the OFF or high impedance state.

Write

A low pulse on $\overline{WE}$ with $\overline{CS}$ low or a low pulse on $\overline{CS}$ with $\overline{WE}$ low indicates a write cycle. The address is latched on the falling edge of $\overline{CS}$ or $\overline{WE}$ and the data is latched on the first rising edge of $\overline{CS}$ or $\overline{WE}$ once a byte write has begun it will automaticaly time itself to completion

Page Mode Write

The page write feature of the device allows 1 to 128 bytes of data to be written during a single internel programming period. The host can fetch data from another location within the system during a page write operation, but the page address (A7 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initialised during any write operation. Following the initial byte the host can write up to 128 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the write enable HIGH to LOW transition, must begin within 150us (t_{BLC}) of the falling edge of the preceding write enable. If a subsequent Write Enable HIGH to LOW transition is not detected within 150 us the internal automatic programming cycle will commence.

DATA Polling

In order to detect the end of a write cycle, two methods are provided. During a write operation (Byte or Page) an attempt to read the last byte written will result in the compliment of the written data appearing on D7 (or D15, D23 or D31, depending on the device selected). Once the write cycle is completed, true data appears on the outputs and the next write cycle may begin. Using this method of indicating the end of a write can effectively reduce the total write time by 50%.

TOGGLE bit

In addition to $\overline{DATA}$ polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 (or D14, D22 or D30, depending on the device selected). toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read as normal, allowing the next write cycle to be performed. This can eliminate the software housekeeping chore of saving and fetching the last address and data written in order to implement $\overline{DATA}$ polling.

Hardware Data Protection

Both hardware and software protection is provided as described below.

Four types of hardware protection give high security against accidental writes:

- If $V_{cc} \leq 3.8V$, Write is inhibited.
- $\overline{OE}$ low, $\overline{CS}$ or $\overline{WE}$ high inhibits inadvertant Write Cycles during power-on and power-off. Write Cycle timing specifications must be observed concurrently.
- Pulses are less than 15ns on $\overline{WE}$ do not initiate a Write Cycle.
- V_{cc} Power on delay - once V_{cc} has reached 3.8V the device will automaticaly time out 5ms before allowing a write.

Software controlled data protection, once enabled by the user, means that a software algorithm must be used before any write can be performed. To enable this feature the algorithm opposite is followed, and must be reused for each subsequent write operation. Once set the data protection remains operational until it is disabled by using the second algorithm overleaf: power transitions will not reset this feature.

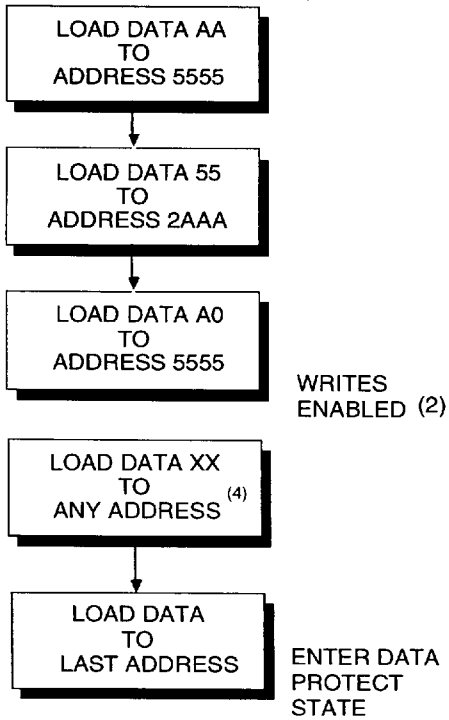
Software Data Protection

The algorithms below describe the process by which an individual 128K x 8 device on the PUMA may be software write protected and unprotected. Thus these algorithms apply to the PUMA operating in 8 bit mode; if 16 or 32 bit modes are being used, then the relevant data would be placed on the 16 or 32 bit buses as two or four 8 bit bytes respectively e.g. 5555_H and 55555555_H. In the case of 16 bit mode, this process would be repeated twice with the appropriate devices selected.

The PUMA 2E4001 is shipped with the data protection NOT ENABLED. In this mode data should be protected during power up and power down operations through the use of external circuits.

Once data protection has been enabled it is set for the life of the device unless the device unless the reset algorithm is followed. In protected mode write operations to the device(s) on the PUMA must be preceeded by a series of three write operations to three specific locations, after which 1 to 128 bytes of data may be written. Once the page load cycle is complete the device(s) return to the data protected state

NOTE:Once initiated, this sequence of write operations should not be interrupted.



Notes:

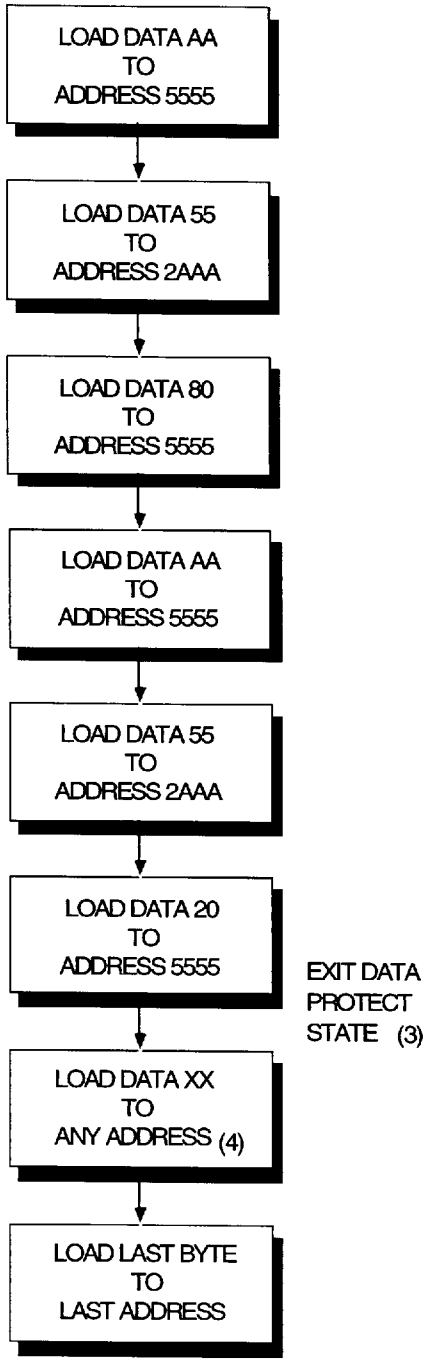
(1) Data Format I/O7-I/O0 (Hex);
Address Format: A14-A0 (Hex) (A15 don't care)
Once initiated, this sequence of write operations should not be interrupted.

(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.

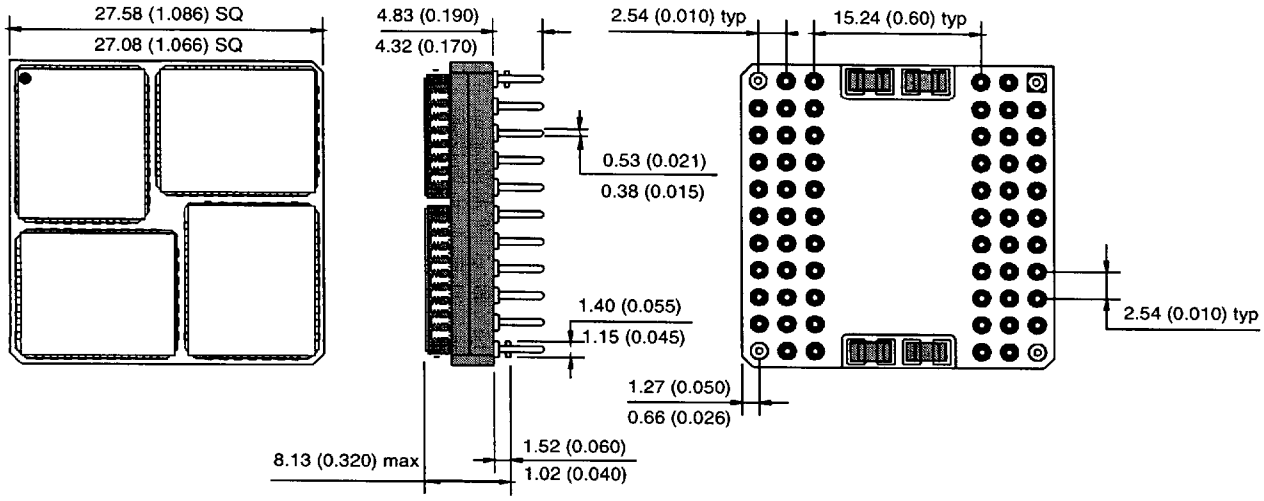
(3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.

(4) 1 to 128 bytes of data may be loaded.

Software Data Protect Disable



Package Details Dimensions in inches.



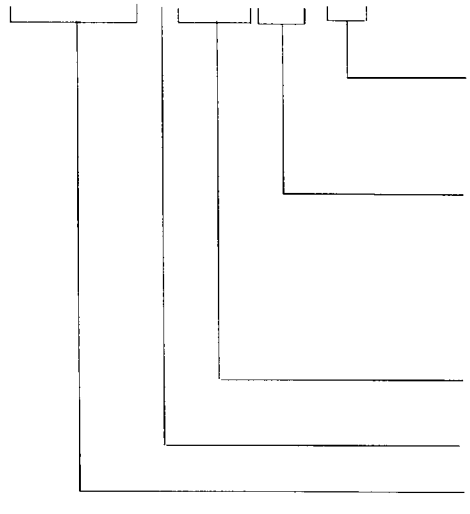
Military Screening Procedure

Module Screening Flow for high reliability product is in accordance with Mil-883 method 5004 .

MB MODULE SCREENING FLOW		
SCREEN	***TEST METHOD***	***LEVEL***
Visual and Mechanical		
External visual	2017 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition C (10 Cycles, -65°C to +150°C)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable Device Specifications at T_A=+25°C	100%
Burn-in	T_A=+125°C,160hrs minimum.	100%
Final Electrical Tests	Per applicable Device Specification	
Static (DC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (AC)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at Post Burn-in at T_A=+25°C	10%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2E4001MB-15



Speed	15	= 150 ns
	17	= 170 ns
	20	= 200 ns
Temp. range/screening	Blank	= Commercial Temperature
	I	= Industrial Temperature
	M	= Military Temperature
	MB	= Screened in accordance with MIL-STD-883.
Organisation	4001	= 128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	E	= EEPROM
Package	PUMA 2	= 66 pin Ceramic PGA