Preferred Device

Product Preview

SMARTDISCRETES™ 52 Amps, 40 Volts

Self Protected with Temperature Sense

N-Channel D2PAK

SMARTDISCRETES devices are an advanced series of Power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on–resistance per silicon area while incorporating additional features such as clamp diodes. They are capable of withstanding high energy in the avalanche and commutation modes. The avalanche energy is specified to eliminate guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

This new SMARTDISCRETES device features integrated Gate-to-Source diodes for ESD protection, and Gate-to-Drain clamp for overvoltage protection. Also, this device integrates a sense diode for temperature monitoring.

- Ultra Low RDS(on) Provides Higher Efficiency
- IDSS Specified at Elevated Temperature
- Avalanche Energy Specified
- Overvoltage Protection
- Temperature Sense Diode
- ESD Human Body Model Discharge Sensitivity Class 3

MAXIMUM RATINGS (T_{.J} = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	VDSS	40	Vdc
Drain-to-Gate Voltage	VDGR	40	Vdc
Gate-to-Source Voltage	VGS	±10	Vdc
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ (Note 1.) ($V_{DD} = 25$ Vdc, $V_{GS} = 5.0$ Vdc, $I_{L(pk)} = 25$ A, $L = 1.4$ mH, $R_G = 10$ k Ω)	E _{AS}	450	mJ
Drain Current - Continuous @ T _A = 25°C - Continuous @ T _A = 140°C - Single Pulse (t _p ≤10 μs)	I _D I _D	52 25 200	Adc
Total Power Dissipation (t ≤ 10 seconds) Linear Derating Factor	P _D @ T _A = 25°C	115 0.76	W W/°C
Thermal Resistance – Junction–to–Case – Junction–to–Ambient (Note 1.)	R _θ JC R _θ JA	1.3 80	°C/W

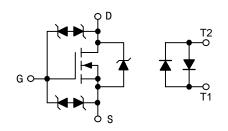
1. Measured while surface mounted to an FR4 board using the minimum recommended pad size. Typical value is 64°C/W.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



http://onsemi.com

52 AMPERES 40 VOLTS RDS(on) = 20 m Ω





D²PAK CASE 936D PLASTIC





TBD = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NIB6404-5L	D ² PAK	TBD

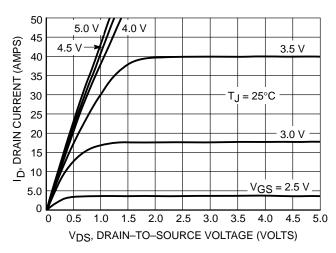
Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_.J = 25°C unless otherwise noted)

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS		•				
Drain–to–Source Breakdown Voltage (Note 2.) (V _{GS} = 0 Vdc, I _D = 250 μAdc, –55°C < T _J < 175°C) Temperature Coefficient (Negative)			40 -	51 7.0	55 -	Vdc mV/°C
Gate-to-Source Clamp Voltage (Note 2.) (VGS = 0 Vdc, IG = 20 µAdc)			10	13	20	Vdc
Zero Gate Voltage Drain Current (VDS = 35 Vdc, VGS = 0 Vdc) (VDS = 15 Vdc, VGS = 0 Vdc) (VDS = 35 Vdc, VGS = 0 Vdc, TJ = 125°C)			- - -	1.1 0.2 4.0	100 2.0 20	μAdc
Gate-Body Leakage Current (VGS	$= 5.0 \text{ Vdc}, \text{ V}_{DS} = 0 \text{ Vdc})$	IGSS	-	0.02	1.0	μAdc
ON CHARACTERISTICS (Note 2.)						
Gate Threshold Voltage (Note 2.) (VDS = VGS, ID = 1.0 mAdc) Threshold Temperature Coefficient (Negative)			1.0 _	1.7 4.5	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2.) (VGS = 5.0 Vdc, I _D = 20 Adc)			-	18	20	mΩ
Forward Transconductance (V _{DS} =	= 15 Vdc, I _D = 10 Adc) (Note 2.)	9FS	TBD	34	-	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	_	1720	_	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0 \text{ Vdc},$ f = 1.0 MHz)	C _{oss}	-	525	-	
Transfer Capacitance]	C _{rss}	-	120	-	
SWITCHING CHARACTERISTICS (Note 3.)	'		•		•
Turn-On Delay Time		td(on)	-	16	_	ns
Rise Time	$(V_{DD} = 32 \text{ Vdc}, I_D = 25 \text{ Adc},$	t _r	_	263	_	-
Turn-Off Delay Time	$V_{GS} = 5.0 \text{ Vdc},$ $R_{G} = 10 \Omega$ (Note 2.)	td(off)	_	149	-	
Fall Time	1	t _f	_	345	_	
Gate Charge		QT	_	29	-	nC
	(V _{DS} = 32 Vdc, I _D = 25 Adc, V _{GS} = 5.0 Vdc) (Note 2.)	Q ₁	_	6.0	_	
		Q ₂	_	16	-	
		Q ₃	_	2.0	-	
SOURCE-DRAIN DIODE CHARAC	FERISTICS	<u>'</u>		•		
Forward On-Voltage	(I _S = 20 Adc, V _{GS} = 0 Vdc) (Note 2.) (I _S = 20 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	_ _	0.876 0.746	1.2 -	Vdc
Reverse Recovery Time		t _{rr}	-	60	_	ns
	(I _S = 25 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs) (Note 2.)	ta	_	29	_	
		t _b	_	32	_	
Reverse Recovery Stored Charge		Q _{RR}	_	80	_	рС
TEMPERATURE SENSE DIODE CH	ARACTERISTICS			•		•
Forward (Payaraa) On Valtage	(I _{F(R)} = 250 μAdc) (Note 2.)	VAC(ACR)	715 –	743 570	775 –	mVdc
Forward (Reverse) On–Voltage	$(I_{F(R)} = 250 \mu\text{Adc}, T_J = 125^{\circ}\text{C})$			0.0		
Temperature Coefficient (Negative)	$(I_{F(R)} = 250 \mu Adc, T_J = 125^{\circ}C)$ $I_{F(R)} = 250 \mu Adc,$ $T_J = 160^{\circ}C$	VFTC	1.57	1.71	1.85	mV/°C

Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS



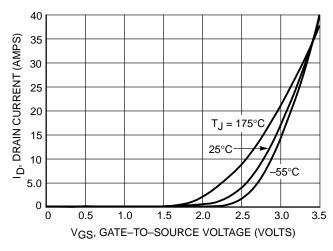


Figure 1. On-Region Characteristics

RDS(on), DRAIN-TO-SOURCE RESISTANCE (m\Overline{O}) 50 45 T_J = 175°C 40 35 30 25 25°C 20 15 10 -55°C 10 20 30 40 <u>5</u>0 ID, DRAIN CURRENT (AMPS)

Figure 2. Transfer Characteristics

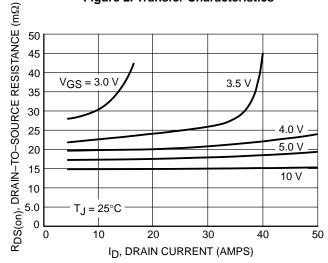
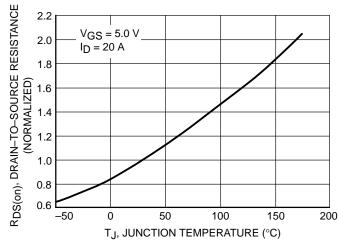


Figure 3. On–Resistance versus Drain Current and Temperature

Figure 4. On–Resistance versus Drain Current and Gate Voltage



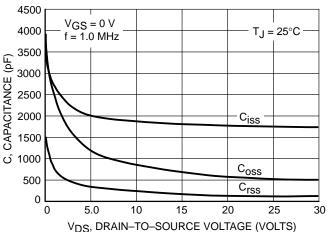
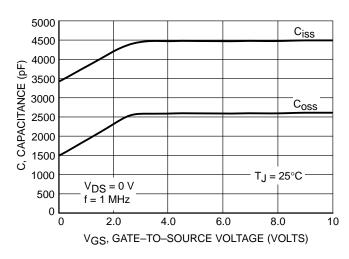


Figure 5. On–Resistance Variation with Temperature

Figure 6. Capacitance Variation

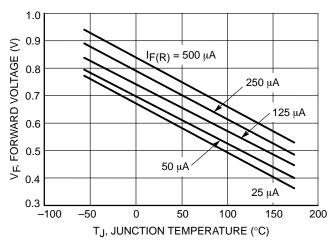
TYPICAL ELECTRICAL CHARACTERISTICS



20 18 IS, SOURCE CURRENT (A) 16 14 12 10 8.0 6.0 $T_{\rm J} = 175^{\circ}{\rm C}$ 4.0 25°C 2.0 0.2 0.3 0.4 0.5 0.6 0 0.7 VSD, SOURCE-TO-DRAIN VOLTAGE (VOLTS)

Figure 7. Capacitance Variation

Figure 8. Diode Forward Voltage versus Current



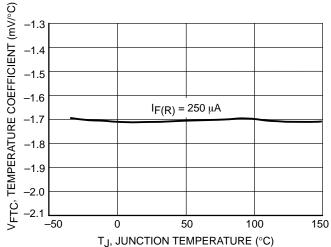


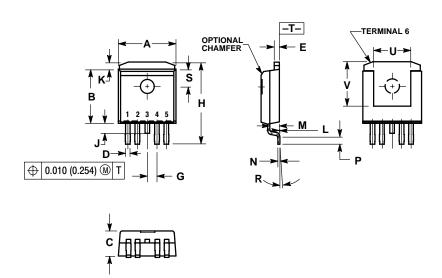
Figure 9. Sense Diode Forward Voltage Variation with Temperature

Figure 10. Sense Diode Temperature Coefficient Variation with Temperature

PACKAGE DIMENSIONS

DPAK

CASE 936D-03 **ISSUE B**



NOTES:

- OTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
 4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
 5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.386	0.403	9.804	10.236	
В	0.356	0.368	9.042	9.347	
С	0.170	0.180	4.318	4.572	
D	0.026	0.036	0.660	0.914	
E	0.045	0.055	1.143	1.397	
G	0.067	BSC	1.702 BSC		
Н	0.539	0.579	13.691	14.707	
J	0.125	MAX	3.175 MAX		
K	0.050 REF		1.270 REF		
L	0.000	0.010	0.000	0.254	
M	0.088	0.102	2.235	2.591	
N	0.018	0.026	0.457	0.660	
P	0.058	0.078	1.473	1.981	
R	5°REF		5° REF		
S	0.116 REF		2.946 REF		
U	0.200 MIN		5.080 MIN		
V	0.250 MIN 6.350 M		MIN		

Notes

Notes

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JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031

Phone: 81–3–5740–2700 **Email**: r14525@onsemi.com

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